

SOI-based monolithic integration of SiON and Si planar optical circuits

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ABSTRACT

In recent years there has been a growing interest in using Silicon on Insulator (SOI) as a platform for integrated planar optical circuits [1], this is mainly due to the high quality yield volume processes demonstrated by the CMOS manufacturing industry and recent MEMS technology progress[2]. In this work we present monolithic integration of Silicon and SiON planar lightwave circuits on a single SOI chip processed in a CMOS fabrication environment. The demonstration of a processing scheme that yields low loss waveguides for both silicon and SiON as well as efficient transition of light between the two materials is the goal of this present work. The patterning of waveguides in both silicon and SiON regions is done in a self aligned process using one lithography mask and two separate dry etch steps each highly selective to one of the two materials. The effect of a high temperature anneal on the IR absorption of SiON related N-H bond was measured using FTIR and waveguide optical loss. Up to 98% reduction in absorption is demonstrated which allows acceptable loss across the C-band. We have achieved low propagation loss, single mode, and rib waveguides for both Silicon and SiON core regions as well as low loss silicon-SiON waveguides junction. The silicon-SiON junction loss has been measured to be 0.9+/-0.1dB, only 0.3dB greater than the theoretical value determined by Fresnel's facet reflection. A new design of surface corrugated Bragg grating on the SiON section of the integrated device is described where the grating is embedded within the core which is composed of two slightly skewed index SiON layers. We show 8 times improvement of the grating spectral thermal stability compared to the previous work done on SOI platform. Achieving silicon-SiON monolithic integration of planar waveguide circuit enables future integration of already demonstrated applications, e.g., silicon can be used to achieve fast modulation, optical amplification, and Raman lasing whereas SiON can be used for a-thermal Bragg grating filters and efficient fiber-waveguide coupling.

Keywords: Bragg grating, Waveguide, Silicon, SiON, C-MOS, SOI.

1. INTRODUCTION

SOI based Silicon light circuits have been extensively investigated in the past few years. The potential of the Silicon as an optical material for the near IR applications was realized and significant progress has been made in this field. Fast modulation [3] and Raman lasing [4] are just two examples of recent advances in the field of Silicon Photonics. The cost effective and the mature Silicon CMOS technology provide a convenient environment for the development of SOI based photonic platform. Low cost substrate and high volume manufacturing techniques may be used for the development of photonic devices comparable to that currently realized with III-V materials and far more. In addition, recently developed Silicon MEMS technology provides passive alignment technology that can be used to

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package a chip level device with optical fiber and with a light source. By integration of multiple photonic devices on a cost-effective platform there is a hope to drive applications to high volume, reducing costs further and opening up new markets. Monolithic integration of both the optical and the electronic components on a single chip is especially a promising technology as the standard CMOS electrical circuitry technology is approaching a data transfer barrier due to metallic interconnect RF radiation.

Silicon has many material attributes that make it the ideal choice for optical integration: its high refractive index can result in small footprint devices; high thermal conductivity and a relatively large thermo-optic coefficient mean efficient thermally driven devices. While for some applications these attributes are an advantage, for others they can cause difficulties: high refractive index may cause high scattering losses, large thermal conductivity results in difficult isolation for many devices on a single chip, and a large thermo-optic coefficient may cause problems for un-cooled applications. Therefore monolithic integration of an additional optical material, other than silicon, which has complimentary qualities has high potential of yielding more flexible and rich platform altogether.

One of the commonly used materials in the CMOS industry that meets the above requirements is silicon-oxynitride (SiON) which was independently investigated extensively as an optical material [4]. Common techniques of deposition allow control over wide a range of n - the index of Refraction. By setting the nitrogen to oxygen ratio of the deposited film, n can be set to any value between 1.45 similar to silicon-di-oxide and 2.0 typical to silicon-nitride. Control over n in this range allows both low contrast planar waveguides for optical fiber mode matching, as well as high contrast waveguides that are matched with silicon optical mode and hence an attractive candidate to be included in SOI based integration. The goal of this work is to use well known CMOS techniques to define areas of SiON on an SOI platform such that a low loss planar waveguide circuit of the two combined materials is achieved. In addition we show realization of a waveguide grating that is less sensitive to temperature as one of the supplementary capabilities of the integrated device enabled by the reduced thermo-optic coefficient of SiON (~ 8 times less than silicon).

2. PROCESSING and RESULTS

For fabrication we use 6" SOI wafers that have 2 μm of EPI-silicon and thick (3 μm) Buried Oxide (BOX) which is larger than the BOX thickness values commonly used for silicon light-wave circuits (0.4-1.0 μm). This thicker bottom cladding is needed to prevent leakage of optical power to the substrate where the mode of the SiON waveguide is less confined than compared to the silicon waveguide. The first step of the processing is defining the SiON area in resemblance to the well known CMOS approach of forming isolation regions on a silicon substrate by dry-etching silicon and later filling the trenches with Silicon-di-oxide. As shown in Fig1, SiON pads are formed on the top of the BOX where silicon is removed. The silicon etch is done in the presence of thin (0.2 μm) Silicon-oxide used as hard mask through high density SF6-O2 plasma etcher. The etch processing characteristics are designed to be highly selective: a silicon to SiO₂ etch rate ratio greater than 30 results in a very fine control over the penetration to the BOX, measured to be in the range of 30 to 50nm (Fig 2). Another requirement on the etching is to form smooth surface at the top of the BOX of ~1nm RMS roughness as measured by atomic force microscope (AFM). In addition the etched silicon sidewall should be very close to vertical and smooth. Both features are essential for a low loss Si to SiON waveguide junction which is presented later.

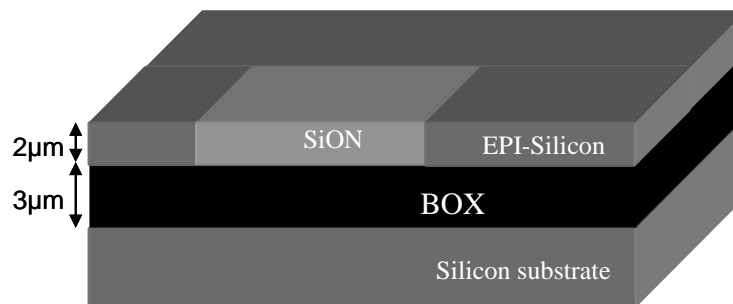


Figure 1: Schematics of SiON pad formation replacing EPI-silicon pads. Thick 3 μm BOX is needed to prevent leakage of the optical mode to the silicon substrate.

After forming the trenches a SiON layer is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) tool. The top plate is powered at a frequency of 13.56 MHz and the deposition temperature is 400C. The plasma chamber pressure is controlled through pumping rate and gas feeding. Three gas types involved in the deposition process: Silane (SiH₄) diluted in N₂, nitrous oxide (N₂O) and ammonia (NH₃). The deposition chamber pressure, the RF power and the gas flow rates were calibrated to achieve the desired refractive index and deposition rate. Figure 3 shows the effect of ammonia to silane flow rate ratio on the film refractive index as measured by ellipsometry on a reference sample of 1μm film SiON deposited on silicon wafer at 632.8 nm. A SiON index range of 1.6 to 1.7 yields high contrast waveguide that match the silicon waveguide mode shape without cracking in subsequent thermal anneal step which is more likely to happen for layers with n>1.7. Standard Chemical Mechanical Polishing (CMP) is then used to remove the excess SiON from the top of the silicon section. Careful control over the polish end-point setting is required as the depth of the penetration to the EPI-silicon level determines the waveguide height for both silicon and SiON as shown in Fig 2.

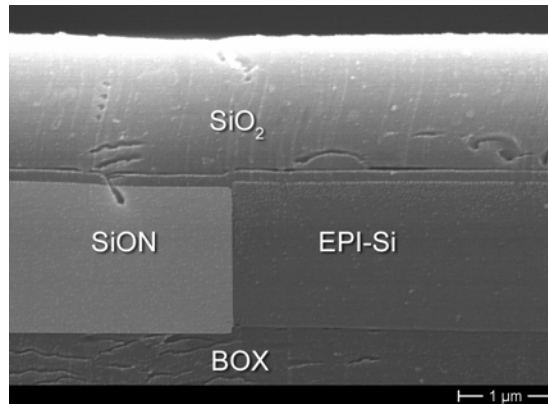


Figure 2: X-sectional SEM image of the Silicon/SiON waveguide junction (with the SiON highlighted for clarity). Interface smoothness and verticality is achieved by SF₆/O₂ plasma etch as well as small (~50nm) penetration to the BOX in the SiON area.

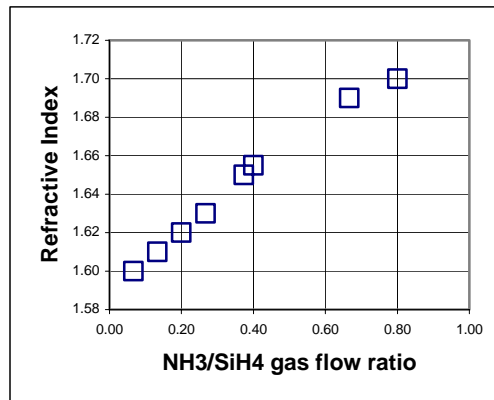


Figure 3: The effect of NH₃/SiH₄ gas flow ratio on refractive index. The desired index range of 1.6 to 1.7 can be achieved with ~0.002 repeatability and deposition rate of ~0.8μm/min.

Next a thermal anneal step is used to reduce the concentration of hydrogen in the SiON film [4]. Since the input process involves SiH₄ and NH₃ gasses the as-deposited-SiON layer contains significant amount of hydrogen. The presence of N-H bonds cause absorption that peaks in proximity to the c-band at wavelength 1515nm, which is due to the first overtone of the N-H stretching vibration at wavenumber of 3350 cm⁻¹ as shown in the Fourier Transform Infrared (FTIR) spectrum in Fig. 4a. A blow up portion of the spectrum near the vibration frequency of interest is

depicted in Figure 4b after correction for background modulations. Optimized spectrum resolution and the signal gain allow detection of N-H concentration at the cm⁻³. The N-H concentration of the as deposited layer is measured to be $\sim 1E22$ cm⁻³ for n=1.63 film. It is reduced by annealing at 1100C-1150C in a nitrogen atmosphere to 2-7% of the as-deposited value (see Fig 5a). In addition FTIR results shows that the presence of thin (0.15 μ m) cap silicon-oxide layer that covers both silicon and SiON regions is not interfering with the anneal efficiency. On partial set of the anneal conditions (1100C only) we have measured the optical loss of SiON waveguide (which patterning details described below) in the range of 1470nm to 1620nm (Fig 5b). The anticipated absorption peak around 1515nm is at -25dB/cm for un-annealed wafer and -5dB for the 12H anneal duration. According to the FTIR measurements it is expected that more aggressive anneal conditions will yield significantly reduced absorption which would be an acceptable figure for the C-band.

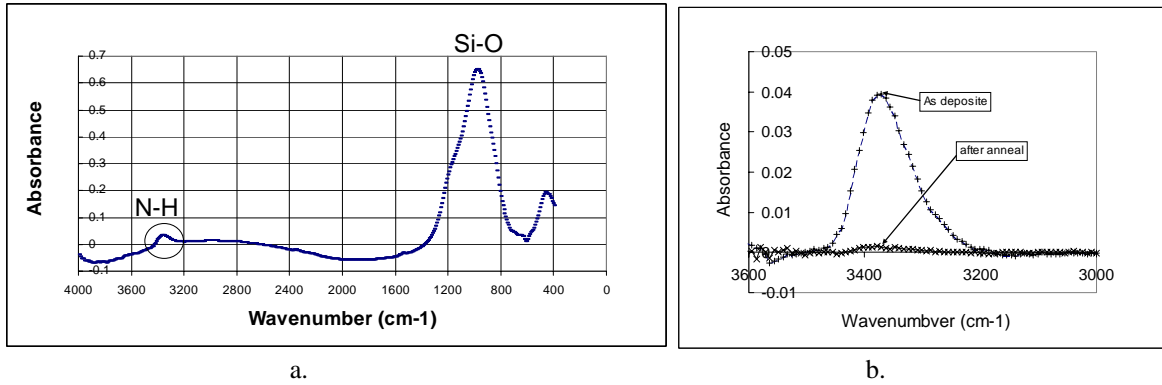


Figure 4: (a) FTIR absorbance spectrum of SiON film deposited on silicon with no thermal anneal. The N-H stretching vibration is evident at 3370 cm-1. (b) blow up of the N-H vibration area before and after thermal anneal of 12H at 1100C.

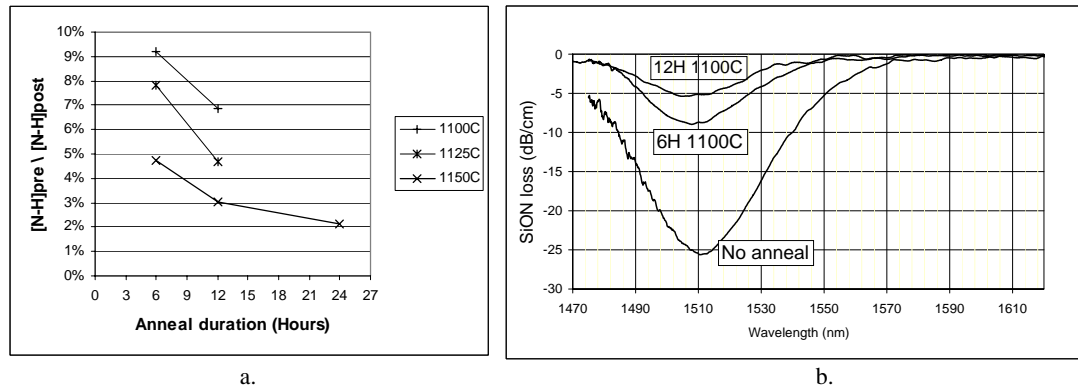


Figure 5: reduction of [N-H] concentration in SiON film as measured at various anneal conditions (a) reduction of FTIR absorbance 3370 cm-1 peak of bulk 1 μ m film deposited on silicon and (b) optical loss of 1.5 μ m rib waveguide.

The rib waveguides for both silicon and SiON are patterned using one photolithography mask and two sequential Reactive Ion Etching (RIE) steps. The two RIE plasma gasses are Ar-SF₄ and Cl₂ for SiON and silicon etch respectively. Both etch steps are highly selective to the other material which means that the silicon etch rate is much smaller than the SiON etch rate in the SiON etch step and vice versa. This novel patterning sequence has two important merits in reference of low junction loss: First there is no lateral offset between the waveguides (see Fig. 6) as the line of photo-resist that defines that pattern is continuous over the junction and secondly independent control over the rib etch depth at each side of the junction allows further mode matching.

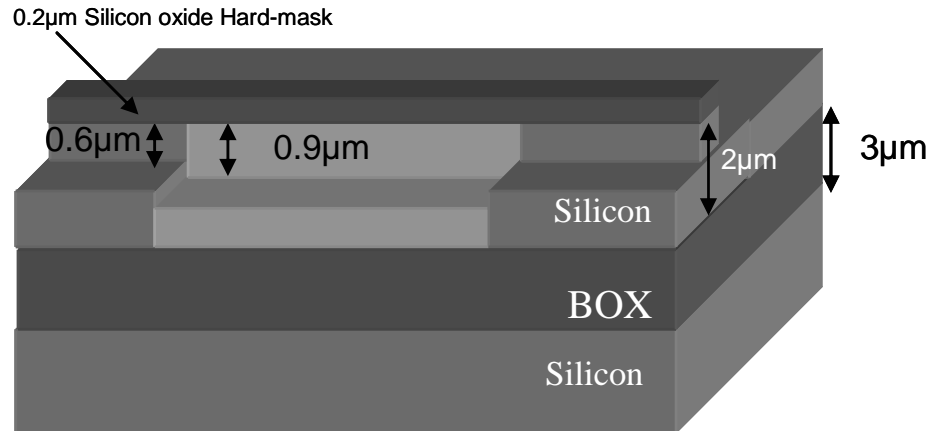


Figure 6: Silicon –SiON self alignment Rib waveguide patterning. The SiON Rib height is larger than the silicon for the purpose of reducing junction loss.

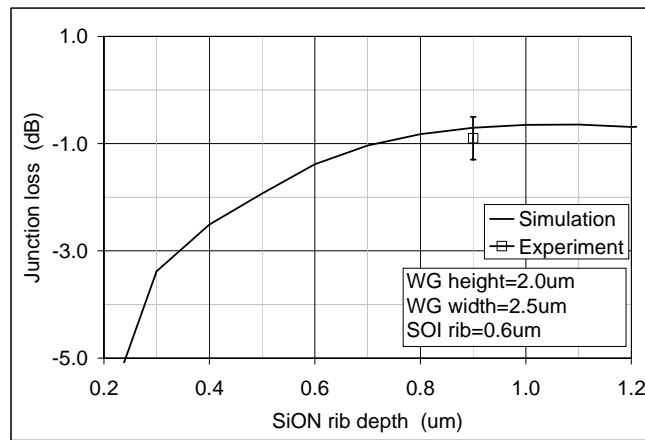


Figure 7: The junction loss for Si-SiON junction for Fixed RIB waveguide height of 0.6 μm. Optimal mode matching is achieved for SiON Rib height larger than 0.8 μm.

An important contribution to the junction loss is the Fresnel loss at the interface between the two materials of large index difference: $n(\text{SiON})=1.6-1.7$, $n(\text{Silicon})=3.45$. Using the beam propagation method to determine the effective index of the two waveguides involved we obtain a reflection of 13% at the interface corresponding to a loss of 0.6dB. Beyond this, there is a loss associated with the modal mismatch at the interface. Assuming the waveguide width and height is fixed at 2.0 μm for both waveguides, and the rib etch depth for the silicon waveguide is 0.6 μm (ensuring single mode operation) the simulated junction loss as a function of etch depth of the SiON waveguide rib is shown in Figure 7. As can be seen due to the lower confinement of the SiON waveguide its rib etch depth needs to be deeper than the silicon rib ($\sim 0.8 \mu\text{m}$) to ensure the junction loss is dominated by Fresnel reflection. By selecting a SiON rib waveguide etch depth of 0.9 μm we have demonstrated a minimum junction loss of $0.9 \pm 0.1 \text{ dB}$ which is close to the limit set by the Fresnel reflectivity.

3. SiON BRAGG GRATING

As an example of the benefit of the integration scheme described above we form waveguide-based Bragg gratings on the SiON section of the device to add thermally stable reflection and transmission filters to the existing functionalities on the SOI platform. SiON waveguide grating was already realized [5] using thermal oxide as the bottom

cladding on silicon substrate where the surface corrugated grating is located at the interface between the core and the top cladding therefore the etching depth into the core determines the coupling strength.

We introduce a new approach to construct the grating which aligns with the requirement of high contrast as shown in Figure 8. The core consists of two flavors of SiON layers with small index difference in the range of 0.01 to 0.04 which is significantly smaller than the core-clad corresponding difference. The surface corrugation is produced in the interface of SiON-1 and SiON-2. In addition the position of the grating can be set at any height within the waveguide core Fig8a and 8b are schematics representation of two such setting. In the quest for a stronger grating, the flexibility to determine grating position may be an advantage as the coupling strength is directly correlated to the interaction of the optical mode field with the grating corrugations and typically the strongest optical field is at the middle of the waveguide total height.

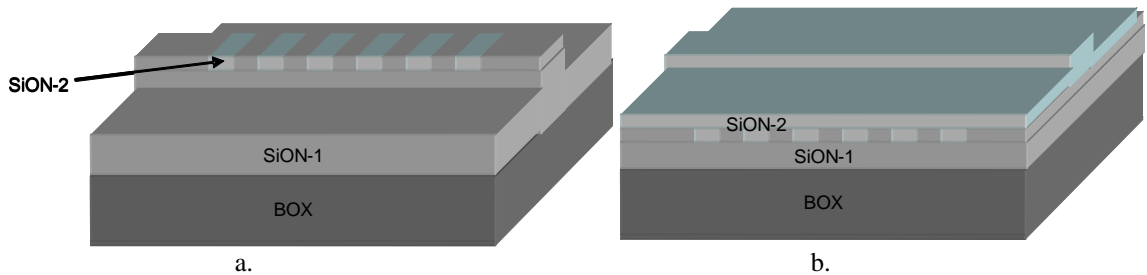


Figure 8: Schematics representation of two variations on dual SiON layer grating. The core consists of two films separately deposited. The position of the grating for type (a) is at the very top of the rib waveguide and for type (b) is embedded at the slab.

The fabrication process that is described above is then modified to include two SiON deposition steps instead of one. In between those two film depositions the grating is patterned using standard photolithography and RIE of similar characteristics to the waveguide etching that is described earlier. Special attention is needed to eliminate the formation of air void trapped during SiON-2 deposition on top of the grating trench. The grating period, duty cycle, depth as well as the deposition characteristics affects the fill quality. Typically we have used second or larger grating order that translate into $0.8\mu\text{m}$ period length with duty cycle of $\sim 50\%$ and grating depth of $0.2\text{-}0.7\mu\text{m}$. The CMP of the silicon and the SiON section is done after the SiON-2 deposition. Figure 9 shows the measured reflectivity of a 1250 period grating as a function of the grating position above the buried oxide. As expected the reflectivity peaks when the grating is positioned at the center of the waveguide.

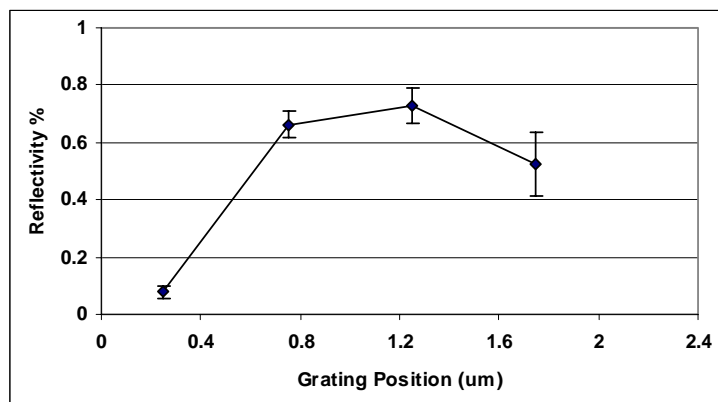


Figure 9: Bragg grating reflectivity as a function of the grating position in μm within the core (total waveguide height= $2.3\mu\text{m}$)

For demonstration of thermal stability, gratings are patterned on top of the SiON waveguide as shown in Fig 8a of 0.7 μ m depth, $n(\text{SiON-1})=1.68$, $n(\text{SiON-2})=1.69$. The spectral reflectivity of a 3.28- μ m period grating is shown in Fig. 10a. The peak reflectivity is 90% and the 3-dB bandwidth is 0.5-nm at 1344.4nm for a 1250 period grating, oscillations are seen as the gratings are not apodized. To demonstrate the diversity using different materials brings we show the difference between the thermal behavior of two sets of gratings: one fabricated from silicon (designed for 1537-nm), see ref [6] and the other fabricated in SiON (designed for 1345-nm) both sets of gratings being fabricated on an SOI wafer. As the temperature is varied from 25-82C the SiON grating shows ~8x lower thermal sensitivity as shown in Fig. 10b (due to its lower thermo-optic coefficient) than silicon based gratings making it more useful for un-cooled applications.

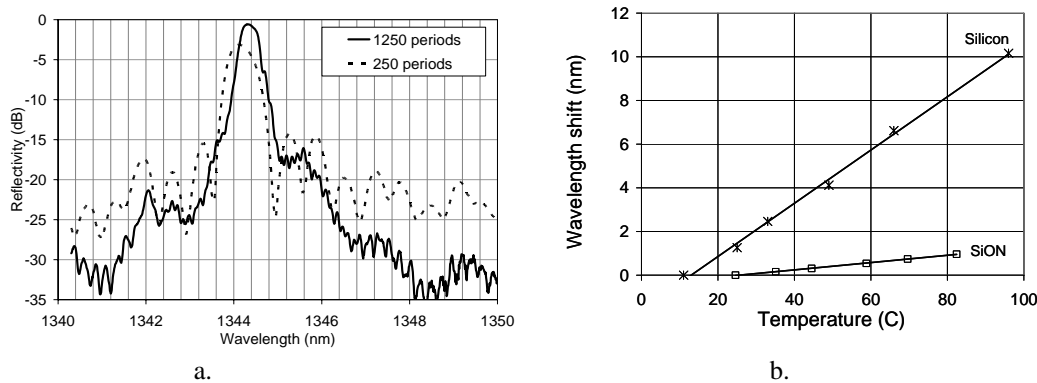


Figure 10. (a) Measured reflection spectra (in dB) for a SiON grating integrated onto SOI; (b) Thermal shift of the reflection spectra of two gratings integrated onto SOI one made of silicon and one SiON.

4. CONCLUSIONS

In this paper we demonstrate the feasibility of integrating SiON waveguides with silicon waveguide on SOI platform. The integrated lightwave circuit exhibits low optical loss for both types of waveguides as well as for the junction. The SiON absorption peak intensity at 1515nm was substantially reduced by thermal treatment as part of the integrated processing. We demonstrate the advantages of using different materials by comparing the thermal performance of silicon and SiON gratings fabricated on SOI.

ACKNOWLEDGEMENTS

The authors would like to thank Duc Tran, Larisa Peremislov, Assia Barkai, Rami Cohen, Dani Hak and Rami Gabay for technical assistance in device fabrication; to Andrew Alduino for backend processing, and to Sean Koehl for data collection software.

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