

Electrically pumped hybrid AlGaInAs-silicon evanescent laser

Alexander W. Fang¹, Hyundai Park¹, Oded Cohen³, Richard Jones², Mario J. Paniccia²,
and John E. Bowers¹

¹University of California, Santa Barbara, Department of Electrical and Computer Engineering, Santa Barbara, CA 93106, USA

²Intel Corporation, 2200 Mission College Blvd, SC12-326, Santa Clara, California 95054, USA

³Intel Corporation, S.B.I. Park Har Hotzvim, Jerusalem, 91031, Israel
awfang@enr.ucsb.edu

Abstract: An electrically pumped light source on silicon is a key element needed for photonic integrated circuits on silicon. Here we report an electrically pumped AlGaInAs-silicon evanescent laser architecture where the laser cavity is defined solely by the silicon waveguide and needs no critical alignment to the III-V active material during fabrication via wafer bonding. This laser runs continuous-wave (c.w.) with a threshold of 65 mA, a maximum output power of 1.8 mW with a differential quantum efficiency of 12.7 % and a maximum operating temperature of 40 °C. This approach allows for 100's of lasers to be fabricated in one bonding step, making it suitable for high volume, low-cost, integration. By varying the silicon waveguide dimensions and the composition of the III-V layer, this architecture can be extended to fabricate other active devices on silicon such as optical amplifiers, modulators and photo-detectors.

©2006 Optical Society of America

OCIS codes: (140.5960) Semiconductor lasers; (250.5300) Photonic integrated circuits.

References and links

1. G. T. Reed, "The optical age of silicon," *Nature* **427**, 615–618 (2004).
2. G. T. Reed, and A. P. Knights, *Silicon Photonics: An Introduction*, (John Wiley, Chichester, West Sussex, 2004).
3. L. Pavesi, D. J. Lockwood, eds., *Silicon Photonics*, (Springer-Verlag, Berlin, 2004).
4. D. A. B. Miller, "Optical interconnects to silicon," *IEEE J. Sel. Top. Quantum Electron.* **6**, 1312–1317 (2000).
5. R. S. Jacobsen, "Strained silicon as a new electro-optic material," *Nature* **441**, 199-202 (2006).
6. V. R. Almeida, C. A. Barrios, R. R. Panepucci, and M. Lipson, "All-optical control of light on a silicon chip," *Nature* **431**, 1081-1084 (2004).
7. H. Rong, "A continuous-wave Raman silicon laser," *Nature* **433**, 725-728 (2005).
8. O. Boyraz, and B. Jalali, "Demonstration of a silicon Raman laser," *Opt. Express* **12**, 5269 (2004).
9. R. Espinola, J. Dadap, R. Osgood, Jr., S. McNab, and Y. Vlasov, "Raman amplification in ultrasmall silicon-on-insulator wire waveguides," *Opt. Express* **12**, 3713-3718 (2004).
10. S. G. Cloutier, P. A. Kosyrev, and J. Xu, "Optical gain & stimulated emission in periodic nanopatterned crystalline silicon," *Nature Materials* **4**, 887 (2005).
11. L. Pavesi, L. Dal Negro, C. Mazzoleni, G. Franzò, and F. Priolo, "Optical gain in silicon nanocrystals," *Nature* **408**, 440–444 (2000).
12. A. Irrera, et al., "Electroluminescence properties of light emitting devices based on silicon nanocrystals," *Physica E* **16**, 395-399 (2003).
13. B. Gelloz and N. Koshida, "Electroluminescence with high and stable quantum efficiency and low threshold voltage from anodically oxidized thin porous silicon diode," *J. Appl. Phys.* **88**, 4319-4324 (2000).
14. S. Lombardo, "A Room-temperature luminescence from Er³⁺-implanted semi-insulating polycrystalline silicon," *Appl. Phys. Lett.* **63**, 1942–1944 (1993).
15. K. Kato, and Y. Tohmori, "PLC hybrid integration technology and its application to photonic components," *IEEE J. Sel. Topics. Quantum Electron* **6**, 4-13 (2000)
16. E. L. Friedrich, M. G. Oberg, B. Broberg, S. Nilsson, and S. Valette, "Hybrid integration of Semiconductor Lasers with Si-based single-mode ridge waveguides," *J. Lightwave Technol.* **10**, 336-340 (1992)

17. J. Sasaki, M. Itoh, T. Tamanuki, H. Hatakeyama, S. Kitamura, T. Shimoda, T. Kato, "Multiple-chip precise self-aligned assembly for hybrid integrated optical modules using Au-Sn solder bumps," *IEEE Transactions on Advanced Packaging* **24**, 569-575 (2001).
18. C. Monat, et al., "InP membrane-based microlasers on silicon wafer: microdisks vs. photonic crystal cavities," *Conference Proceedings to the 2001 International Conference on Indium Phosphide Materials FA24*, 603-606 (2001)
19. S. Mino et al. "Planar lightwave circuit platform with coplanar waveguide for opto-electronic hybrid integration," *J. Lightwave Technol.* **13**, 2320 (1995).
20. H. T. Hattori, "Heterogeneous integration of Microdisk lasers on silicon strip Waveguides for Optical Interconnects," *IEEE Photon. Technol. Lett.* **18**, 223-225 (2006).
21. H. Park, H., A. W. Fang, S. Kodama, and J. E. Bowers, "Hybrid silicon evanescent laser fabricated with a silicon waveguide and III-V offset quantum wells," *Opt. Express* **13**, 9460-9464 (2005).
22. A. Karim, et al. "Super lattice barrier 1528-nm vertical-cavity laser with 85oC continuous-wave operation," *IEEE Photon. Technol. Lett.* **12**, 1438, (2000).
23. D. Pasquariello, et al. "Plasma-Assisted InP-to-Si Low Temperature Wafer Bonding," *IEEE J. Sel. Topics Quantum Electron.* **8**, 118, (2002).
24. H. Boudinov, H. H. Tan, and C. Jagadish, "Electrical isolation of n-type and p-type InP layers by proton bombardment," *J. Appl. Phys.* **89-10**, 5343-5347 (2001).
25. B. W. Hakki, and T. L. Paoli, "CW degradation at 300K of GaAs double-heterostructure junction lasers –II: Electronic gain," *J. Appl. Phys.* **44**, 4113-4119 (1973)
26. N. Margalit, "High-temperature long-wavelength vertical-cavity lasers," Ph.D. Thesis, University of California Santa Barbara, (1998).
27. R. Ramaswamy, K. N. Sivarajan, *Optical networks: a practical perspective*, (Academic Press, San Francisco, 2002).
28. J. H. Marsh, and A. C. Bryce, "Fabrication of photonic integrated circuits using quantum well intermixing," *Mater. Sci. Eng. B* **24**, 272-278, (1994).
29. J. Geske, V. Jayaraman, Y. L. Okuno, and J. E. Bowers, "Vertical and lateral heterogeneous integration," *Appl. Phys. Lett.* **79**, 1760-2, (2001).

1. Introduction

Silicon based optoelectronic integration offers the promise of low-cost solutions for optical communications and interconnects [1-4]. While there have been many advances in silicon optoelectronic device performance [5], [6], a room temperature electrically pumped, silicon laser is one of the last hurdles holding back large scale optical integration onto a silicon platform. Many approaches to light emission and amplification in silicon have been demonstrated including Raman lasers [7, 8] and amplifiers [9], nano-patterning [10], nanocrystalline-Si structures [11-13], and doping silicon rich oxides with rare earths [14]. All of these demonstrations, however, have been limited to optical pumping and/or operation at cryogenic temperatures. Alternatively III-V lasers may be coupled to silicon waveguides, so called hybrid integration. This may be done using flip-chip bonding [15, 16], self assembly [17] or vertical coupling of membrane type devices [18]. All of these approaches have the same deficit in that two devices of different dimensions and/or materials have to be aligned to sub-micron precision to enable efficient coupling.

Although the cost of a silicon photonic circuit may be small, aligning a pre-fabricated laser chip to a planar optical circuit is time consuming and expensive, and drives up the cost of the final assembled and packaged device. Conventionally, individual laser die are fabricated, diced, placed onto the silicon chip, and then aligned to the waveguide, in a time-consuming and costly process [19]. The laser die can either be actively aligned to the waveguide or mechanical stops can be used to passively align the laser to the silicon waveguide [15, 16]. The placement of individual lasers is expensive, time consuming, and not optimal for high volume manufacturing. A more promising approach has been presented by Hattori *et al.* [20] where they fabricate membrane III-V disk lasers vertically coupled to a passive silicon waveguide. This configuration eases the alignment tolerance to 2-dimensions but coupling is still limited due to the different materials used for the laser and the passive waveguide and the authors note that misalignment still causes discrepancies in their measured results.

Previously we demonstrated an optically pumped silicon evanescent laser [21]. The critical missing element was electrical pumping, so an external pump laser was needed. Here

we demonstrate an *electrically driven* hybrid AlGaInAs-silicon evanescent laser and architecture where the laser cavity is solely defined by a silicon waveguide, that is wafer bonded to a III-V layer. In addition, we demonstrate the capability of multiple electrically driven lasers operating simultaneously, all fabricated with a single bonding step.

The hybrid AlGaInAs-silicon evanescent laser is comprised of an offset multiple quantum well region bonded to silicon waveguides that are fabricated on a silicon-on-insulator wafer, [see Fig. 1(a)]. The optical mode of this laser overlaps both the III-V material and the silicon waveguide. The novelty of this structure is that the optical mode can obtain electrically pumped gain from the III-V region while being guided by the underlying silicon waveguide region. Due to the symmetry of the III-V region in the lateral direction, no alignment step is needed between the III-V wafer and the silicon waveguide prior to bonding. This allows one to produce electrically pumped laser sources on a silicon wafer that are completely self-aligned to ‘passive’ silicon waveguide sections, because both laser waveguide and passive waveguide sections are defined using the same etch step. This is a key advantage of this evanescent laser approach when compared to conventional discrete laser bonding approaches.

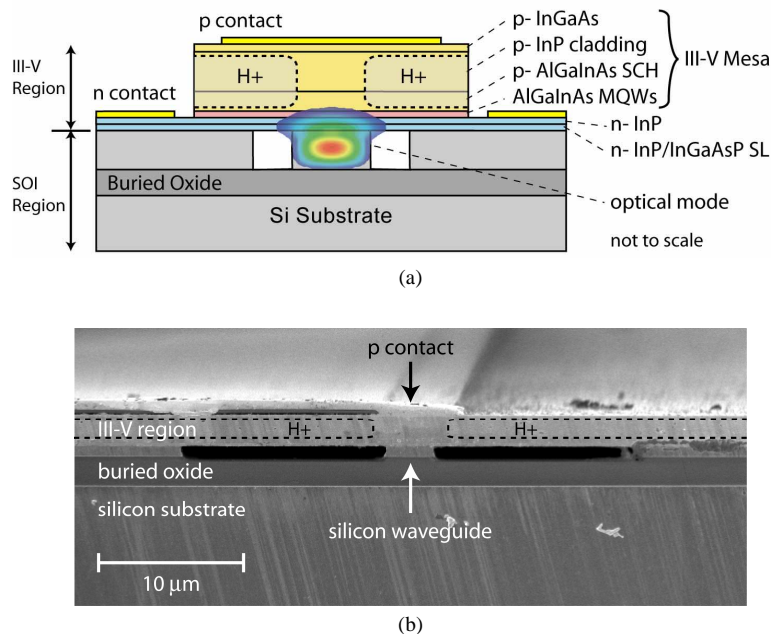


Fig. 1. (a). Schematic drawing of the hybrid laser structure with the optical mode superimposed (b) A scanning electron microscope cross sectional image of a fabricated hybrid AlGaInAs-silicon evanescent laser.

This approach can be performed at the wafer, partial wafer or die level, depending on the application, providing a solution for large scale optical integration onto a silicon platform. Figure 2 is a schematic of a transmitter module based on this evanescent approach showing how one could produce multiple, compact evanescent lasers of different wavelengths each self-aligned and coupled to silicon modulators and then all combined together with a silicon multiplexer. This entire transmit module could be fabricated on a single die with the multiple electrically pumped lasers fabricated with on single wafer bond. In addition the properties of the optical mode can be tailored from device to device by varying the silicon waveguide width enabling complex photonic integrated systems on a single chip.

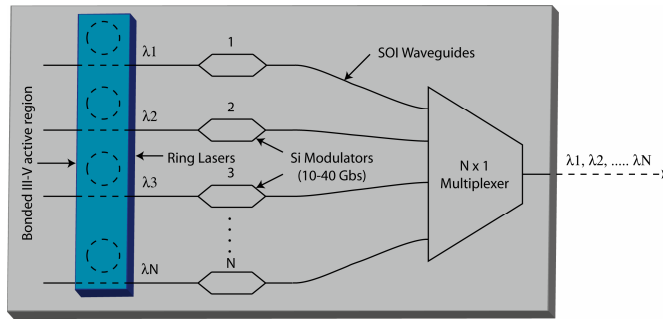


Fig. 2. Schematic drawing of an integrated silicon transmitter photonic chip showing multiple evanescent lasers fabricated on a silicon chip, all self aligned to silicon modulators and multiplexed to a single output.

2. Device structure and fabrication

The hybrid AlGaInAs-silicon evanescent laser is fabricated using an AlGaInAs quantum well epitaxial structure that is bonded to a low-loss silicon strip waveguide. The silicon strip waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate with a 2 μm thick buried oxide using standard projection photolithography and $\text{Cl}_2/\text{Ar}/\text{HBr}$ -based plasma reactive ion etching. The silicon waveguide was fabricated with a final height of 0.76 μm and width of 2.5 μm resulting in a mode that exists predominantly in the silicon waveguide. The calculated overlap of the optical mode with the silicon waveguides is 75 % while there is a 3 % overlap in the quantum wells.

The III-V epitaxial structure is grown on an InP substrate and is summarized in Table 1. The quantum well active layer is bounded by the separate confinement hetero-structure (SCH) and n-layers. The superlattice region is used to inhibit the propagation of defects from the bonded layer into the quantum well region [22]. This III-V structure is then transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding [23]. The low temperature process consists of a thorough solvent cleaning procedure, and surface treatments with buffered HF for silicon and NH_4OH for InP. The samples then undergo an additional surface treatment in an oxygen plasma reactive ion etch chamber. The samples surfaces are placed in physical contact at room temperature and subsequently annealed at 300 $^\circ\text{C}$ with an applied pressure of 1.5 MPa for 12 hours.

Table. 1. III-V Epitaxial growth layer structure

III-V Epitaxial growth layer structure			
Name	Composition	Doping Concentration	Thickness
P contact layer	P-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$1 \times 10^{19} \text{ cm}^{-3}$	0.1 μm
Cladding	P-type InP	$1 \times 10^{18} \text{ cm}^{-3}$	1.5 μm
SCH	P-type $\text{Al}_{0.131}\text{Ga}_{0.34}\text{In}_{0.528}\text{As}$, 1.3 μm	$1 \times 10^{17} \text{ cm}^{-3}$	0.25 μm
Quantum Wells	$\text{Al}_{0.089}\text{Ga}_{0.461}\text{In}_{0.45}\text{As}$, 1.3 μm (9x)	undoped	10 nm
	$\text{Al}_{0.055}\text{Ga}_{0.292}\text{In}_{0.653}\text{As}$, 1.5 μm (8x)	undoped	7 nm
N layer	N-type InP	$1 \times 10^{18} \text{ cm}^{-3}$	110 nm
Super Lattice	N-type $\text{In}_{0.85}\text{Ga}_{0.15}\text{As}_{0.327}\text{P}_{0.673}$ (2x)	$1 \times 10^{18} \text{ cm}^{-3}$	7.5 nm
	N-type InP (2x)	$1 \times 10^{18} \text{ cm}^{-3}$	7.5 nm
N bonding layer	N-type InP	$1 \times 10^{18} \text{ cm}^{-3}$	10 nm

After InP substrate removal with a mixture of HCl/H₂O, 75 μm wide mesas are formed using photolithography and by CH₄/H/Ar- based plasma reactive ion etching through the p-type layers and H₃PO₄/H₂O₂ selective wet etching of the quantum well layers to the n-type layers. Ni/AuGe/Ni/Au alloy n-contacts are deposited onto the exposed n-type InP layer 38 μm away from the center of the silicon waveguide. 4 μm wide Pd/Ti/Pd/Au p-contacts are then deposited on the center of the mesas. The p-region on the two sides of the mesa are implanted with protons (H⁺) which electrically insulates the p-type InP [24] resulting in a ~ 4 micron wide p-type current channel down through the non conductive p-type mesa, preventing lateral current spreading in the p-type mesa. The electrical current flows through the center of the mesa to achieve a large overlap with the optical mode. Ti/Au probe pads are deposited on the top of the mesa. The wafer is then diced and the waveguide facets are polished forming ~ 860 μm long laser cavity. A cross-sectional SEM (Scanning Electron Micrograph) image of the final fabricated hybrid laser is shown in Fig. 1(b).

3. Experiment and results

The laser is driven by applying a positive bias voltage to the top p contact. The laser output from one waveguide facet is collected by a lensed single mode fiber and then characterized by using a spectrum analyzer or photodetector while simultaneously imaging the laser mode exiting the opposite facet with an infrared camera. The entire silicon chip is mounted on a TEC controller which allows the operating temperature of the laser to be varied from 0 °C to 80 °C.

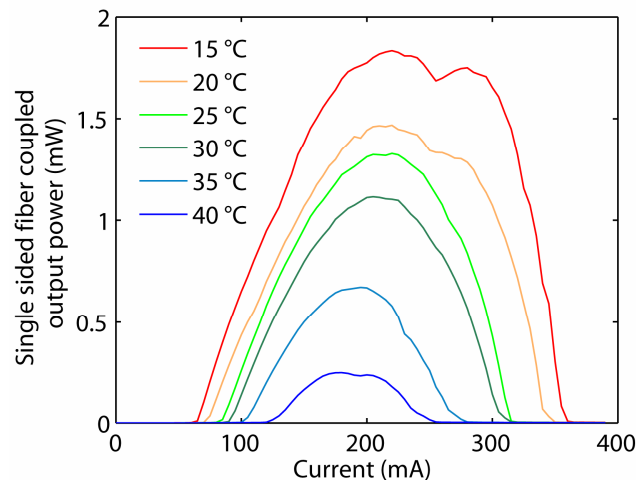


Fig. 3. The single sided fiber coupled laser output as a function of drive current for various operating temperatures.

Figure 3 shows the measured c.w. laser output power from one facet as a function of injected current for various operating temperatures ranging from 15 to 40 °C. As can be seen from Fig. 3, the laser threshold is 65 mA with a maximum output power of 1.8 mW at 15 °C. The laser has a 40 °C maximum lasing temperature with a characteristic temperature of 39 K. We have measured laser outputs from both facets and have found that they both have similar output powers and thresholds. Using the measured 6 dB coupling loss from waveguide to fiber, and the fact that light is only collected from one facet, we calculate a differential quantum efficiency of 12.7 %. A 15 cm⁻¹ modal loss was measured using the Hakki-Paoli method in the long wavelength regime [25]. The laser has a threshold voltage of 2 V and a series resistance of 7.5 ohms. These results are typical of other hybrid lasers tested.

The ~ 40 °C maximum laser temperature is currently limited by the poor heat extraction from the active region and unwanted heat generation caused by the high electrical series resistance of the thin n-layer [Fig 1(a)]. The temperature of the active region at laser turn off is found to be 80 °C and the thermal resistance of the device was estimated to be 40 °C/W by analyzing the measured L-I roll off characteristics and I-V characteristics [26].

The maximum operating temperature can be improved by minimizing the thermal impedance and electrical series resistance of the device. Reduction of the buried oxide thickness from 2 μm to 1 μm will bring the thermal resistance down to 28 °C/W. Heat sinking the top side of the laser would reduce the thermal resistance to 4 °C/W. A significant improvement in operating temperature would be achieved by reducing the n-layer electrical series resistance by narrowing the n-contact distance from the center of waveguide from 38 μm down to less than 10 μm .

Since the current device relies only on the 30 % silicon-to-air facet reflection, a significant reduction in threshold current would be achieved through the deposition of high reflection coatings onto the waveguide facets or using highly resonant ring cavity structures.

Additional improvements in lasing threshold and differential efficiency could be made by improving the injection efficiency of the device. The proton implant profile is designed to be effective through at least the upper half of the SCH in the p-type mesa, but has not been experimentally optimized. This implant profile could be optimized in order to reduce the current spreading in the SCH while maintaining the high conductivity on the n-type layers. In addition, the 4 μm wide current conduction channel created by the proton implant can be narrowed to reduce the effective current spreading.

All of these improvements stated above should increase the c.w. operating temperature to greater than 70 °C and lower the threshold current down to below 20 mA. This is important in order to achieve the 70 °C operating temperature and 0.5 mW fiber coupled power requirements of commercial transmitters [27].

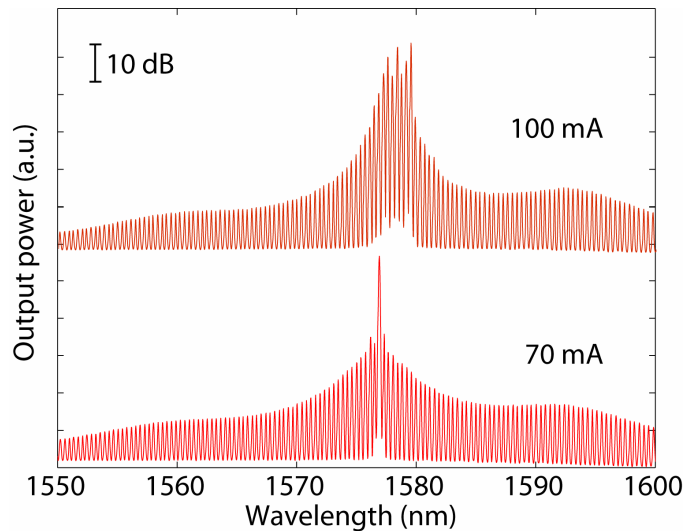


Fig. 4. The hybrid laser spectrum taken slightly above threshold (70 mA) and well above threshold (100 mA). The y-axis is on a logarithmic scale.

Figure 4 shows the measured multi-mode lasing spectrum of the silicon evanescent laser driven slightly above threshold at 70 mA, and well above threshold at 100 mA. The spectrum was measured with an HP 70952A optical spectrum analyzer with a resolution bandwidth of 0.08 nm. The lasing wavelength is around 1577 nm at 70 mA and is shifted to longer wavelengths at 100 mA due to device heating. The spectrum consists of the Fabry-Perot

response with a free spectral range of 0.38 nm corresponding to a modal group index of 3.68. Single wavelength operation and high side mode suppression should be achievable with distributed Bragg reflector mirrors or ring cavity configurations in conjunction with single mode rib waveguides.

To demonstrate the highly scalable nature of this hybrid laser approach, Fig. 5 shows the imaged output facet using an infrared camera of seven c.w. silicon evanescent lasers operating simultaneously from a single bonded silicon chip. The lasers were fabricated on an 8 mm wide silicon chip containing 36 lasers of varying waveguide widths from 1-3.5 μm . The number of evanescent laser devices running simultaneously is only limited by the electrical contact configuration of the current experimental set up (i.e. the number of electrical probes that could be placed simultaneously onto the test chip rather than the number of functional devices). Waveguides with larger widths showed multimode behavior in the lateral direction. Waveguides 2.5 μm wide and narrower lased at the fundamental mode. The yield of this process is reasonable with 26 of the 36 lasers on this chip lasing all with similar performance when tested individually. The output powers and current thresholds were all on the order of ~ 1 mW and ~ 75 mA respectively. The current yield is dominated by waveguide chipping and bond delamination during polishing of the bonded waveguide facets and is more prevalent in the narrower waveguides. This should be greatly improved by utilizing monolithic laser feedback schemes, such as ring resonator cavities or gratings in the silicon region, removing the device performance dependency on facet polishing.

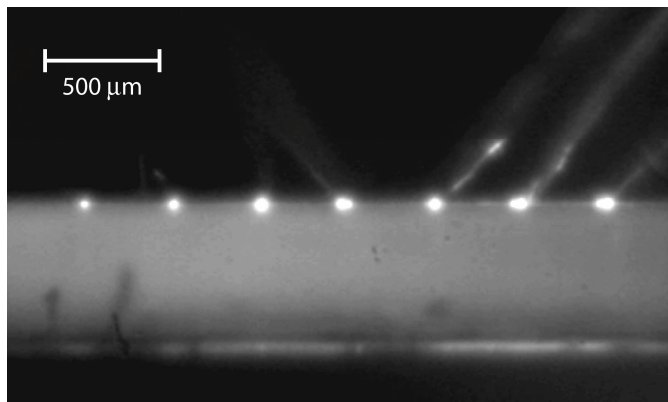


Fig. 5. An infrared image taken from one of the polished facets showing seven c.w. silicon evanescent lasers operating simultaneously.

4. Conclusion

The demonstration of an electrically pumped, room temperature laser that can be integrated onto a silicon platform is a significant step toward the realization of cost-effective, highly integrated silicon photonic devices. This approach combines the benefits of two different material systems to provide a unique solution to light generation for silicon photonics. We have demonstrated room temperature c.w. lasing with 65 mA threshold, ~ 1.8 mW output power and overall differential quantum efficiency of 12.7 %. We demonstrate an important advantage of this approach by fabricating multiple lasers onto one silicon die with a single, low temperature wafer bond to a patterned SOI photonic chip. More importantly these multiple lasers do not require any critical alignment of III-V material to the silicon waveguide potentially making this a large scale integratable solution. More compact, single mode lasers could be fabricated using any of the conventional integrated laser architectures, such as using integrated Bragg reflectors in the silicon waveguide or silicon ring resonator cavities placed below the III-V gain chip (see Fig. 2). Such integrated cavities will remove the need to polish the laser facets and could allow for hundreds of small laser cavities with much lower threshold currents to be fabricated onto a silicon chip. In addition by selectively altering the III-V

structure through processes such as quantum well intermixing [28] or nonplanar wafer bonding [29], this highly scaleable architecture can be extended to fabricate other active devices on silicon such as optical amplifiers, modulators and photo-detectors.

Acknowledgments

We thank N. Izhaky, A. Alduino, O. Raday, R. Gabay, D. Tran, K. Callegari, & G. Zeng for assistance in device fabrication & sample preparation; M. Rao, J. Klamkin, C. Wang, J. Raring, C. Ding, G. Cole, M. Sysak, C. Schaake, Y. Pei, B. Koch, E. Burmeister & M. Mehta for helpful discussions; Intel & Jag Shah & Wayne Chang through DARPA for supporting this research through contracts W911NF-05-1-0175 and W911NF-04-9-0001.