Low Temperature Wafer Bonding for III-V Si Photonic Integrated Circuits

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Abstract

VLSI Photonics is an important research direction that is driven by the need for increasing circuit complexity and chip functionality as well as lower cost photonic integrated circuits. Recently, lasers, amplifiers and photodetectors have been demonstrated using evanescent coupling from Si optical waveguides to III-V materials. A key problem is to develop a low temperature bonding process between Si and III-V materials that is CMOS compatible and scalable to 150 mm wafers.

In this paper, strong bonding between thermal SiO_2 grown on 100 mm diameter silicon-on-insulator (SOI) wafers and chemical vapor deposition (CVD) SiO_2 on InP wafers is demonstrated at low temperatures (≤ 300 °C). A key parameter for evanescently coupled photonic circuits is to keep the SiO_2 layer less than 100 nm thick for strong coupling between the Si waveguide and III-V gain and absorption layers. A thin deposited oxide is also preferred to minimize the surface roughness to less than 1 nm, eliminating the need for chemical mechanic polishing. Two approaches are employed to achieve a bubble-free bonding interface.

The first approach involves growing thin (< 50 nm) thermal SiO_2 to allow moisture easily penetrating through the oxide and react with the Si beneath, forming Si-O-Si covalent bond, and the byproduct H_2 can diffuse along the interface by patterning the SOI wafer with channels. The bubble density is proportional to the oxide thickness due to the slower diffusion rate of H_2O over H_2 molecules. The bubble density for this method is also dependent on channel density which in turn may be influenced by the silicon device layout. The bubble density is measured under a microscope after selectively removing the InP substrate.

Treating the SiO_2 surfaces with dilute HF (< 0.5%) aqueous solution is shown to be another valid approach to obtain high quality bonding. A one minute HF dip immediately prior to contact at room temperature results in the breaking of Si-O-Si rings and the formation of large fluorinated silicon oxide (SiOF) rings. The highly porous structure facilitates the diffusion of impurities and enhances moisture absorptivity, effectively reducing the out-gassing rate. The bonding strength dependence on CVD SiO_2 quality is also studied by comparing conventional PECVD SiO_2 deposited at 250 °C and high-density inductively coupled plasma (ICP) PECVD SiO_2 at 100 °C with the same thickness. Higher refractive index and smoother surface are found in ICP PECVD SiO_2, indicating a superior quality, which subsequently resulted in a stronger bonding interface energy.

All bonding experiments were performed in an N_2 gas ambient for 3 hours using a Karl Suss wafer bonder.

We report on the impact of scaling the bonding process to 100 mm wafers via these two wafer bonding processes on hybrid silicon evanescent laser performance.

Keywords: photonic integrated circuits, wafer bonding, silicon.