150 mm InP-to-Silicon Direct Wafer Bonding for Silicon Photonic Integrated Circuits

(1)Di Liang, Alexander W. Fang, John E. Bowers
(2)Douglas C. Oakley, Antonio Napoleone, David C. Chapman, Chang-Lee Chen, Paul W. Juodawlkis
(3)Omri Raday

(1)Department of Electrical and Computer Engineering, University of California, Santa Barbara, California, 93106, USA
(2)Lincoln Laboratory, Massachusetts Institute of Technology, 244 Wood Street, Lexington, Massachusetts, 02420, USA
(3)Intel Corporation, S.B.I. Park Har Hotzvim, Jerusalem 91031, Israel

Recently attention has been concentrated on silicon photonic integrated circuits (PICs) as a potential solution to solve the bottleneck of power consumption and interconnect bandwidth in future microprocessors. In attempting to integrate III-V compound semiconductors on silicon substrates, low-temperature wafer bonding has much lower threading dislocation density than heteroepitaxy. High-performance lasers, amplifiers, photodetectors and modulators have been demonstrated lately on a hybrid silicon evanescent platform using a low-temperature direct wafer bonding process[1]. In order to benefit from the mature CMOS technology and reach a commercialization phase, a CMOS-compatible, highly-scalable and low-cost wafer bonding technique is required.

We report in this paper a record-large 150 mm in diameter, InP-based (001) epitaxial wafer with multiple quantum-well (MQW) laser structure has been successfully wafer-bonded to a prepatterned silicon-on-insulator (SOI) substrate (001) intimately with no interfacial material (e.g., deposited oxide or spin-on polymer). As shown in Fig. 1, over 95% of the III-V epitaxial layer is transferred with only negligible loss around the wafer edge primarily due to a small III-V wafer horizontal slide during room-temperature mating. A highly efficient vertical outgassing channel (VOC) design[2] is employed to allow gas byproducts (H_2O and H_2) from the intrinsic polymerization reactions plus trapped air to be absorbed by the buried oxide (BOX) layer of the SOI substrate. Benefiting from the optimized VOC design, an interfacial void-free bonding is therefore obtained across the entire 150 mm wafer area. The bright spots highlighted in the Fig. 1 are periodically distributed etch calibration patterns on the SOI wafer. Due to lack of the mechanical support, thin III-V layer collapses as shown in the Fig. 1 inset after the InP substrate removal. A ~5 mm in diameter bubble at the center, visible in infrared imaging prior to anneal as well, is due to either a epitaxial defect or a surface particle.

The low-temperature bonding process starts from rigorous wafer surface clean in H_2SO_4:H_2O (3:1) and NH_4OH (39%) solutions for SOI and InP wafers, respectively. Upon native oxide removal in the HF solution, the SOI wafer experiences an O_2 plasma surface activation in a commercial EVG 801 LowTemp Plasma Activation System for 30 seconds, followed by the same treatment for the InP wafer as well. Wafers are then cleaned again in a modified microcleanroom[3] setup with deionized water spray rinse which also serves as the final surface activation step to terminate the surface with –OH groups. After a 300 °C, 15-hour anneal in an oven, the 635 μm thick InP substrate is selectively removed in a HCl:H_2O (3:1) solution, resulting in only ~2 μm thick epitaxial layer on the SOI substrate. A crack-opening measurement indicates that the bonding surface energy exceeds the fracture energy of the bulk InP material.

A high-resolution X-ray diffraction (XRD) rocking curve measurement was conducted on the as-grown III-V wafer and then the transferred III-V layer to further study the quality of epitaxial transfer. This in-plane laser structure contains eight periods of strained (1% compression, λ_{avg}=1.53 μm) InGaAsP (8 nm) offset MQW plus a 1.5 μm thick InP cladding. Fig. 2 shows the direct comparison of the Omega-2 Theta scans at wafer center. The InP main peak and satellites are well maintained, indicating the excellent signature transfer of the MQW active region. A ~90 μm wafer warp is measured from an Omega scan (data not shown), which is comparable to that of commercial 150 mm SOI wafers.

In conclusion, we have demonstrated a record-large, high-quality InP-to-silicon direct wafer bonding. 150 mm in diameter InP-based laser epitaxial layers were successfully transferred to the SOI substrate with well-preserved MQW structure and small wafer warp. >95% bonding yield, high surface energy, void-free interface exhibits the promising large-volume, CMOS-based production perspective for low-cost silicon PICs.

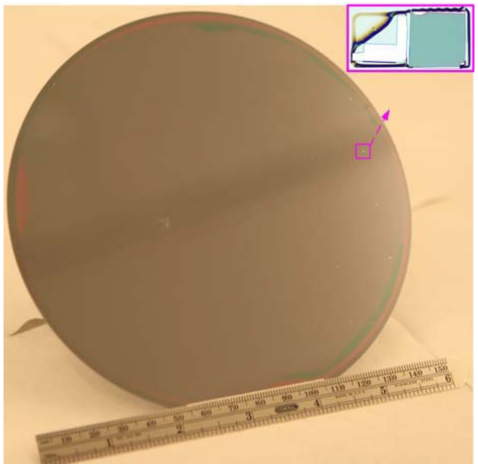

Fig. 1. Image of 150 mm InP-based MQW epitaxial layer transferred to the SOI substrate. Inset: an etch calibration pattern in the SOI substrate causing III-V collapsing.

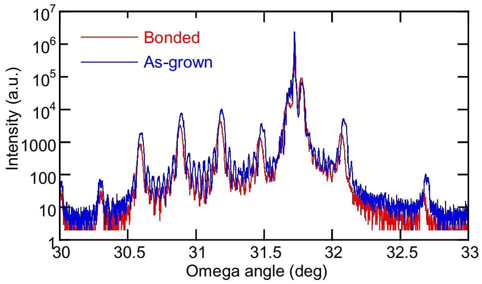

Fig. 2. XRD rocking curve measurement of 150 mm as-grown (top) and transferred (bottom) InP epitaxial wafer.

[1] H. Park, A. W. Fang, D. Liang, Y.-H. Kuo, H.-H. Chang, B. R.Koch, H.-W. Chen, M. N. Sysak, R. Jones and J. E. Bowers, *Adv. Opt. Technol.*, in press, (2008).

[2] D. Liang and J. E. Bowers, manuscript accepted by *J. Vac. Sci. Technol. B*, (2008).

[3] R. Stengl, K.-Y. Ahn, and U. Gösele, *Jpn. J. App. Phy.* **27**, L2364 (1988).