An electrically pumped hybrid silicon evanescent amplifier

Hyundai Park, Alexander W. Fang, and John E. Bowers
Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA 93106
hdpark@engr.ucsb.edu
Richard Jones
Intel Corporation, 2200 Mission College Boulevard, SC12-326, Santa Clara, CA 95054
Oded Cohen
Intel Corporation, SBI Park Har Hotzvim, Jerusalem, 91031, Israel

Abstract: A hybrid silicon evanescent amplifier utilizing a wafer bonded structure of a silicon waveguide and AlGaInAs quantum wells is demonstrated. Maximum chip gain obtained is 13 dB with a 3 dB output saturation power of 11dBm.

OCIS codes: (250.5980) Semiconductor optical amplifiers; (250.5300) Photonic integrated circuits

1. Introduction

Recent progress in silicon photonics has been motivated by mature silicon processing technology for photonic integrated circuits with low cost and high functionality. Optical amplifiers are key components in realizing high levels of photonic integration as they compensate for optical losses from individual photonic elements. An optically pumped Raman amplifier has been demonstrated [1], but an electrically pumped optical amplifier on silicon is yet to be realized, primarily due to the indirect nature of the silicon bandgap. A die of optical amplifiers can be attached to a SOI wafer, but their gain and noise figure are limited by reflections from interfaces and coupling loss to the silicon waveguide. We address this problem by wafer bonding a high gain layer to an SOI waveguide, such that the light into and out of the chip remains predominantly in the silicon waveguide layer. The amplifier can be used as a postamplifier integrated with silicon evanescent lasers [2] or used as an integrated preamplifier with waveguide SiGe photodetectors. The electrically pumped hybrid silicon evanescent amplifier demonstrated here has a maximum chip gain of 13 dB with a 3 dB output saturation power of 11 dBm.

2. Device Structure and Fabrication

The silicon evanescent amplifier is a hybrid structure that consists of an offset multiple quantum well region bonded to a silicon waveguide fabricated on a silicon-on-insulator wafer. Details of the structure are shown in Fig.1a. With this architecture, the optical mode can obtain electrically pumped gain from the III-V region while being guided by the underlying silicon waveguide region.

The silicon strip waveguide is formed on the (100) surface of an undoped silicon-on-insulator (SOI) substrate with a 2 μm thick buried oxide using standard photolithography and Cl_2/Ar/HBr-based plasma reactive ion etching. The silicon waveguide was fabricated with a final height of 0.76 μm and width of 2 μm resulting in a mode that exists predominantly in the silicon waveguide. The calculated overlap of the optical mode with the silicon waveguide is 73.8 % while there is a 3.4 % overlap in the AlGaInAs quantum wells.

The III-V epitaxial structure is grown on an InP substrate and is summarized in Table 1. The quantum well active layer is bounded by a p-type AlGaInAs SCH layer and n-type InP and InP/InGaAsP superlattice (SL) layers to enable current injection. The superlattice region is used to inhibit the propagation of defects from the bonded layer into the quantum well region [3]. This III-V structure is then transferred to the patterned silicon wafer through low temperature oxygen plasma assisted wafer bonding [4]. The low temperature process consists of a thorough solvent cleaning procedure, and surface treatments with buffered HF for silicon and NH_4OH for InP. After surface treatment with oxygen plasma in a reactive ion etch chamber, the samples are placed in physical contact at room temperature and subsequently annealed at 300 ºC with an applied pressure of 1.5 MPa for 12 hours.

After InP substrate removal with a mixture of HCl/H_2O, 75 μm wide mesas are formed using photolithography and by CH_4/H/Ar-

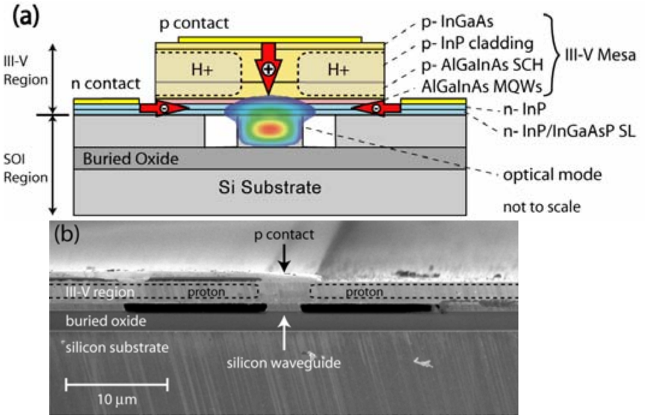

Fig. 1. (a) Device structure (b) SEM image of fabricated device.

Name	Composition	Doping	Thickness
P contat layer	$In_{0.53}Ga_{0.47}As$	P-type, 1x10^{19} cm^{-3}	0.1 μm
Cladding	InP	P-type, 1x10^{18} cm^{-3}	1.5 μm
SCH	1.3Q-$Al_{0.131}Ga_{0.34}In_{0.528}As$	P-type, 1x10^{17} cm^{-3}	0.25 μm
Quantum wells	1.3Q-$Al_{0.289}Ga_{0.461}In_{0.45}As$ (9x)	undoped	10 nm
	1.5Q-$Al_{0.055}Ga_{0.292}In_{0.653}As$ (8x)	undoped	7 nm
Spacer	InP	N-type, 1x10^{18} cm^{-3}	110 nm
Super lattice	1.1Q-$In_{0.85}Ga_{0.15}As_{0.327}P$ (2x)	N-type, 1x10^{18} cm^{-3}	7.5 nm
	InP (2x)	N-type, 1x10^{18} cm^{-3}	7.5 nm
Bonding layer	InP	N-type, 1x10^{18} cm^{-3}	10 nm

Table 1. III-V epitaxial layer structure.

based plasma reactive ion etching through the p-type layers. H_3PO_4/H_2O_2 selective wet etching is used to remove the quantum well layers above the n-type contact layer. Ni/AuGe/Ni/Au alloy n-contacts are deposited onto the exposed n-type InP layer 38 µm away from the center of the silicon waveguide. 4 µm wide Pd/Ti/Pd/Au p-contacts are then deposited on the center of the mesas. The p-region on the two sides of the mesa are implanted with protons (H+) which electrically insulates the p-type InP, the implant limits the conducting region of the structure to a ~ 4 micron wide p-type current channel down through the p-type mesa, thus preventing lateral current spreading. The electrical current flows through the center of the mesa to achieve a large overlap with the optical mode. Ti/Au probe pads are deposited on the top of the mesa. To minimize the optical feedback due to facet reflection, the sample is diced in a manner that orients the waveguides at an angle of 7 ° with the normal to the facet plane. After the facets are polished, an antireflection coating of Ta_2O_5 is applied to each facet. The device length after dicing and polishing process is ~ 1.36 mm. A cross-sectional SEM (Scanning Electron Micrograph) image of the final fabricated hybrid amplifier is shown in Fig. 1b.

3. Experiment and Results

The device, mounted on a temperature controlled stage set to 15 °C, is driven by applying a positive voltage at the p-contact. The device gain is measured by launching and collecting the signal through lensed-fibers at both the input and output facets. The angle between the fiber and the normal to the facet is ~25° to maximize the coupling of output light from the 7° angled waveguide. Coupling efficiency from the device to the fiber is measured to be -5 dB by measuring insertion loss at long wavelengths. Figure 2 shows the measured small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using 5 dB coupling loss. The maximum fiber-to-fiber gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. The inset of the figure represents the net modal gain, $\Gamma g-\alpha$, where Γ is the QW confinement factor, g is the material gain, and α is the waveguide loss. The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current density at the active region, $g=g_0 \log(J/J_{tr})$, where g_0 is 972 cm^{-1} and J_{tr} is 544 A/cm^2. The injection efficiency and waveguide loss (α) are measured to be 70 % and 15 cm^{-1} respectively [2]. Γ is assumed to be 3.4 % from the calculation of the optical mode profile. At lower current densities, the gain increases logarithmically while at higher current densities it saturates due to device heating caused by the series resistance (7.5 Ω) and thermal impedance (40 K/W). It is possible to circumvent some of these heating effects by reducing the distance between the n-contact and the active region to 10 µm, and decreasing the buried oxide thickness to 1 µm [2]. With these improvements, we expect to increase the chip gain to more than 20 dB. Figure 3 shows the gain spectra with different bias currents. The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA.

The 3 dB output saturation power from the chip is measured to be 11 dBm as shown in Fig. 4a. The 3 dB output saturation power can be written as, [5]

$$P_{0,SAT} = \frac{G_0 \log 2}{G_0 - 2} \cdot \frac{wd}{\Gamma} \cdot \frac{h\upsilon}{(dg/dN)\tau}$$

where G_0 is the unsaturated chip gain, w is the optical mode width at the quantum well region, d is the total thickness of the active material, hυ is the photon energy, dg/dN is the differential gain, and τ is the carrier lifetime. Figure 4b shows the calculated 3 dB output saturation power with different confinement factors (Γ) and optical mode widths (w). The measured value agrees well with theoretical calculations computed with a mode width of 2 µm. The evanescent coupling scheme of the device structure typically provides 2 % to 3 % of QW confinement factor resulting in higher output saturation powers than conventional III-V amplifiers with centered quantum wells whose typical confinement factor is around 5 % to 15 %. Moreover, the tapered or flared waveguide structure demonstrated with III-V amplifiers [6] can also be applied to this device by manipulating the silicon waveguide width without changing the III-V region for better output saturation output power.

The noise figure (NF) is measured from the spontaneous emission density at the signal wavelength [7] as shown in Fig. 5. The measured NF varies between 13 dB and 10 dB depending on the current level. The NF usually decreases at higher current levels

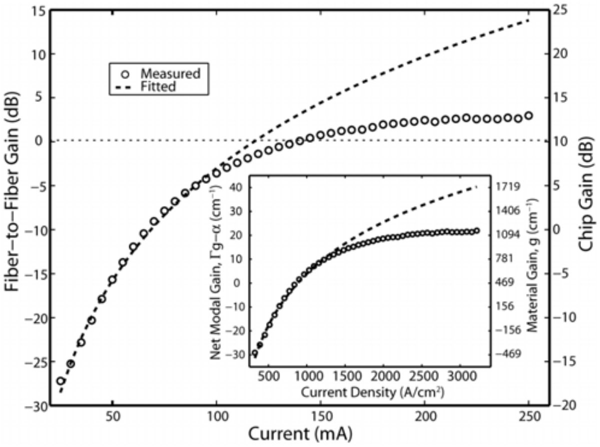

Fig. 2. Amplifier gain vs current (inset) Net modal gain extracted from the chip gain vs current density at 1575 nm.

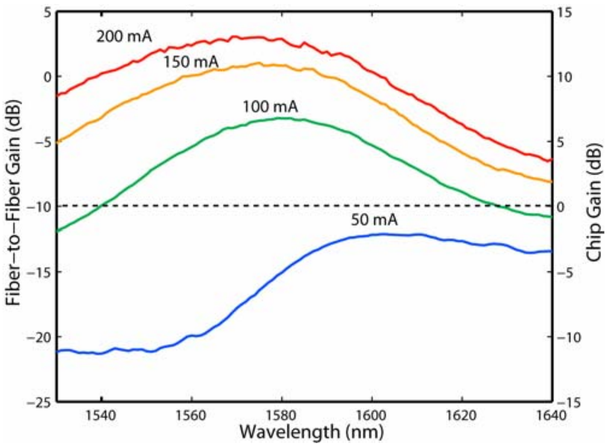

Fig. 3. Amplifier gain vs wavelength with different current levels.

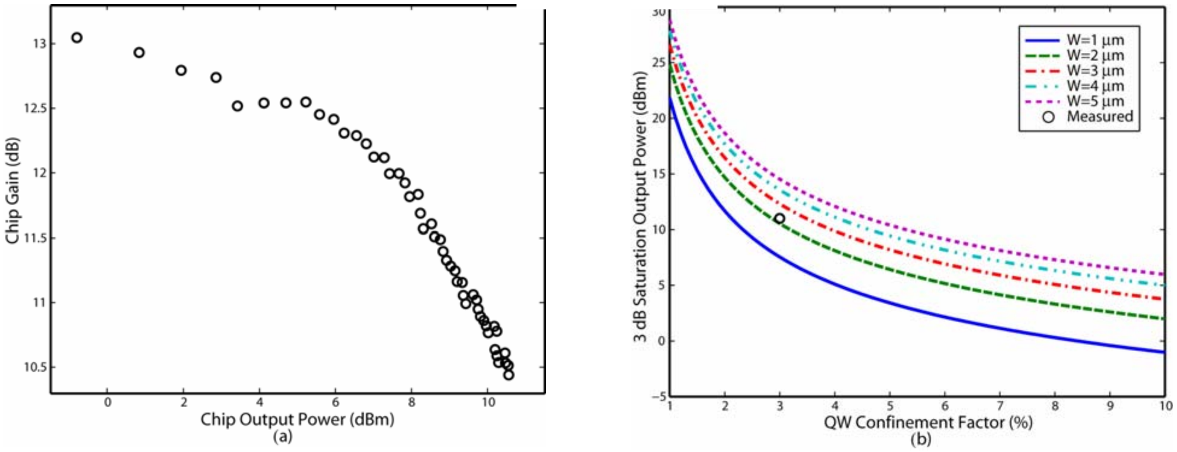

Fig. 4. (a) Amplifier gain vs output power at 1575 nm (b) 3dB saturation output power vs confinement factor and different optical mode width.

because of a larger spontaneous-emission factor [5]. The internal NF of the device can be between 8 dB and 5 dB considering 5 dB coupling loss. This is a typical value for conventional semiconductor optical amplifiers. The inset of Fig. 5 shows the amplified spectra with ASE noise spectra with different current levels. The spectral ripple from the residual facet reflectivity is ~0.2 dB at 13 dB chip gain which corresponds to a facet reflectivity of 5x10^{-4}.

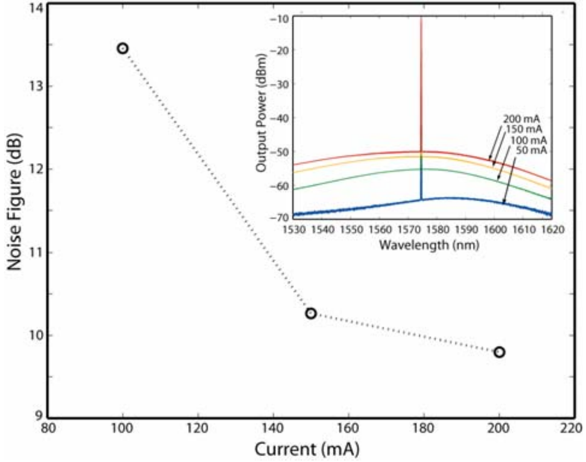

Fig. 5. Noise figure with amplified spectra (inset) for different current levels.

5. Conclusion

We have demonstrated an electrically pumped hybrid silicon evanescent amplifier incorporating AlGaInAs quantum wells with a silicon waveguide. The amplifier combines efficient optical gain from III-V materials with silicon waveguides that control the characteristics of the optical mode. The demonstrated chip gain is 13 dB which can be improved beyond 20 dB with optimization of thermal and electrical properties of the device. The 3 dB output saturation of the device is 11 dBm. The evanescent coupling scheme uses offset quantum wells, which provide lower quantum well confinement factor leading to higher output saturation powers than a conventional semiconductor optical amplifier. This amplifier design utilizes a silicon evanescent platform that allows for efficient integration with silicon evanescent lasers, photodetectors and mode converters.

6. References

[1] R. Jones, H. Rong, A. Liu, A. W. Fang, M. J. Paniccia, D. Hak, and O. Cohen, "Net continuous wave optical gain in a low loss silicon-on-insulator waveguide by stimulated Raman scattering," *Opt. Express* **13**, 519-525 (2005).

[2] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J. E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," *Opt. Express* **14**, 9203-9210 (2006).

[3] A. Karim, K. A. Black, P. Abraham, D. Lofgreen, Y. J. Chiu, J. Piprek, and J. E. Bowers , "Super lattice barrier 1528-nm vertical-cavity laser with 85 ºC continuous-wave operation," *IEEE Photon. Technol. Lett.* **12**, 1438-1440 (2000).

[4] D. Pasquariello, and K. Hjort, "Plasma-Assisted InP-to-Si Low Temperature Wafer Bonding," *IEEE J. Sel. Topics Quantum Electron*. **8**, 118-131 (2002).

[5] G. P. Agrawal, *Fiber-Optic Communication Systems*, Wiley, New York, 2002.

[6] A. Tauke-Pedretti, M. Dummer, J. S. Barton, M. N. Sysak, J. W. Raring, and L.A. Coldren, "High Saturation Power and High Gain Integrated Photoreceivers," *IEEE Photon. Technol. Lett.* **17**, 2167-2169 (2005).

[7] D. M. Baney, P. Gallion, and R. S. Tucker, "Theory and measurement techniques for the noise figure of optical amplifiers," *Opt. Fiber Technol.* **6**, 122 (2000).

Acknowledgement

This work was supported by DARPA through contracts W911NF-05-1-0175 and W911NF-04-9-0001, and by Intel. The authors thank Jag Shah and Wayne Chang for useful discussions.