A Hybrid AlGaInAs–Silicon Evanescent Amplifier

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***Abstract*—We report a hybrid AlGaInAs–silicon evanescent amplifier incorporating a silicon waveguide with a III–V gain medium. The optical mode of the hybrid amplifier is mostly confined to the silicon waveguide and evanescently coupled to the AlGaInAs quantum-well (QW) region where optical gain is provided by electrical current injection. These two different material systems are bonded by low-temperature oxygen plasma assisted wafer bonding at 300 °C. The fabricated device shows 13 dB of maximum chip gain with 11 dBm of output saturation power. Evanescent coupling allows a lower active region confinement factor to provide a higher saturation output power than amplifiers with centered QWs, which is important for applications that require linear amplification.**

***Index Terms*—Semiconductor optical amplifiers, silicon-on-insulator (SOI) technology.**

I. Introduction

PHOTONIC integration has progressed greatly in realizing diverse functionality in a small form factor for optical interconnects as well as long-haul communication systems. Silicon photonics is a promising platform to fabricate dense photonic integrated circuits on a large silicon wafer using highly accurate silicon processing technology. However, the optical amplifier, an essential component for the compensation of loss in a photonic system, has only been realized in silicon through optical pumping using the Raman effect [1]. As a result, integration of electrically pumped optical amplifiers on silicon has required coupling individual III–V amplifier die to the silicon passive devices [2]. The limited alignment accuracy of the die-attach method results in reduced amplifier performance caused by large coupling loss, and interface reflection. Recently, we demonstrated an electrically pumped silicon evanescent laser utilizing a wafer bonded structure of the silicon waveguide and III–V quantum wells (QWs) [3], and here we extend this approach to on-chip optical amplification. This approach can provide a small coupling loss and low reflection between the active and passive devices since the hybrid mode lies predominantly in the silicon region, and the silicon waveguides for both passive and active sections are defined in a single etch process. Here we demonstrate a silicon evanescent amplifier utilizing this approach, with a maximum chip gain of 13 dB and a 3-dB output saturation power of 11 dBm.

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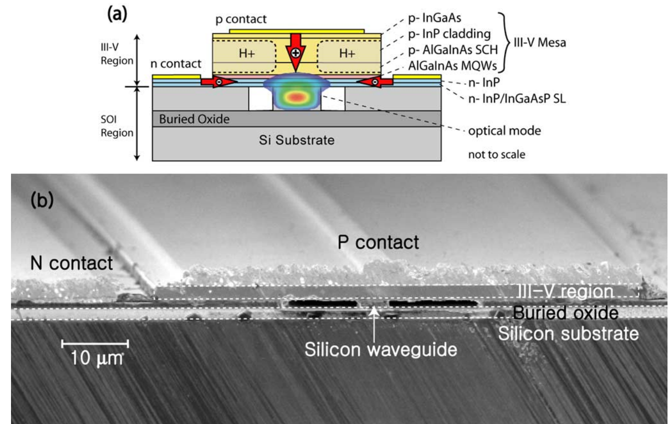

Fig. 1. (a) Device structure cross section. (b) SEM image.

TABLE I
III–V Epitaxial Layer Structure

Name	Composition	Doping	Thickness
P contat layer	$In_{0.53}Ga_{0.47}As$	P-type, $1x10^{19}$ cm^{-3}	0.1 µm
Cladding	InP	P-type, $1x10^{18}$ cm^{-3}	1.5 µm
SCH	1.3Q-$Al_{0.131}Ga_{0.34}In_{0.528}As$	P-type, $1x10^{17}$ cm^{-3}	0.25 µm
Quantum wells	1.3Q-$Al_{0.289}Ga_{0.461}In_{0.45}As$ (9x)	undoped	10 nm
(PL: 1545 nm)	1.7Q-$Al_{0.055}Ga_{0.292}In_{0.653}As$ (8x)	undoped	7 nm
Spacer	InP	N-type, $1x10^{18}$ cm^{-3}	110 nm
Super lattice	1.1Q-$In_{0.85}Ga_{0.15}As_{0.327}P$ (2x)	N-type, $1x10^{18}$ cm^{-3}	7.5 nm
	InP (2x)	N-type, $1x10^{18}$ cm^{-3}	7.5 nm
Bonding layer	InP	N-type, $1x10^{18}$ cm^{-3}	10 nm

II. Device Structure and Fabrication

The silicon evanescent amplifier is comprised of an offset multiple QW region bonded to a silicon waveguide fabricated on a silicon-on-insulator (SOI) wafer, as shown in Fig. 1(a). With this hybrid structure, the optical mode can obtain electrically pumped gain from the III–V region while being guided by the underlying silicon waveguide region.

The silicon strip waveguide is formed on the (100) surface of an undoped SOI substrate with a 2-μm-thick buried oxide using Cl_2–Ar–HBr-based plasma reactive ion etching. The silicon waveguide was fabricated with a final height of 0.76 μm and a width of 2 μm, resulting in a mode that exists predominantly in the silicon waveguide. The calculated overlap of the optical mode with the silicon waveguide is 74% while there is a 3.4% overlap with the QWs.

The III–V epitaxial structure is grown on an InP substrate and is summarized in Table I. The eight QWs are compressively strained (0.85%) while the barriers are tensile strained (−0.55%). The QW active region is bounded by p-AlGaInAs SCH layer and n-type layers. A superlattice region is used at

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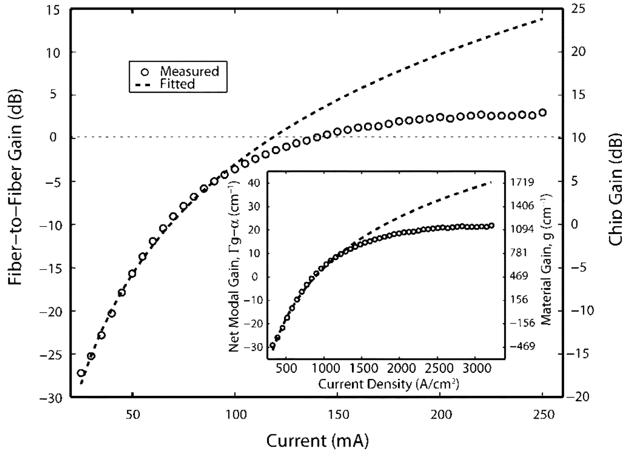

Fig. 2. Amplifier gain versus current. (inset) Net modal gain extracted from the chip gain versus current density at 1575 nm.

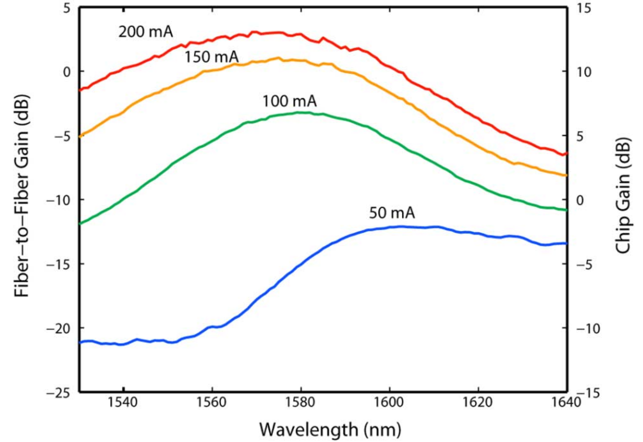

Fig. 3. Amplifier gain versus wavelength with different current levels.

the bonding interface to inhibit the propagation of defects from the bonded layer into the QW region [4]. This III–V structure is then transferred to the patterned silicon wafer through low-temperature oxygen plasma assisted wafer bonding with 300 °C annealing temperature [5]. The specific bonding process is described in [3].

After removal of the InP substrate with a mixture of HCl–H_2O, 75-μm-wide mesas are formed by dry-etching the p-type layers using a CH_4–H–Ar-based plasma reactive ion etch. Subsequent wet-etching of the QW layers to the n-type layers is performed using H_3PO_4–H_2O_2. Ni–AuGe–Ni–Au alloy contacts are deposited onto the exposed n-type InP layer 38 μm away from the center of the silicon waveguide. A 4-μm-wide Pd–Ti–Pd–Au p-contacts are then deposited on the center of the mesas. Proton (H+) implantation on the two sides of the p-type mesa creates a 4-μm-wide current channel and prevents lateral current spreading, ensuring a large overlap between the carriers and the optical mode. Ti–Au probe pads are then deposited on the top of the mesa. To minimize the optical feedback due to facet reflection, the sample is diced orienting the waveguides at an angle of 7° with the normal to the facet plane. After the facets are polished, an antireflection (AR) coating of Ta_2O_5 ($\sim$5%) is applied to each facet. The final device length is $\sim$1.36 mm. A cross-sectional scanning electron microscope (SEM) image of the final fabricated hybrid amplifier is shown in Fig. 1(b).

III. Experiment and Results

The device is mounted on a temperature-controlled stage set to 15 °C and is driven by applying a positive voltage at the p-contact. The device gain is measured by launching and collecting the signal through lensed-fibers at both the input and output facets. The input polarization is controlled by a polarization controller. The angle between the fiber and the normal to the facet is $\sim$25° to maximize the coupling of output light from the 7° angled waveguide. Coupling efficiency from the device to the fiber is measured to be -5 dB from the measured insertion loss of 20 dB at long wavelengths. Fig. 2 shows the measured TE small-signal fiber-to-fiber gain and, on the second y-axis, the estimated chip gain using 5-dB coupling loss. The maximum fiber-to-fiber TE gain is 3 dB corresponding to a chip gain of 13 dB at 1575 nm. The inset of the figure represents the net modal gain $\Gamma g - \alpha$, where Γ is the QW confinement factor, g is the material gain, and α is the waveguide loss. The dotted line of the inset is a data fit using the logarithmic function between the material gain and the current density at the active region $g = g_0 \log(J/J_{\mathrm{tr}})$, where g_0 is 972 cm^{-1} and J_{tr} is 544 A/cm^2. The injection efficiency and waveguide loss (α) is measured to be 70% and 15 cm^{-1}, respectively [3]. Γ is assumed to be 3.4% from the calculation of the optical mode profile. At lower current densities, the gain increases logarithmically, while at higher current densities, it saturates due to device heating caused by the series resistance (7.5 Ω) and thermal impedance (40 K/W). These heating effects can be circumvented by reducing the distance between the n-contact and the active region to $\sim$10 μm, and decreasing the buried oxide thickness to 1 μm [3]. With these improvements, it should be possible to increase the chip gain to more than 20 dB.

Fig. 3 shows the gain spectra with different bias currents measured by changing an input wavelength of a tunable laser with 1-nm step. The maximum gain occurs at 1575 nm with a spectral full-width at half-maximum of 62 nm at 200 mA for TE polarization. The measured TM gain is typically lower than TE gain because of the compressively strained QWs. For example, TM gain is around 1 dB when TE gain is 10 dB. Fig. 4(a) shows gain saturation characteristics of the device. Output power on the x-axis is rescaled from the measured value considering 5-dB coupling loss. The 3-dB output saturation power from the chip is measured to be 11 dBm. The 3-dB output saturation power, $P_{0,\mathrm{SAT}}$, can be theoretically written as [6]

$$P_{0,\mathrm{SAT}} = \frac{G_0 \log 2}{G_0 - 2} \cdot \frac{wd}{\Gamma} \cdot \frac{hv}{(dg/dN)\tau}$$

where G_0 is the unsaturated chip gain, w is the optical mode width at the QW region, d is the total thickness of the active material, hv is the photon energy, dg/dN is the differential gain, and τ is the carrier lifetime. Fig. 4(b) shows the calculated $P_{0,\mathrm{SAT}}$ with different confinement factors (Γ) and optical mode widths (w) at a unsaturated chip gain (G_0) of 13 dB. The measured value agrees well with theoretical calculations computed with a mode width of 2 μm. The evanescent coupling scheme of the device structure typically provides 2% to 3% of QW confinement factor resulting in higher output saturation powers than amplifiers with centered QWs whose typical confinement factor is around 5% to 15%. Further improvement of the saturated

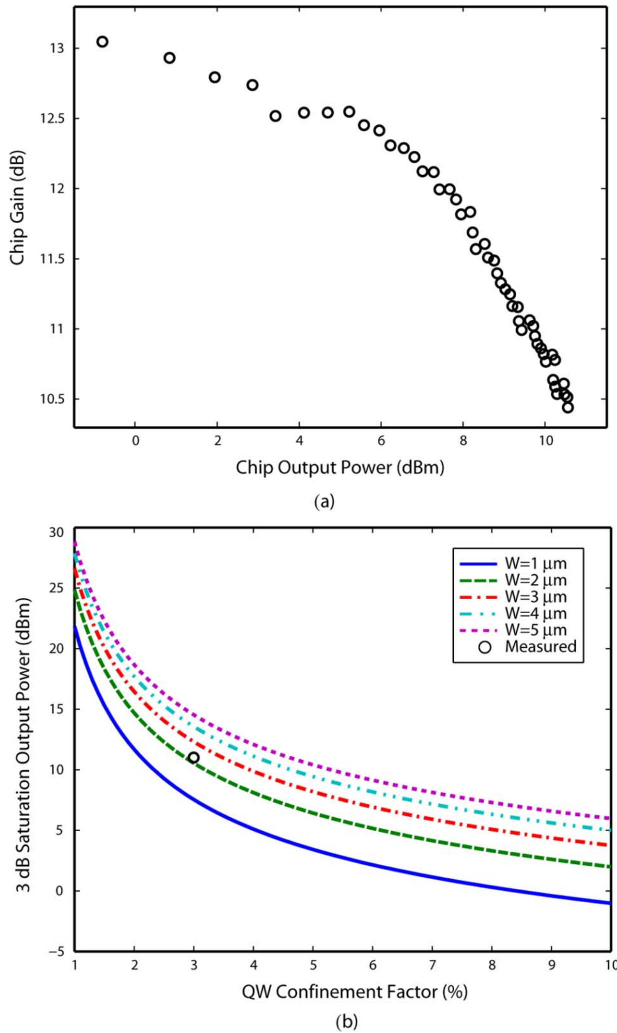

Fig. 4. (a) Amplifier gain versus output power at 1575 nm. (b) 3-dB saturation output power versus confinement factor and different optical mode width.

output power may be obtained by using the tapered or flared waveguide structure demonstrated with III–V amplifiers [7] by manipulating the silicon waveguide width without changing the III–V region.

The noise figure (NF) is measured from the spontaneous emission density at the signal wavelength [8], as shown in Fig. 5. The measured NF varies between 13 and 10 dB depending on the current level. The NF usually decreases at higher current levels because of a larger spontaneous-emission factor [6]. The internal NF of the device can be between 8 and 5 dB considering 5-dB coupling loss. The inset of Fig. 5 shows the amplified spectra with amplified spontaneous emission noise spectra with different current levels. The residual reflectivity from a 7° angled and AR-coated facet is estimated to be 5×10^{-4} by measuring a spectral ripple of 0.2 dB at 13-dB chip gain.

IV. Conclusion

We have demonstrated an electrically pumped hybrid silicon evanescent amplifier incorporating AlGaInAs QWs with a silicon waveguide. The amplifier combines efficient optical gain

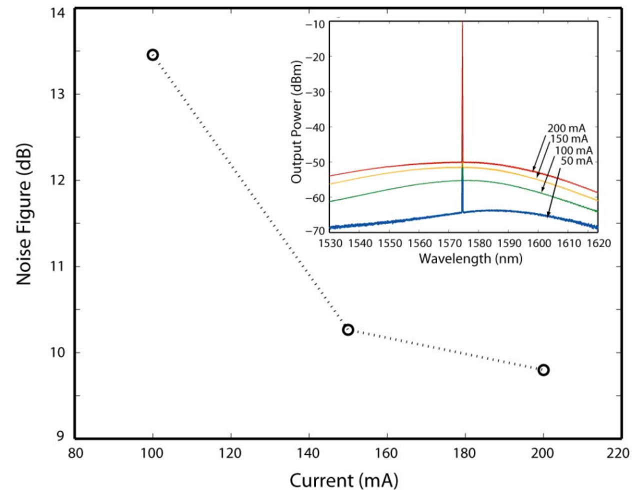

Fig. 5. NF with different currents. (inset) Amplified spectra.

from the III–V materials with silicon waveguides that control the characteristics of the optical mode. The demonstrated chip gain is 13 dB which can be improved beyond 20 dB with optimization of thermal and electrical properties of the device. The 3-dB output saturation power of the device is 11 dBm. The evanescent coupling scheme uses offset QWs, which provide lower QW confinement factor leading to higher output saturation powers than a centered QW optical amplifier. This amplifier design allows for efficient integration with other active devices such as silicon evanescent lasers, photodetectors on a silicon photonics platform.

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