

PROF. C. PATRICK YUE

Associate Professor of Electrical and Computer Engineering
Associate Director, Computer Engineering Program
Harold Frank Hall 5159, University of California, Santa Barbara, CA 93106
cpyue@ece.ucsb.edu, Phone: (805) 893-7825
www.ece.ucsb.edu/yuegroup

PUBLICATIONS

Peer-Reviewed Conference Papers

- C1 P. Park, L. Chen, L. Wang, S. Long, H. K. Yu, and C. P. Yue, "On-Wafer Wireless Testing and Mismatch Monitoring Using RF Transmitters with Integrated Antennas," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, June, 2009.
- C2 K.-H. Liang, L. Chen, and C. P. Yue, "A 200-Mb/s 10-mW Super-regenerative Receiver at 60 GHz Using 65-nm CMOS Technology," in *Proceedings of International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, April 2009.
- C3 M. Seo, B. Jagannathan, C. Carta, J. Pekarik, L. Chen, C. P. Yue, and M. Rodwell, "A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS using Dummy-Prefilled Microstrip Lines," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, Feb. 2009.
- C4 C. Sheldon, E. Torkildson, M. Seo, C. P. Yue, M. Rodwell, and U. Madhow, "Spatial multiplexing over a line-of-sight millimeter-wave MIMO link: A two-channel hardware demonstration at 1.2Gbps over 41m range," in *Proceedings of European Conference on Wireless Technology (EuWiT)*, pp. 198–201, October 2008.
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- C6 C. Sheldon, E. Torkildson, M. Seo, C. P. Yue, U. Madhow, and M. Rodwell, "A 60GHz Line-of-Sight 2x2 MIMO Link Operating at 1.2Gbps," in *IEEE International Antenna Propagation-Society Symposium (APS)*, August 2008.
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- C8 L. Chen and C. P. Yue, "Adaptive Biasing Circuit Overcoming Process Variation for High-Speed Circuits in Scaled CMOS Technology," in *Proceedings of International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, April 2008.
- C9 P. Park and C. P. Yue, "A Feasibility Study of On-wafer Wireless Testing," in *Proceedings of International Symposium on VLSI Design, Automation & Test (VLSI-DAT)*, April 2008.
- C10 J. Jang and C. P. Yue, "Low-Power Feedback-Enhanced Electro-mechanical Impedance (FEMI) Sensors," in *Proceedings of SPIE International Symposia on Smart Structures & Materials and Nondestructive Evaluation for Health Monitoring and Diagnostics*, Mar. 2008.
- C11 C. P. Yue and D. H. Shin, "Cell-Based High-Frequency IC Design in Scaled CMOS," in *the Proceedings of IEEE Radio-Frequency Integration Technology (RFIT)*, December, 2007.
- C12 D. H. Shin, J. Park, and C. P. Yue, "A Low-Power, 3–5-GHz CMOS UWB LNA Using Transformer Matching Technique," in *IEEE Asian Solid-State Circuits Conference Proceedings of Technical Papers*, November 2007.
- C13 J. Park, J.F. Liu, L. R. Carley, and C. P. Yue, "A 1-V, 1.4-2.5 GHz Charge-Pump-Less PLL for a Phase Interpolator Based CDR," in *2007 IEEE Custom Integrated Circuits Conference Proceedings of Technical Papers*, September 2007.
- C14 K. Choi, D. H. Shin, C. P. Yue, "A 1.2-V, 5.8-mW, Ultra-Wideband Folded Mixer in 0.13- μ m CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, pp. 489–492, June 2007.

- C15 D. Hong, S. Sabri, C. P. Yue, and K.-T. Cheng, "A Two-Tone Test Method for Continuous-Time Adaptive Equalizers," in *2007 Design, Automation and Test in Europe*, April 2007.
- C16 R. Sun, J. Park, F. O'Mahony, and C. P. Yue, "A Tunable Passive Filter for Low-Power High-Speed Equalizers," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, June 2006.
- C17 D. H. Shin and C. P. Yue, "A Unified Modeling and Design Methodology for RFICs Using Parameterized Sub-Circuit Cells," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, June 2006.
- C18 D. W. Greve, I. J. Oppenheim, H. Sohn, and C. P. Yue, "An Inductively Coupled (Wireless) Lamb Wave Transducer," in the *Third International Workshop on Advanced Smart Materials and Smart Structures Technology*, May 2006.
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- C26 F. O'Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "Design of a 10GHz clock distribution network using coupled standing-wave oscillators," in *Proceedings of 40th Design Automation Conference (DAC)*, pp. 682–687, June 2003.
- C27 N. Talwalkar, C. P. Yue, and S. S. Wong, "An Integrated 5.2GHz CMOS T/R Switch with LC-Tuned Substrate Bias," in *2003 International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 362–363, February 2003.
- C28 F. O'Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "10GHz Clock Distribution Using Coupled Standing-Wave Oscillators," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 428–429, February 2003. **(Best Student Paper)**
- C29 R. T. Chang, C. P. Yue, and S. S. Wong, "Near Speed-of-Light On-Chip Electrical Interconnect," *IEEE Symposium on VLSI Circuits*, pp. 18–21, June 2002.
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- C34 H. T. Soh, C. P. Yue, A. M. McCarthy, C. Ryu, T. H. Lee, and C. F. Quate, "Ultra-Low Resistance, Through-Wafer Via (TWV) Technology and Its Applications in Three Dimensional Structures in

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- C38 C. P. Yue, C. Ryu, J. Lau, T. H. Lee, and S. S. Wong, “A Physical Model for Planar Spiral Inductors on Silicon,” in *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 155–158, Dec. 1996.

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- I1 C. P. Yue and D. H. Shin, “Cell-based high-frequency IC design in scaled CMOS,” in *Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT)*, pp. 1452–1455, October 2008.
- I2 C. P. Yue and S. S. Wong, “Scalability of RF CMOS (Invited),” in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Digest of Papers*, pp. 53–56, June 2005.
- I3 S. S. Wong, S.-Y. Kim, C. P. Yue, R. Chang, and F. O'Mahony, “Extraction and Applications of On-Chip Interconnect Inductance,” in *Proceedings of the 7th International Conference on Solid-State and Integrated-Circuit Technology (ICSSICT)*, pp. 141–146, October 2004.
- I4 S. S. Wong, P. Yue, R. Chang, S.-Y. Kim, B. Kleveland, and F. O'Mahony, “On-Chip Interconnect Inductance - Friend or Foe,” in *Proceedings of the 4th International Symposium on Quality Electronic Design (ISQED)*, pp. 389–394, March 2003.
- I5 N. Talwalkar, C. P. Yue, and S. S. Wong, “Compact Modeling of High Frequency Phenomena for On-chip Spiral Inductors,” in *Proceedings of Sixth International Conference on Modeling and Simulation of Microsystems (ICMSM)*, February 2003.
- I6 T. Blalack, Y. Leclercq, and C. P. Yue, “On-Chip RF Isolation Techniques,” in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, pp. 205–211, Oct. 2002.
- I7 C. P. Yue and S. S. Wong, “Design Strategy of On-Chip Inductors for Highly Integrated RF Systems,” in *Proceedings of 36th Design Automation Conference (DAC)*, pp. 982–987, June 1999.

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- J1 P. Park, D. H. Shin, and C. P. Yue, “High-Linearity CMOS T/R Switch Design Above 20 GHz Using Asymmetrical Topology and AC-Floating Bias,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 4, pp. 948–956, April 2009.
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- J3 A. Kaya, C. P. Yue, and J. A. Bain, “Experimental Evidence for Gyromagnetic Damping in Magnetic Heads Determined by Impedance Measurements up to 9 GHz,” *IEEE Transactions on Magnetics*, vol. 41, no. 10, pp. 2923–2925, October 2005.
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- J5 N. A. Talwalkar, C. P. Yue, H. Gan, and S. S. Wong, “Integrated CMOS transmit-receive switch using LC-tuned substrate bias for 2.4-GHz and 5.2-GHz applications,” *IEEE Journal of Solid-State Circuits*, vol. 39, no. 6, pp. 863–870, June 2004.
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Book Chapters

- B1 C. P. Yue, J. Park, R. Sun, L. R. Carley, and F. O'Mahony, "Low-Power, Parallel Interface with Continuous-Time Adaptive Passive Equalizer and Crosstalk Cancellation," in *Design of High-Speed Communications Circuits*, edited by Ramesh Harjani, World Scientific Publishing, ISBN: 981-256-590-6, pp. 459–476, Jan. 2006.
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- T2 PilJae Park, "A Fully Integrated Transmitter for On-Wafer Wireless Testing," Ph.D. Thesis, University of California Santa Barbara, 2008.
- T3 Jaejin Park, "A 10 Gb/s 8-PAM Transceiver in a 0.13- μ m CMOS Process," Ph.D. Thesis, Carnegie Mellon University, 2006.
- T4 Ruifeng Sun, "A Low-Power 20-Gb/s Continuous-Time Adaptive Passive Equalizer," M.S. Thesis, Carnegie Mellon University, 2005.
- T5 C. Patrick Yue, "On-Chip Spiral Inductors for Silicon-Based Radio Frequency Integrated Circuits," Ph.D. Thesis, Stanford, 1998.

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- P2 U.S. Patent No. 7,236,044, June 26, 2007.
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- P13 U.S. Patent No. 6,504,431, January 7, 2003.
D. J. Weber, C. P. Yue, and D. K. Su, "*CMOS Transceiver Having an Integrated Power Amplifier.*"