

Design Strategy of On-Chip Inductors for Highly Integrated RF Systems

(Invited Paper)

C. Patrick Yue
T-Span Systems Corporation
44 Encina Drive
Palo Alto, CA 94301
(650) 470-8251
patrick@tspan.com

S. Simon Wong
Stanford University
Center for Integrated Systems 202
Stanford, CA 94305
(650) 725-3706
swong@snf.stanford.edu

1. ABSTRACT

This paper describes a physical model for spiral inductors on silicon which is suitable for circuit simulation and layout optimization. Key issues related to inductor modeling such as skin effect and silicon substrate loss are discussed. An effective ground shield is devised to reduce substrate loss and noise coupling. A practical design methodology based on the trade-off between the series resistance and oxide capacitance of an inductor is presented. This method is applied to optimize inductors in state-of-the-art processes with multilevel interconnects. The impact of interconnect scaling, copper metallization and low-K dielectric on the achievable inductor quality factor is studied.

1.1 Keywords

Spiral inductor, quality factor, skin effect, substrate loss, substrate coupling, patterned ground shield, interconnects

2. INTRODUCTION

The rapid growth of the wireless communication market has fueled the demand for low-cost radio systems on a chip. Traditionally, radio systems are implemented on the board level using a large number of discrete components. Silicon IC technology has progressed to offer device performance suitable for analog operations up to several giga-hertz and thus presents the potential for integrating radios on a chip. At the same time, a great deal of effort has been devoted to on-chip inductors as they are used extensively in RF circuits for frequency tuning and impedance transformation. The use of spiral inductors in silicon IC was first reported by Nguyen

and Meyer in 1990 [1]. Since then, numerous research work has been published on modeling inductors [2]–[4] and on techniques to improve the quality factor (Q) [7]–[10]. For typical inductance ranging from 1 to 20 nH, conventional silicon technologies can deliver Q 's of about 5. However, as interconnect technology advances, the achievable Q is improving to above 10. Although on-chip inductors have Q 's significantly lower than their discrete counterparts (typical Q 's of about 50), they have been proven to be useful and essential in highly integrated RF systems [11][12]. A single-chip GPS receiver have employed as many as sixteen on-chip inductors [13]. In order to efficiently identify the optimal inductor layouts and account for the inductors and their parasitics in circuit simulation, an accurate equivalent circuit model is necessary. This paper begins with the description of a physical inductor model. Based on the insight from this model, a special ground shield is constructed to improve the inductor performance. Then, a simple and effective method for inductor layout optimization is described. Finally, the impact of advancements in interconnect technology on inductors is investigated.

3. INDUCTOR MODELING

The key to accurate, physical modeling is the ability to identify the relevant parasitics and their effects. Since an inductor is intended for storing magnetic energy, the inevitable resistance (R) and capacitance (C) in a real inductor are counter-productive and thus are considered parasitics. The parasitic resistances dissipate energy through ohmic loss while the parasitic capacitances store unwanted electric energy.

The cut-away view of a typical on-chip inductor in Figure 1 highlights the parasitics present in the structure. The inductance and resistance of the spiral and the underpass is represented by the spiral inductance, L_s , and the series resistance, R_s , respectively. The overlap between the spiral and the underpass allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance, C_s . The oxide capacitance between the spiral and the silicon substrate is modeled by C_{ox} . The capacitance and resistance of the silicon substrate are modeled by C_{Si} and R_{Si} .

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.
DAC 99, New Orleans, Louisiana
©1999 ACM 1-58113-092-9/99/0006..\$5.00

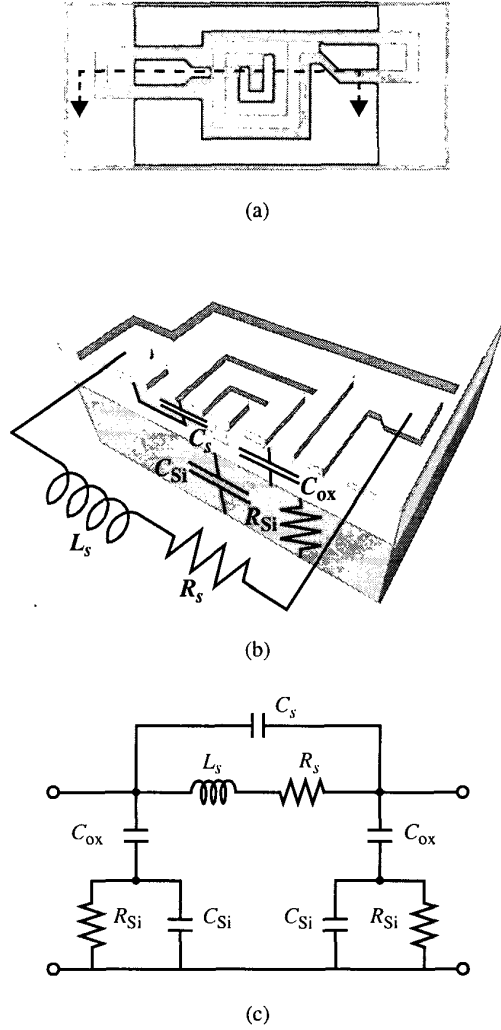


Figure 1. (a) Top view, (b) cut-away view, and (c) the physical model of an on-chip spiral inductor.

3.1 Spiral Inductance

The foundation for computing inductance is built on the concepts of the self inductance of a wire and the mutual inductance between a pair of wires. A comprehensive collection of formulas and tables for inductance calculation was summarized by F.W. Grover in [14]. Based on Grover's formulas, Greenhouse developed an algorithm for computing the inductance of planar rectangular spirals [15]. The Greenhouse's method states that the overall inductance of a spiral can be computed by summing the self inductance of each wire segment and the positive and negative mutual inductance between all possible wire segment pairs. The mutual inductance between two wires depends on their angle of intersection, length, and separation. Two wires orthogonal to each other have no mutual coupling since their magnetic flux are not linked together. The current flow directions in the wires determine the sign of coupling. The

coupling is positive if the currents in the two wires are in same direction and negative for opposite currents. To evaluate the overall inductance of a N -turn square spiral, it involves $4N$ self-inductance terms, $2N(N-1)$ positive mutual-inductance terms and $2N^2$ negative mutual-inductance terms.

3.2 Series Resistance

The series resistance of the inductor increases with frequency due to skin effect. A first-order model for R_s can be expressed by

$$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-l/\delta})} \quad (1)$$

where δ and ρ denote the skin depth and resistivity of the interconnect material, respectively. Proximity effect between the traces of the spiral can also cause R_s to increase because of mutually induced eddy current. From electromagnetism simulation [16], we found that if the adjacent lines are properly spaced, the proximity effect between adjacent lines is negligible and is therefore not considered in our model.

3.3 Substrate Effects

The inductor quality factor can be derived from the circuit model shown in Figure 1 as follows:

$$Q = 2\pi \frac{|\text{Peak Magnetic Energy} - \text{Peak Electric Energy}|}{\text{Energy Loss in One Oscillation Cycle}}$$

$$= \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + [(\omega L_s/R_s)^2 + 1] \cdot R_s} \quad (2)$$

$$\times \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o \right)$$

where

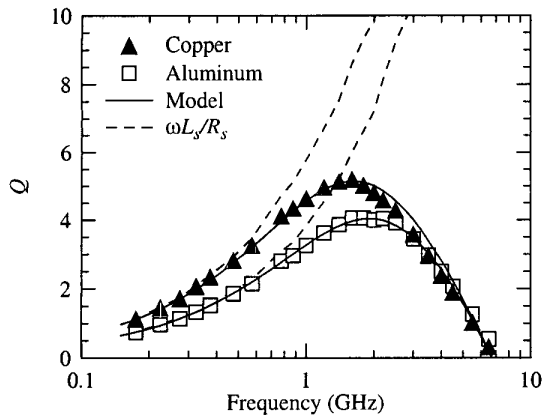
$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \quad (3)$$

and

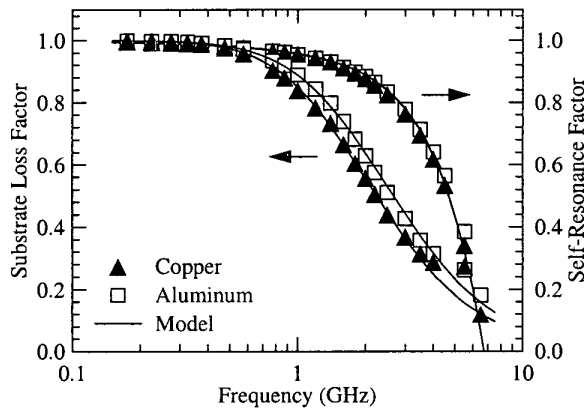
$$C_p = C_{ox} \cdot \frac{1 + \omega^2 (C_{ox} + C_{si}) C_{si} R_{si}^2}{1 + \omega^2 (C_{ox} + C_{si})^2 R_{si}^2} \quad (4)$$

In (2), $\omega L_s/R_s$ accounts for the magnetic energy stored and the ohmic loss in the series resistance. The second term in (2) is the substrate loss factor representing the energy dissipated in the silicon (R_{si}). The last term is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at the self-resonant frequency.

Figure 2 shows the measured and modeled frequency behavior of Q and the degradation factors for two typical on-chip inductor. One of the inductors uses aluminum and the other uses copper. In both cases, at low frequencies, Q is well described by $\omega L_s/R_s$ when both degradation factors are close to unity. As frequency increases, the degradation



(a)



(b)

Figure 2. The frequency behavior of (a) Q and (b) substrate loss and self-resonance factors for typical on-chip spiral inductors.

factors decrease from unity as shown in Figure 2(b). This demonstrates that the reduction of Q at high frequencies is a combined effect of substrate loss and self-resonance. Physically, the substrate loss stems from the penetration of electric field into the silicon. As the potential drop across R_{Si} increases with frequency, the energy dissipation in the substrate becomes more severe. For typical on-chip inductors, the substrate loss factor causes 10 to 40% reduction from $\omega L_s/R_s$ at 1 to 2 GHz.

4. PATTERNED GROUND SHIELD

To reduce substrate loss, the inductor's electric field must be terminated before reaching the silicon substrate. A conductive ground shield between the inductor and the substrate can achieve this effect. However, the image current induced by the magnetic field in the conductive ground shield will flow in a direction opposite to that of the current in the spiral. The negative self-inductance will then lead to a significant drop in the total inductance and hence Q . To increase the resistance to the image current, the ground

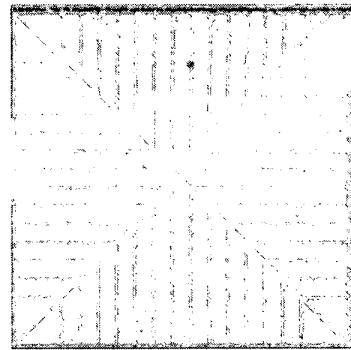


Figure 3. Close-up view of the patterned ground shield.

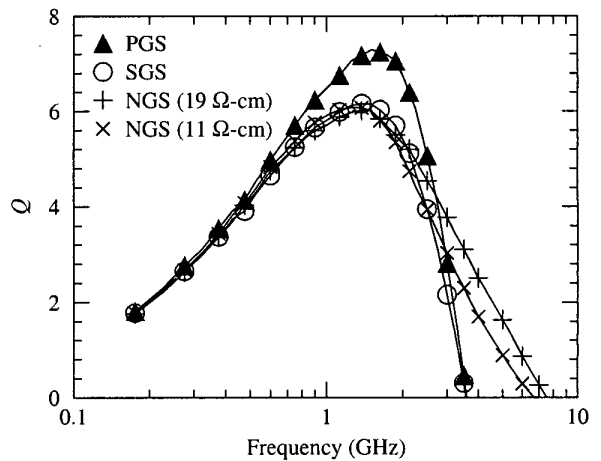


Figure 4. Effect of polysilicon ground shields on Q .

shield can be patterned with slots orthogonal to the spiral as illustrated in Figure 3. In fact, the slots act as open circuits to cut off the path of the induced current.

Figure 4 shows that a patterned ground shield (PGS) implemented using doped polysilicon ($12 \Omega/\text{Sq.}$) improves the Q by more than 30% at 2 GHz over the un-shielded inductors (NGS) and inductors with non-patterned ground shield (SGS). Similar results have been obtained with diffusion shields [17].

In a highly integrated RF systems where multiple inductors are used, noise coupling through substrate can cause detrimental effects on circuit functions. Substrate coupling between adjacent inductors has been measured. Figure 5 shows that the more conductive substrate has a stronger coupling, higher $|S_{21}|$, due to its higher admittance. In contrast, the polysilicon PGS improves the isolation up to 25 dB.

5. DESIGN METHODOLOGY

As the PGS eliminates the substrate effects (R_{Si} and C_{Si}),

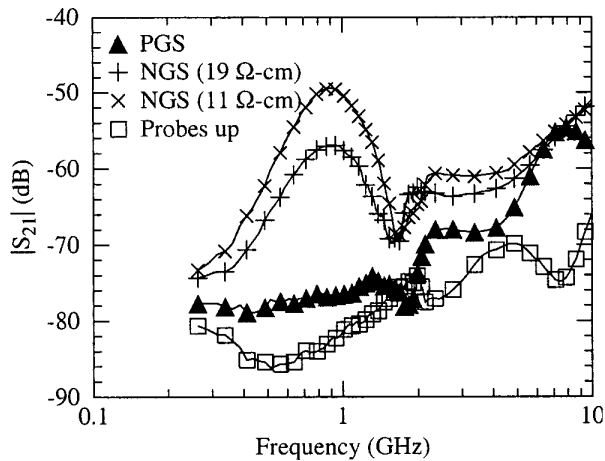


Figure 5. Effect of polysilicon PGS on substrate coupling between two adjacent inductors. The “Probes up” data represents the intrinsic noise floor of the testing setup.

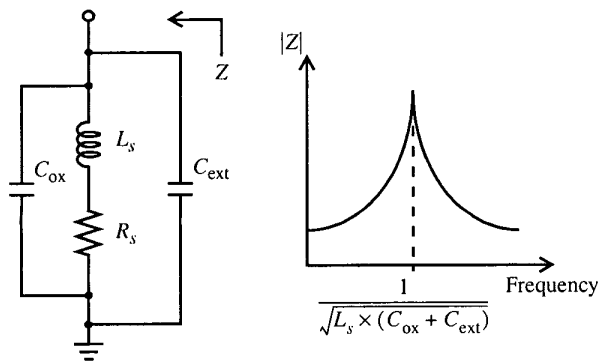


Figure 6. The resonance frequency of an on-chip inductor and capacitor is determined by the spiral inductance and the sum of the inductor’s oxide capacitance and external capacitance.

the design of on-chip inductors is simplified to a trade-off between the series resistance (R_s) and the oxide capacitance (C_{ox}). To reduce R_s , one can widen the inductor traces or strap several metal layers together. But at the same time, C_{ox} is increased. In practice, C_{ox} can be absorbed as part of the capacitance that is resonating with L_s (see Figure 6).

Based on this method, sixteen inductors with patterned ground shields have been designed for a fully functional single-chip GPS receiver [13]. The receiver was fabricated in a 0.5- μm CMOS process with three metal layers. The top-level metal has a dc sheet resistance of 15 m Ω/Sq . and has about 4 μm of oxide above the PGS. The integrated inductors can be seen clearly in the die photo shown in Figure 7. The modeled and measured inductance and Q are summarized in Table 1. Excellent agreement is obtained.

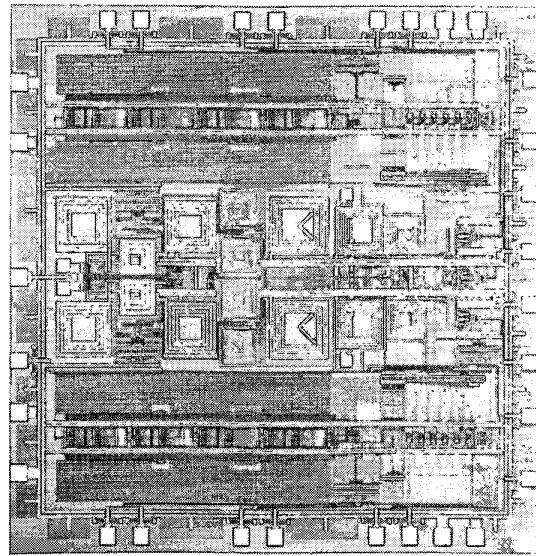


Figure 7. Die photo of the single-chip GPS receiver which employed sixteen spiral inductors with patterned ground shields.

Table 1: Summary of the spiral inductors in the 0.5- μm CMOS GPS receiver.

Modeled		Measured	
Inductance	Q	Inductance	Q
1.2 nH	6.7	1.4 nH	6.8
5.6 nH	7.6	4.8 nH	6.6
5.9 nH	7.4	5.6 nH	6.6
6.9 nH	7.0	6.6 nH	6.8
10.0 nH	4.7	9.5 nH	4.5
10.0 nH	6.3	10.3 nH	6.0
14.3 nH	5.1	14.5 nH	5.2

6. INDUCTORS IN ADVANCED PROCESS

Dramatic changes is expected for interconnect technology in the next few generations. This section investigates their impacts on inductor performance. A conventional 0.25- μm process usually has five metal layers. The top metal layer is typically about 1 μm thick whereas the lower layers are about 0.5 μm . The interlevel dielectric thickness is approximately 1 μm and thus the total oxide thickness below the top metal layer is about 7 μm . It is projected that 0.13- μm technology will offer seven levels of interconnect with a total oxide thickness of 10 μm [18]. Furthermore, copper interconnect and low-K dielectric are expected to become available.

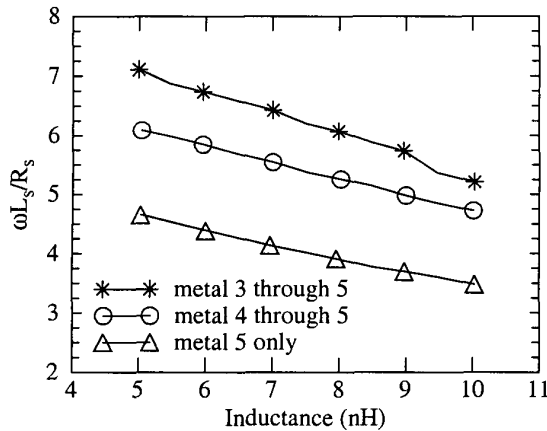


Figure 8. Effect of strapping metal layers.

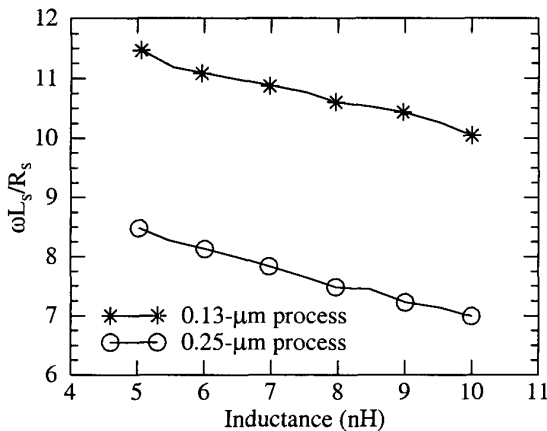


Figure 9. Comparison between inductors in 0.25- μm (strapping metal 3 through 5) and 0.13- μm (strapping metal 3 through 7) process.

Since we assumed that C_{ox} will be incorporated as part of the tuning capacitance, the inductance's quality is better represented by $\omega L_s/R_s$, which is used as a measure of the inductor performance in this study. The optimization was performed at 2 GHz for all cases.

Figure 8 illustrates that by strapping metal 3 through 5, a 50% improvement over using metal 5 alone can be obtained. The oxide thickness below metal 3 is 4 μm . A maximum $\omega L_s/R_s$ of 7 can be achieved for a 5-nH inductor at 2 GHz.

Figure 9 compares the achievable $\omega L_s/R_s$ for 0.25- μm and 0.13- μm processes. The 0.13- μm process offers an enhancement of approximately 40% by strapping metal 3 through 7.

The impact of copper and low-K dielectric on $\omega L_s/R_s$ is shown in Figure 10. A 30% improvement is obtained when

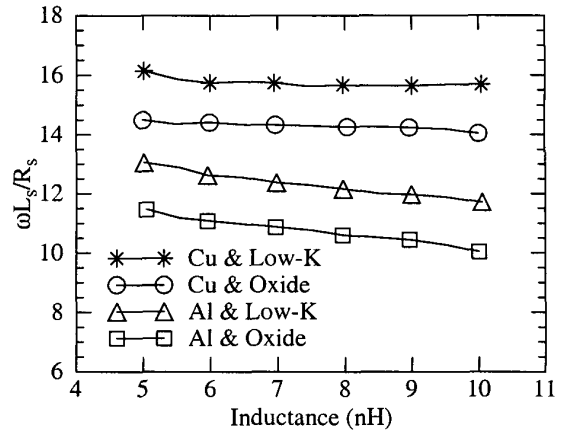


Figure 10. Impact of copper interconnect and low-K dielectric on inductor performance for 0.13- μm process.

aluminum is replaced by copper. Low-K dielectric ($K = 2.5$) offers an additional 15% enhancement when oxide is replaced. By combining the two materials, one can expect inductors in the 0.13- μm generation to have $\omega L_s/R_s$ over 15.

7. CONCLUSIONS

This paper summarized the development of a physical inductor model and the patterned ground shield. An effective design methodology based on the trade-off of the series resistance and oxide capacitance was presented. This method was utilized in designing the inductors for a single-chip GPS receiver. A study on the inductor performance using advanced interconnects was also reported.

8. ACKNOWLEDGEMENTS

The authors would like to thank the Rockwell International and Stanford Nanofabrication Facility staff for their assistance in fabrication. Special thanks goes to Dr. Derek Shaeffer, Dr. Arvin Shahani, and Professor Tom Lee at Stanford for helpful discussions.

9. REFERENCES

- [1] N.M. Nguyen and R.G. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 1028-1030, August 1990.
- [2] D. Lovelace, N. Camilleri, and G. Kannell, "Silicon MMIC inductor modeling for high volume, low cost applications," *Microwave Journal*, pp. 60-71, August 1994.
- [3] J. Crols, P. Kinget, J. Craninckx, and M.S.J. Steyaert, "An analytical model of planar inductors on lowly doped silicon substrates for high frequency analog design up to 3 GHz," in *1996 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 28-29, June 1996.

- [4] C.P. Yue, C. Ryu, J. Lau, T.H. Lee, and S.S. Wong, "A physical model for planar spiral inductors on silicon," in *1996 International Electron Devices Meeting Technical Digest*, pp. 155–158, December 1996.
- [5] J.R. Long and M.A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, March 1997.
- [6] A.M. Niknejad and R.G. Meyer, "Analysis and optimization of monolithic inductors and transformers for RF ICs," in *Proceedings of the IEEE 1997 Custom Integrated Circuits Conference*, pp. 375–378, May 1997.
- [7] J.Y.-C. Chang, A.A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-mm CMOS RF amplifier," *IEEE Electron Device Letters*, vol. 14, no.5, pp. 246–248, May 1993.
- [8] K.B. Ashby, I.A. Koullias, W.C. Finley, J.J. Bastek, and S. Moinian, "High Q inductors for wireless applications in a complementary silicon bipolar process," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 1, pp. 4–9, January 1996.
- [9] J.N. Burghartz, M. Soyuer, and K.A. Jenkins, "Integrated RF and microwave components in BiCMOS technology," *IEEE Transactions on Electron Devices*, vol. 43, no. 9, pp. 1559–1570, September 1996.
- [10] C.P. Yue and S.S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp.743–752, May 1998.
- [11] T.D. Stetzler, I.G. Post, J.H. Havens, and M. Koyama, "A 2.7–4.5 V single chip GSM transceiver RF integrated circuit," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 12, pp. 1421–1429, December 1995.
- [12] R.G. Meyer, W.D. Mack, and J.J.E.M. Hagreraats "A 2.5-GHz BiCMOS transceiver for wireless LAN's," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2097–2104, December 1997.
- [13] D.K. Shaeffer, A.R. Shahani, S.S. Mohan, H. Samavati, H. Rategh, M.M. Hershenson, M. Xu, C.P. Yue, D. Eddleman, and T.H. Lee, "A 115-mW, 0.5- μ m CMOS GPS receiver with wide dynamic-range active filters," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2219–2231, December 1998.
- [14] F.W. Grover, *Inductance Calculations*, Princeton, New Jersey: Van Nostrand, 1946. Reprinted by New York, New York: Dover Publications, 1962.
- [15] H.M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Transactions on Parts, Hybrids, and Packing*, vol. PHP-10, no. 2, pp. 101–109, June 1974.
- [16] *Maxwell 2D Parameter Extractor User's Reference*, Ansoft Corporation, 1997.
- [17] C.P. Yue and S.S. Wong, "A study on substrate effects of silicon-based RF passive components," in *1999 MTT-S International Microwave Symposium Digest*, June 1999.
- [18] *National Technology Roadmap for Semiconductors*, SIA, 1997.