

# A Study on Substrate Effects of Silicon-Based RF Passive Components

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## Abstract

The substrate effects on the performance of metal-insulator-metal (MIM) capacitors and spiral inductors are critical to silicon RF IC's. Based on measured results and physical modeling, this paper presents an extensive study on the substrate parasitics. Contrary to common belief, it is shown that (1) the energy loss in lightly doped substrates is higher than that in epi substrates with heavily doped bulks, (2) the eddy current induced by inductors is negligible even in heavily doped epi substrates up to several giga-hertz, and (3) the high-frequency degradation of  $Q$  for inductors on epi substrates is due to a larger substrate parasitic capacitance which results in a lower self-resonant frequency compared to lightly doped cases. Furthermore, we report for the first time the improvement in  $Q$  for inductors on epi substrates with a patterned ground shield. A fourfold improvement in the  $Q$  of a  $LC$  resonator is achieved using polysilicon, or source/drain diffusion, PGS's.

## Introduction

On-chip passive components are imperative for silicon-based RF IC's. The detrimental effects of the semi-conducting substrate parasitics on metal-insulator-metal capacitors [1], bond pads [2], and spiral inductors [3] have been reported. However, the basic understanding of the physics behind these effects is still not well known. Heavily doped substrates, also known as "epi" substrates, are routinely employed in CMOS and BiCMOS processes while lightly doped ( $1-30 \Omega\text{-cm}$ ) substrates are commonly used in bipolar and some CMOS technologies. Typical epi substrates consist of a lightly doped ( $1-30 \Omega\text{-cm}$ ) epitaxial layer grown on a degenerately doped ( $10-20 \text{m}\Omega\text{-cm}$ ) bulk substrate. The goal of this work is to present a thorough analysis of the parasitic effects due to both kinds of substrate, and therefore facilitate the integration of RF passive components in silicon IC technologies.

## Experimental Results

### A. Capacitors and Bond Pads

To investigate substrate parasitics associated with the bottom plate of a MIM capacitor, metal pads are fabricated on epi, lightly doped, and quartz ( $\epsilon_r = 3.9$ ) substrates. The substrate profile under the pads are listed in TABLE I. The

TABLE I  
Summary of  $100 \times 100 \mu\text{m}^2$  pads.

Sample	$C_{LF}$	Substrate Description
Epi4.1 $\mu\text{m}$	114.3 fF	4.1 $\mu\text{m}$ ox. on epi on p+ Si
Ld4.5 $\mu\text{m}$	100.0 fF	4.5 $\mu\text{m}$ ox. on $10 \Omega\text{-cm}$ Si
Ld5.5 $\mu\text{m}$	79.9 fF	5.5 $\mu\text{m}$ ox. on $10 \Omega\text{-cm}$ Si
Ld6.5 $\mu\text{m}$	67.2 fF	6.5 $\mu\text{m}$ ox. on $10 \Omega\text{-cm}$ Si
Qz2.1 $\mu\text{m}$	5.0 fF	2.1 $\mu\text{m}$ ox. on quartz

low-frequency capacitance ( $C_{LF}$ ) is the pad capacitance measured at 175 MHz. During measurements, the substrates are grounded from the wafer backside through the testing chuck. Measured  $S_{11}$  is converted to  $Y_{11}$ , from which the pad capacitance ( $C_{pad}$ ) and quality factor ( $Q_{pad}$ ) are extracted. The frequency behavior of  $C_{pad}$  is plotted in Fig. 1. For quartz,  $C_{pad}$  is frequency-independent at 6 fF since the electric field penetrates through the entire substrate. For the silicon samples,  $C_{pad}$  is determined by the oxide capacitance at low frequencies. Beyond several hundred mega-hertz,  $C_{pad}$  decreases with frequency as the electric field penetrates into the substrate [3][4]. For lightly doped substrates,  $C_{pad}$  approaches the bulk capacitance of about 20 fF at very high frequencies regardless of the oxide thickness difference. For the epi substrate, the

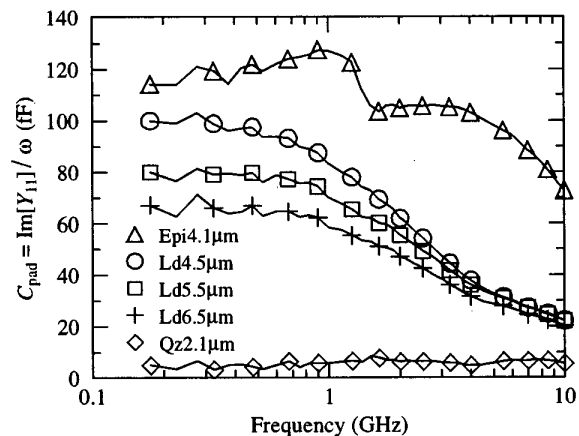


Fig. 1. Measured metal pad capacitance.

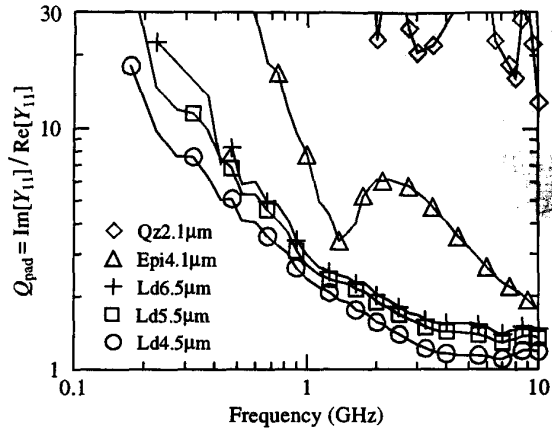


Fig. 2. Measured  $Q$  of metal pad capacitance.

highly conductive bulk acts as an effective ground up to several giga-hertz; therefore, the electric field penetration is limited to the thin epi layer ( $7\ \mu\text{m}$ ). This is consistent with the interfacial charge theory described in [5]. Above  $4\ \text{GHz}$ ,  $C_{\text{pad}}$  begins to decrease as the heavily doped substrate can no longer terminate the electric field.

$Q_{\text{pad}}$  is a measure of energy loss in the substrate; in other words, higher  $Q_{\text{pad}}$  signifies less substrate loss (see Fig. 2). As expected, the insulating quartz substrate offers significantly higher  $Q_{\text{pad}}$  than the semiconducting silicon substrates. For the lightly doped samples,  $Q_{\text{pad}}$  is higher with thicker oxide since the lossy silicon is further away.  $Q_{\text{pad}}$  for the epi substrate is higher than the lightly doped cases despite it has the thinnest oxide ( $4.1\ \mu\text{m}$ ). This indicates that epi substrate is actually less lossy as the electric field only penetrates into the thin resistive epi layer and therefore the lossy volume is considerably smaller than that of the entire lightly doped bulk.

### B. Spiral Inductors

The spiral inductors fabricated on epi, lightly doped, and quartz substrates are summarized in TABLE II. The quartz sample serves as a control for no substrate eddy current can be induced in dielectric. Inductor Gp8nH is fabricated with a  $0.32\text{-}\Omega/\square$  aluminum solid ground plane (SGP) underneath the inductor to deliberately create eddy current. The SGP sheet resistance is adjusted to be similar to that of the  $p^+$  bulk in the epi substrate. By comparing the inductors on epi substrate to the ones on quartz and SGP, the significance of the substrate eddy current in the  $p^+$  bulk can be evaluated. For comparison purposes, the inductors are designed to have similar low-frequency  $L/R$  ratio ( $L_{\text{LF}}/R_{\text{dc}}$ ) of approximately  $1.6\ \text{nH}/\Omega$ . Inductance, parasitic resistances and capacitances, and  $Q$  are extracted from measured two-port S parameters using the techniques described in [6].

TABLE II  
Summary of spiral inductors.

Sample	$L_{\text{LF}}$	$R_{\text{dc}}$	Substrate Description
Epi5nH	5.3 nH	$3.0\ \Omega$	$4.1\ \mu\text{m}$ ox. on epi on $p^+$ Si
Epi10nH	10.5 nH	$7.0\ \Omega$	$4.1\ \mu\text{m}$ ox. on epi on $p^+$ Si
Ld8nH	8.1 nH	$5.0\ \Omega$	$5.6\ \mu\text{m}$ ox. on $19\ \Omega\text{-cm}$ Si
Gp8nH	7.9 nH	$5.0\ \Omega$	$5.2\ \mu\text{m}$ ox. on ground plane
Qz8nH	7.9 nH	$5.0\ \Omega$	$2.1\ \mu\text{m}$ ox. on quartz

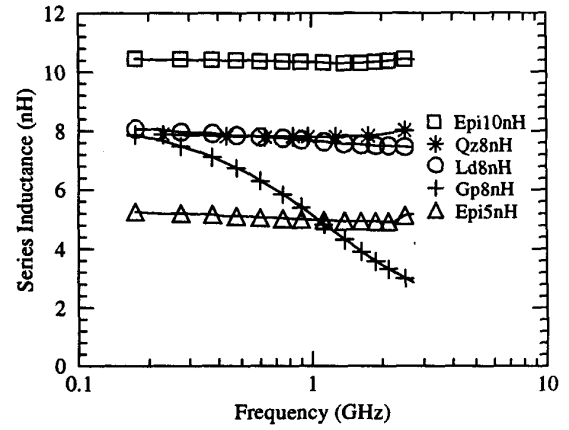


Fig. 3. Measured inductor series inductance.

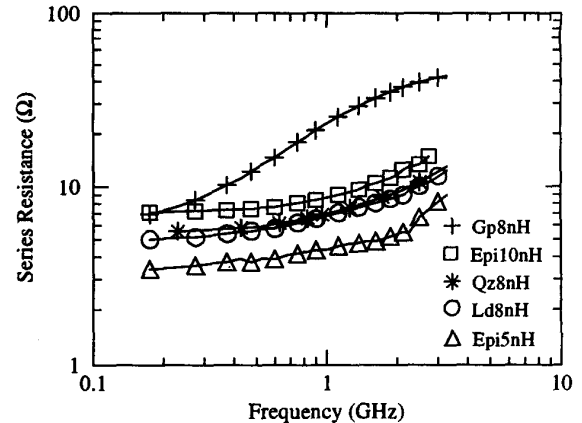


Fig. 4. Measured inductor series resistance.

The measured series inductance and resistance are shown in Fig. 3 and Fig. 4, respectively. Ld8nH and Qz8nH have the same series inductance and resistance indicating that the substrate eddy current is insignificant for the lightly doped substrate as expected. Gp8nH

exhibits much lower inductance and higher resistance owing to the eddy current in the SGP. For the inductors on epi substrates, Epi5nH and Epi10nH manifest the same kind of frequency behavior for the inductance and resistance as those on lightly doped and quartz substrates, proving that eddy current in the epi substrate is negligible up to several giga-hertz. Although the  $p^+$  bulk has a sheet resistance close to that of the SGP in Gp8nH, the carriers in the  $p^+$  bulk are distributed over a much larger volume and hence they are effectively much farther away from the inductor. As a result, no significant eddy current can be induced. In Fig. 5, Qz8nH has the highest  $Q$  because it has the lowest substrate loss and the smallest parasitic capacitance. Gp8nH has the worst  $Q$  due to the eddy current which leads to decrease in inductance and increase in resistance. The maximum  $Q$  for inductors on lightly doped and epi substrates are similar; however, the epi cases have a lower self-resonant frequency ( $srf$ ) because of a larger substrate capacitance (as discussed earlier).

While substrate eddy current is insignificant, ohmic loss in the resistive epi layer caused by electric field penetration is present. This loss can be eliminated by using a patterned ground shield (PGS) as depicted in Fig. 6 [6]. A polysilicon PGS is inserted between inductor Epi5nH and the epi substrate. In Fig. 7, the inductor  $Q$  is improved by about 15%. Similar improvement is obtained with a source/drain diffusion PGS. In many RF applications, inductors are employed for  $LC$  resonators. As suggested in [7], a more appropriate technique for evaluating inductor quality is by measuring the inductor impedance,  $|Z_{ind}|$ , near the  $srf$  and taking the ratio of  $srf$  to  $-3$ -dB bandwidth. This technique essentially treats the substrate parasitic capacitance as part of the resonator. In Fig. 8, measured  $|Z_{ind}|$  are plotted with respect to normalized  $srf$  to account for the difference in substrate capacitance. The resonator  $Q$  for the lightly doped and epi substrates is 2 and 3, respectively. The epi case offers higher  $Q$  because the

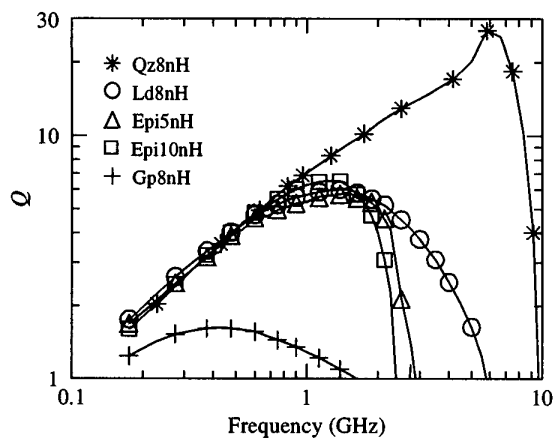
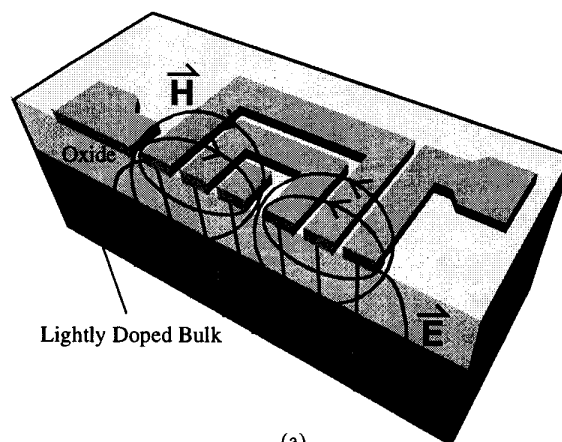
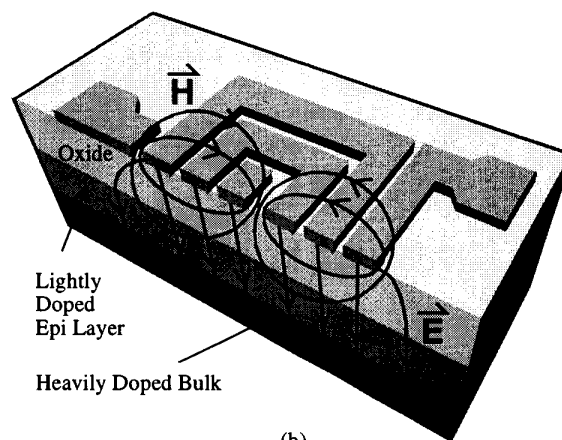


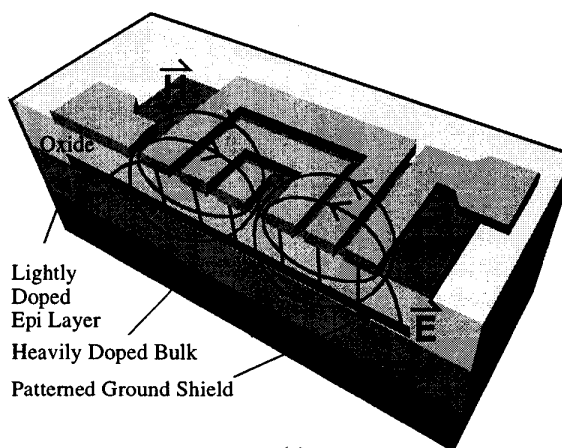
Fig. 5. Measured inductor  $Q$ .



(a)



(b)



(c)

Fig. 6. Cut-away view of the electromagnetic fields associated with spiral inductors on (a) lightly doped substrate, (b) epi substrate, and (c) epi substrate with PGS. PGS terminates the electric field but allows the magnetic field to penetrate through.

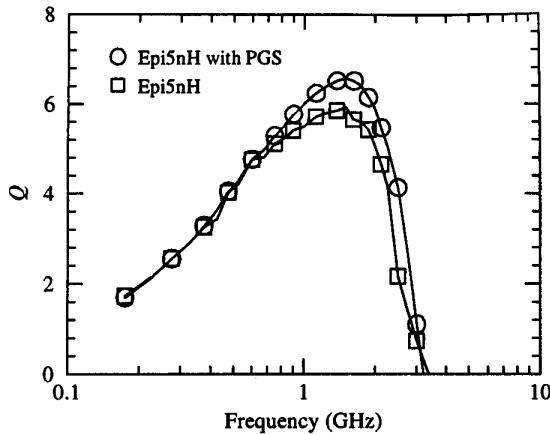


Fig. 7. Improvement in inductor  $Q$  with polysilicon PGS on epi substrate.

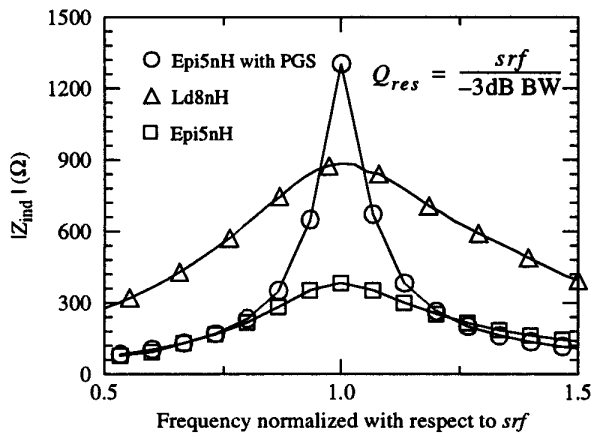


Fig. 8. Measured inductor impedance near  $srf$ . The resonator quality factor,  $Q_{res}$ , is equal to the ratio of  $srf$  to  $-3$ -dB bandwidth. The  $Q_{res}$  for inductor with PGS is four times higher.

substrate loss is less as explained in the previous section. With the insertion of a PGS, the resonator  $Q$  on epi substrate is improved from 3 to 12.

### Conclusions

Substrate effects pertaining to on-chip passive components are investigated experimentally. The results demonstrate that energy dissipation, which degrades  $Q$ , occurs predominately in the epitaxial layer for epi substrates and in the bulk for lightly doped substrates. It is shown that epi substrates present larger substrate capacitance at gigahertz frequencies. For inductive components, substrate eddy currents are shown to be negligible even in epi substrates up to several gigahertz. The effectiveness of polysilicon and diffusion PGS's for inductors on epi

substrates are demonstrated and confirmed with experimental data for the first time.

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