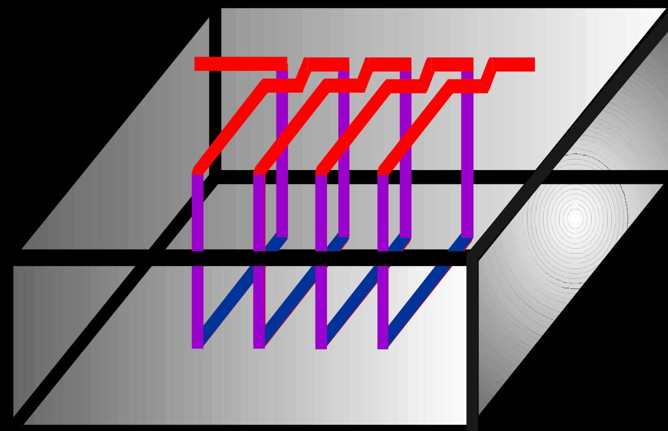
Through-Wafer Vias (TWV) and their Applications in 3 Dimensional Structures.



H.T. Soh, C.P. Yue, A.M. McCarthy, C. Ryu
T.H. Lee, and C.F. Quate

Quate Group, Stanford University.

Through-Wafer Via (TWV) Technology

Applications

- Interconnects in circuits.
  (e.g. Low Z connection to ground in mixed signal circuits.)
- 3D packaging.
  (e.g. chip stacking, monolithic packaging of sensors and actuators.)
- Novel 3D electrical and MEMS structures.
  (e.g. 3D integrated inductor.)

Key Issues

- Via Size must be small.
  (via size must be comparable to a contact pad ~ 30 μm x 30 μm.)
- Low Resistance.
  (vertical connection should have $< 100\ m\Omega$ resistance.)
- Compatible with standard semiconductor processing.

Processing Challenges in TWV.

- Etching of TWV.

  High Density Low Pressure (HDLP) RIE using SF_6 / C_4F_8 chemistry at 15 mTorr.

  Uses alternating etch / passivation process to achieve high aspect ratios.

  Etched 30 µm/side square trenches through 525 um thick wafer.

  Aspect ratio (~ 18: 1), etch rate of 2.2 µm/min ~ 4.5 µm/min.

- Isolation and Metallization of TWV.

  Thermal oxide isolation layer.

  Chemical Vapor Deposition (CVD) of Tungsten or Copper with polysilicon sticking layer.

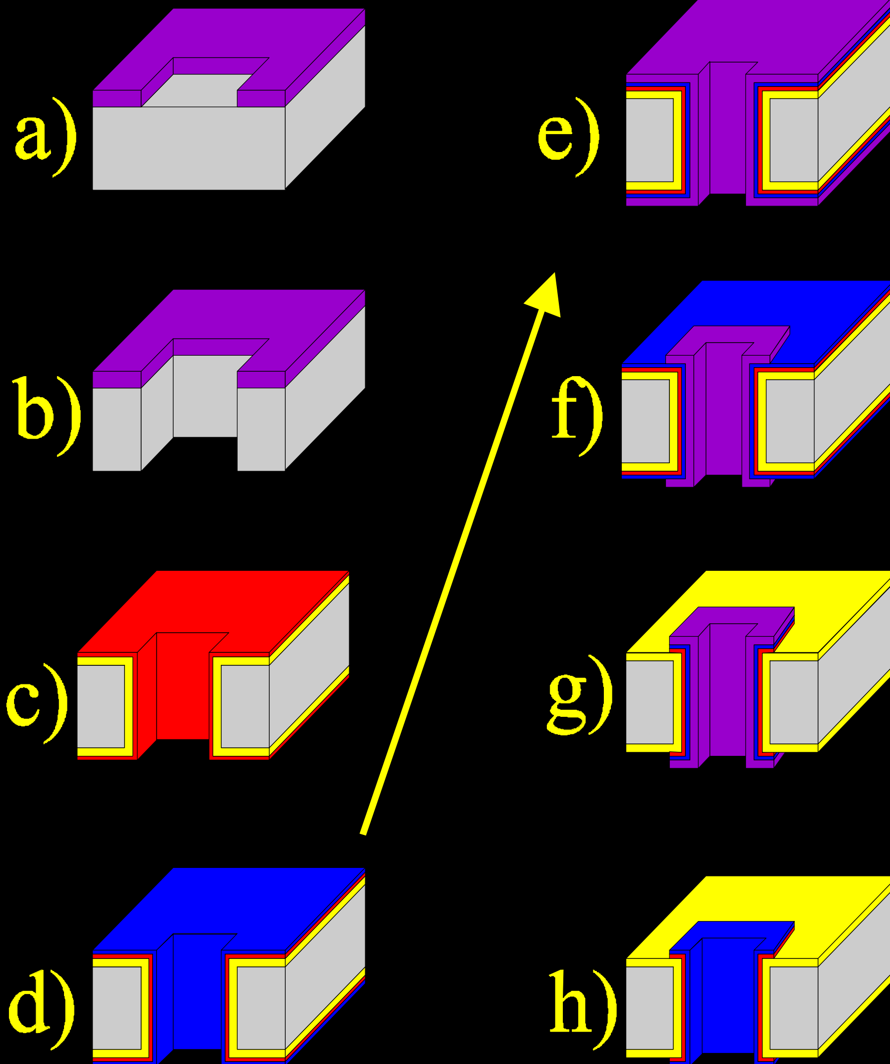
  Conformal electroplating of thick Cu for high conductivity applications.

- Double Sided, Conformal Resist Processing.

  Can not use standard spin on resists to pattern the metal and protect the metallized vias.

  Used Electro-deposited Photoresist for double sided metal patterning.

Process Flow of TWV:



a) Photolithography of thick resist.

b) Through-wafer etching. (HDLP RIE)

c) Thermal oxidation and polysilicon deposition. (LPCVD)

d) CVD metallization (W or Cu) and electro-plating (Cu only).

e) Electro-deposited resist deposition.

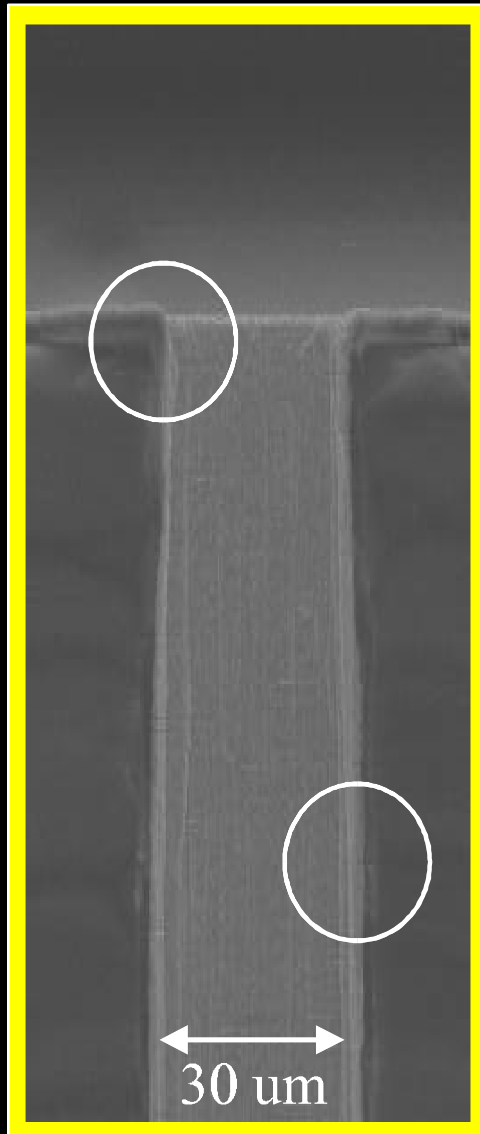
f) Resist patterning by photo lithography.

g) Metal and polysilicon etching.

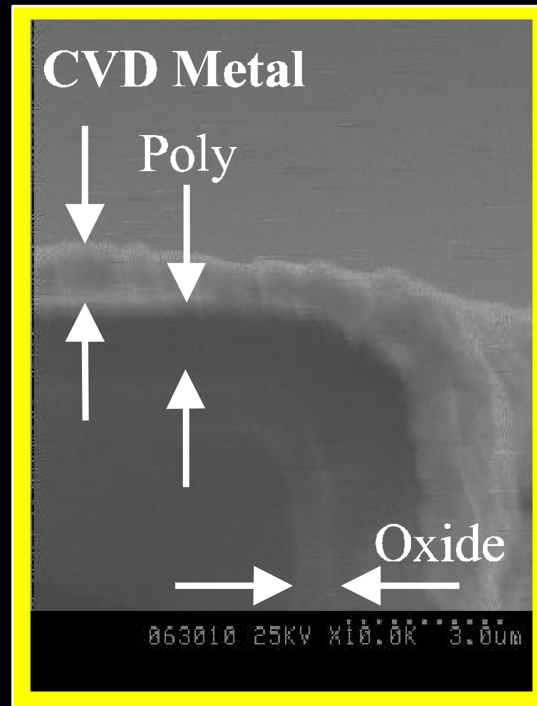
h) photoresist removal.

Quate Group, Stanford University.

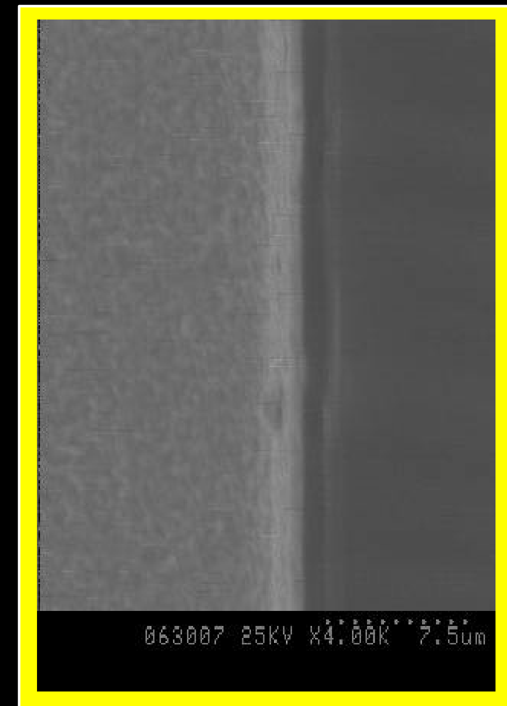
Isolation and Metallization of Deep Trenches



Cross Sectional SEM Micrograph



Top Side



Middle of Wafer

Quate Group, Stanford University.

Double-Sided Lithography using Electro - Deposited Photoresist.

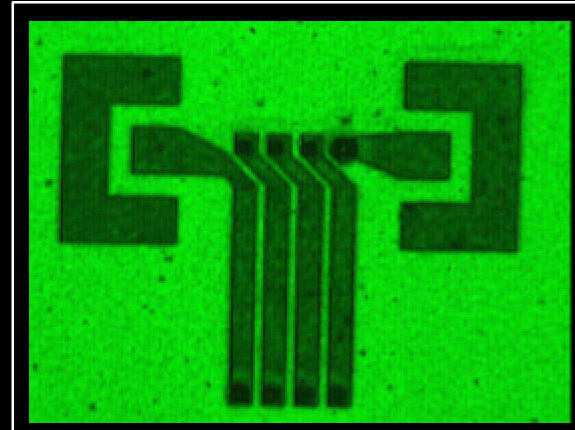
Requirements:

- Double sided patterning of metal layers while protecting the metal in the vias.

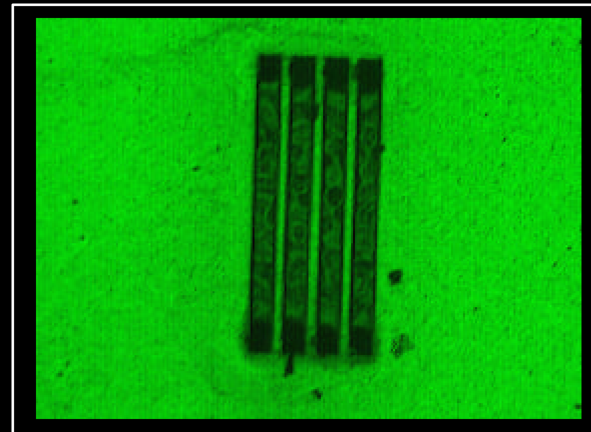
Electro-Deposited Resist:

- Commercially available Shipley PEPR 2400 resist.
- Conformal coating on both sides of the wafer with no spinning.
- Nominal resist thickness of 3 -10 µm, with patterning resolution of ~ 10 µm.
- Adheres well to Cu and W surfaces.
- Capable of protecting the metallized TWVs.

Front Side of Wafer



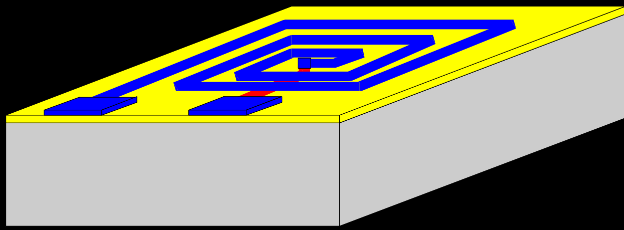
Back Side of Wafer



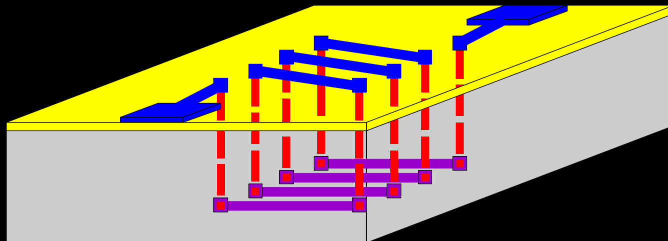
Quate Group, Stanford University.

Application of TWV:
3 Dimensional Integrated Inductors

2 Dimensional Planar Inductor



3 Dimensional Inductor



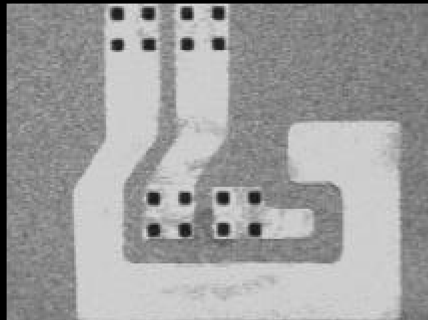
Frequency : 1 - 2 GHz
Inductance: 1 - 10 nH
Quality Factor: 3 - 10

$$Q_{inductor} \propto \frac{w \bullet Lseries}{Rseries}$$

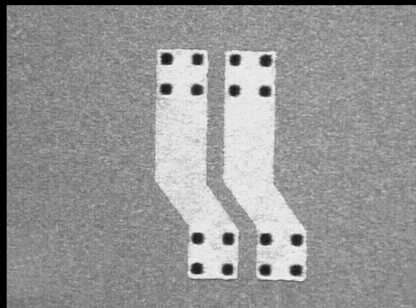
Quate Group, Stanford University.

3 Dimensional Integrated Inductor

Optical Micrographs

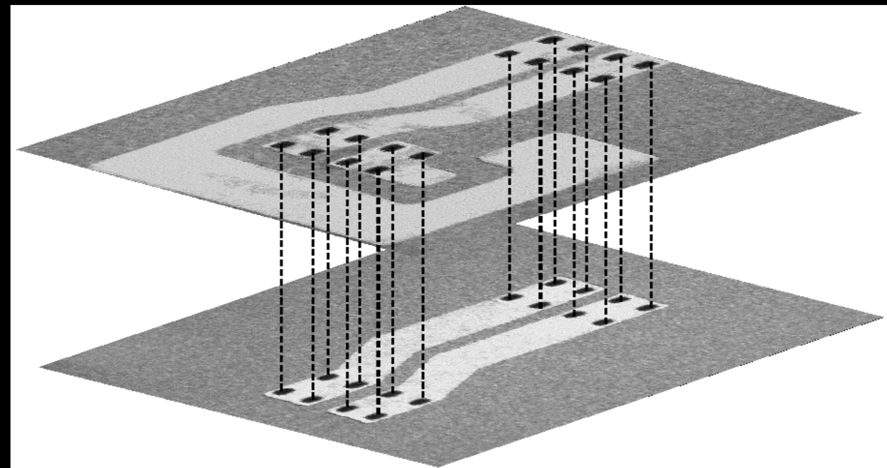


Front side of wafer



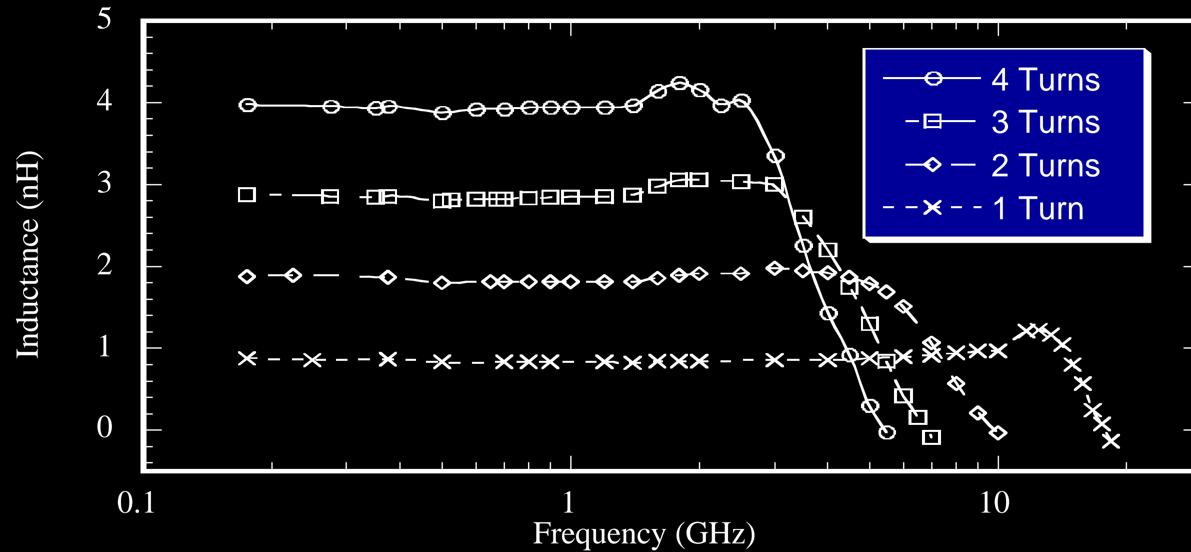
Back side of wafer

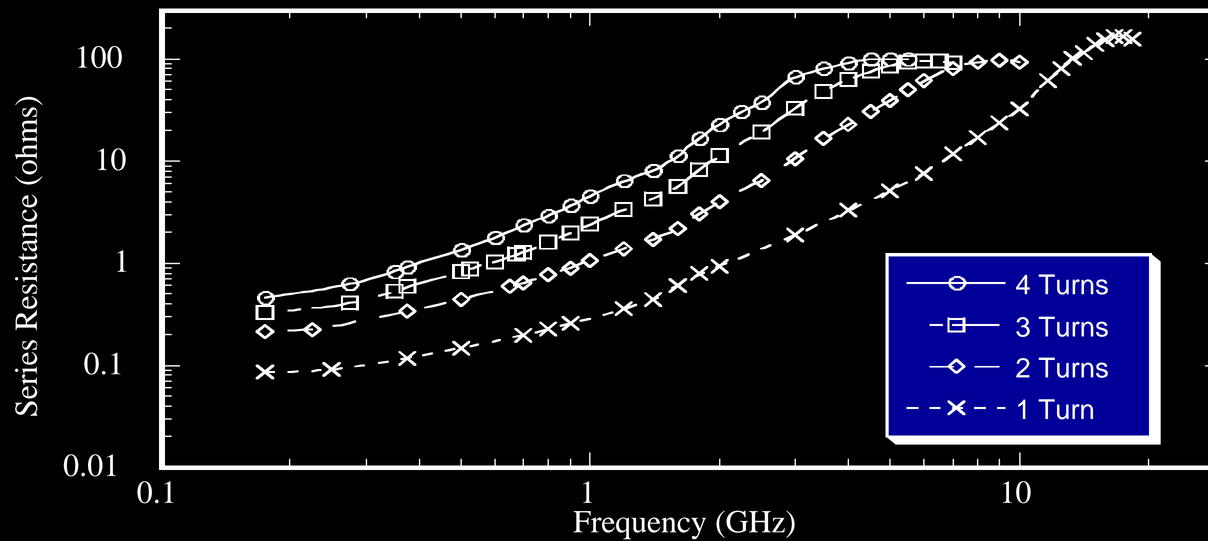
3D Rendering of 2-turn inductor



Quate Group, Stanford University.

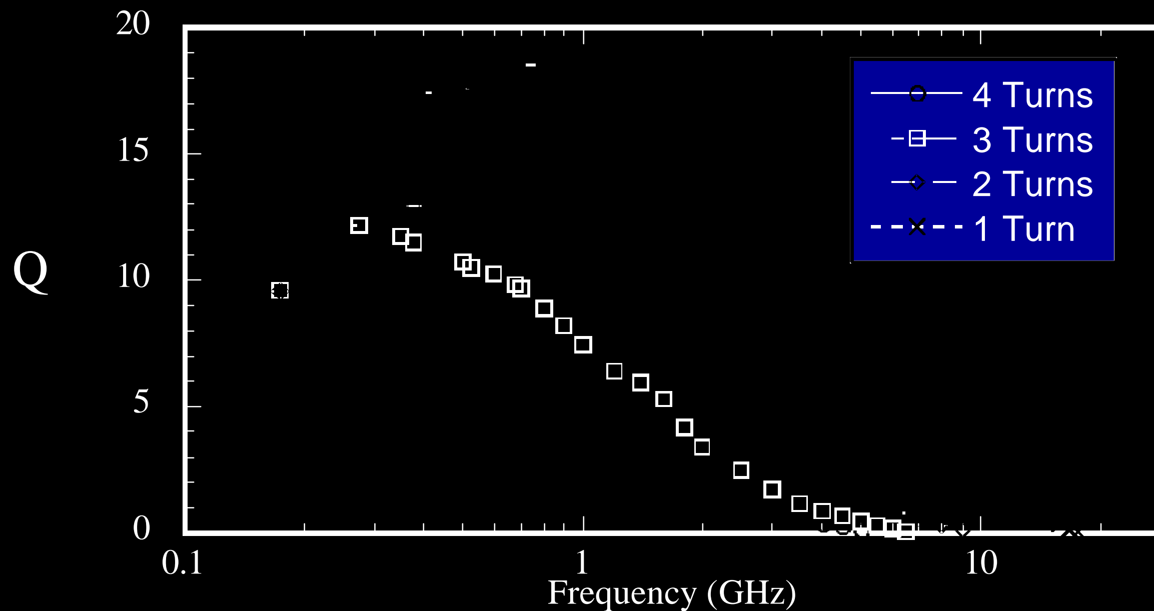
RF Performance of 3D inductors





Quate Group, Stanford University.

RF Performance of 3D inductors



- Q_{max} = 18.5 @ 900 MHz (1 turn inductor)
- Q > 10 @ 300 MHz
- Low series resistance (100 mΩ for 1 turn inductor)
- Performance is limited by the high permitivity and low resistivity of the silicon substrate.

Quate Group, Stanford University.

Conclusions:

- Developed TWV Technology.
  - High Vertical Wiring Density (30 µm via size).
  - Ultra Low Resistance (> 50 mΩ resistance / vertical connection).

- Fabricated Integrated, 3D Inductor on Silicon using TWV Technology.
  - Maximum Q of 18.5 @ 900 MHz.
  - Q > 10 at 300 MHz.

- Future Work.
  - High density packaging by chip stacking.
  - High Q inductors for low frequency applications (micro-NMR).
  - Monolithic packaging of sensors and actuators.

Acknowledgments

• This work was supported by NSF and ONR / JSEP.

• Authors thank V. Malba and C. Harvey at
Lawrence Livermore National Laboratory (LLNL)

• Authors thank Prof. S.S. Wong, and the staff of
Center for Integrated Systems (CIS) at Stanford University.