2

Frequency Response of BJT Amplifiers

This lab will continue our exploration of single-transistor amplifiers using BJTs. We will explore the frequency response of some simple BJT amplifiers, and examine the factors affecting the low- and high-frequency cutoff frequencies in these amplifiers.

Pre-lab Preparation

Before Coming to the Lab

Read through the lab experiment to familiarize yourself with the components. Before coming to the lab, each group should obtain a parts kit from the ECE Shop and assemble your circuit.

Parts List

Use parts from Lab #1 plus a 2N3904 NPN transistor and a 2N3906 PNP transistor.

In-Lab Procedure

3.1 Common-Emitter Amplifier

Figure 3-1 shows an AC-coupled common-emitter amplifier, similar to the CS amplifiers from the previous lab. We will use this circuit to explore the frequency response of the CE/CS amplifier topology. Since the circuit has a rather high gain, we have included a resistor divider network at the input to keep the input signal small.

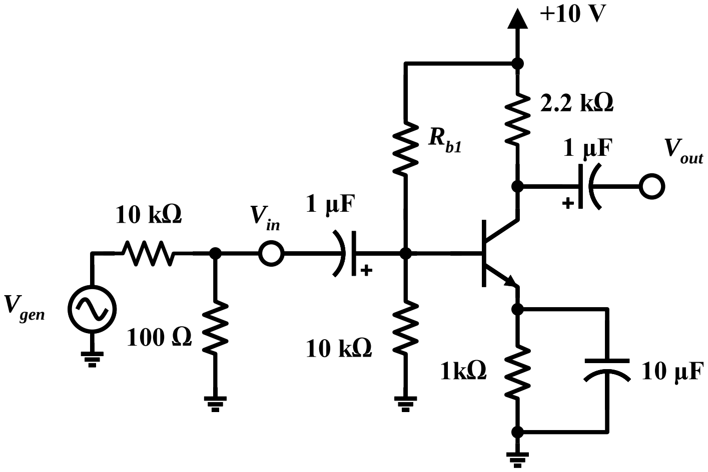

Figure 3-1 – Common-emitter amplifier (with input divider).

- ☐ Using a 2N3904 in the circuit of Figure 3-1, first calculate the base resistance R_{b1} that is needed to bias the device at a collector voltage of $V_c \approx 6-7\,\mathrm{V}$. Assume a nominal value of $\beta \approx 200$ for this calculation (document your work in your lab report).
- ☐ Build the circuit using your calculated value of R_{b1}, and record the DC voltage at the collector, base, and emitter. From these measurements, estimate the collector current I_c, and transconductance g_m.

Low-Frequency Response

- ☐ Adjust the function generator for a 0.1 V amplitude sinewave at 10 kHz and apply to the circuit using the voltage divider shown. Record the waveforms at the points V_{in} and V_{out}, and compute the gain of the amplifier circuit $A_{vo} = V_{out}/V_{in}$. This is the mid-band gain of the amplifier.

Note: it may be hard to see V_{in} directly on the scope since it is a small signal. If so, using signal averaging on the oscilloscope may help. Another alternative is to temporarily increase the input signal until V_{in} is easily measurable and the step-down ratio of the input voltage divider can be determined accurately (for example, in Figure 3-1 the input divider reduces the input signal by a factor of 100 nominally). From that point on you can just observe V_{gen} on the scope and apply your measured scaling factor to indirectly determine V_{in}.

- ☐ From the measured gain, estimate the transconductance and compare with the value determined from DC measurements.
- ☐ Slowly decrease the frequency until the output signal reduces by -3dB ($1/\sqrt{2}$ of its original value). This is the low-frequency cutoff, f_L.
- ☐ Reduce the frequency to $f_L/10$ and measure the gain again. Repeat for $f_L/100$.
- ☐ The pole at f_L is due primarily to the RC time-constant associated with the emitter bypass capacitor. Verify this by replacing the 10µF bypass capacitor by a 100µF capacitor and repeating the last two steps.

In your lab report, compare your measurements of the low-frequency cutoff against the theoretical value.

High-Frequency Response

Now, replace the 10μF bypass capacitor and return the function generator to a 0.1V sinewave at 10kHz.

☐ Increase the frequency to find the high-frequency -3dB cutoff of the amplifier, f_H.

As we learned in class, the upper cutoff is determined by the RC time-constant formed by the internal capacitances of the transistor and the surrounding resistances. We can demonstrate this as follows.

☐ Simulate the effect of increasing C_{be} and C_{bc} by adding an external capacitance between the base and emitter. Add a 0.01uF ceramic capacitor in this way, and re-measure the high-frequency cutoff.
☐ Also measure the gain for $f = 10 f_H$ in this case.

In your lab report, use the measured data to create a Bode plot of the gain-frequency response of the amplifier in Figure 3-1.

3.2 Common-Base Amplifier

The basic circuit is shown in Figure 3-2 and is quite similar to the common-gate circuit from the previous lab. Here we have simplified the topology to eliminate the AC input/output coupling capacitors, and included a voltage divider at the input to keep the drive signal small.

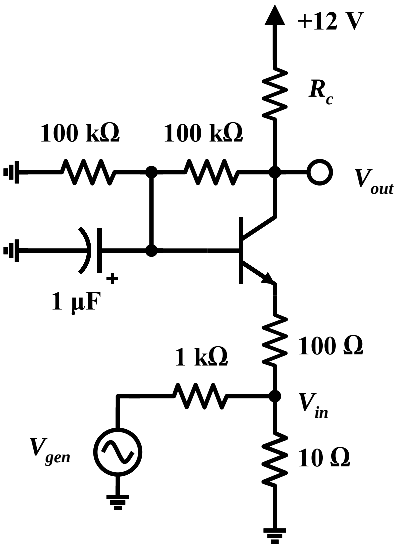

Figure 3-2 – CB amp.

☐ First assemble the circuit using a collector resistor of $R_c = 2.2\,\text{k}\Omega$, as in the CE amplifier. Note the supply voltage is now +12V.
☐ Apply a 1V amplitude sinewave at 10kHz. Observe and record the waveforms at the V_{in} and V_{out} nodes (use AC coupling on the oscilloscope) and from this information calculate the mid-band gain.

Note that we could increase the gain by adding a bypass across the 100Ω emitter resistor, but we have left that out here to simplify the analysis.

Low-Frequency Response

☐ Reduce the frequency to find the low-frequency cutoff f_L. Verify that this is due to the bypass capacitor at the base by increasing this capacitor and re-measuring the low-frequency cutoff. Record your results.

High-Frequency Response

As discussed in the text and lecture, the common-base/common-gate topology has an inherently high cutoff frequency relative to the CE stage.

□ Increase the frequency and try to find the high-frequency -3dB cutoff of the amplifier, f_H. If the function generator doesn't have the frequency range to find this frequency, state this in your report.

□ Simulate the effect of increasing C_{be} and C_{bc} by adding an external capacitance between the base and emitter. Add a 0.01uF ceramic capacitor in this way, and re-measure the high-frequency cutoff if you can.

To see that the internal capacitances impose a limit on the gain-bandwidth product of the amplifier, let's increase the gain and observe the effect on the frequency response:

□ Remove the external capacitance you added in the previous step and increase the gain by changing the collector resistor to $R_c = 10\,\mathrm{k}\Omega$.

□ Now re-measure the mid-band gain at 10kHz and find new high-frequency cutoff.

□ Repeat the last step with the 0.01uF external base-emitter capacitance.

In your lab report, use your measured data to sketch a Bode plot for the common-base amplifier, and compare with theoretical values for mid-band gain and cutoff frequencies.

3.3 Multi-Stage Amplifier Example

The circuit in Figure 3-3 is a cascade of two common-emitter stages, one with an NPN device and the second using a PNP (2N3906) device. Cascading gain stages has the advantage of increased gain, but comes at the expense of a decreased bandwidth, as you will see firsthand below.

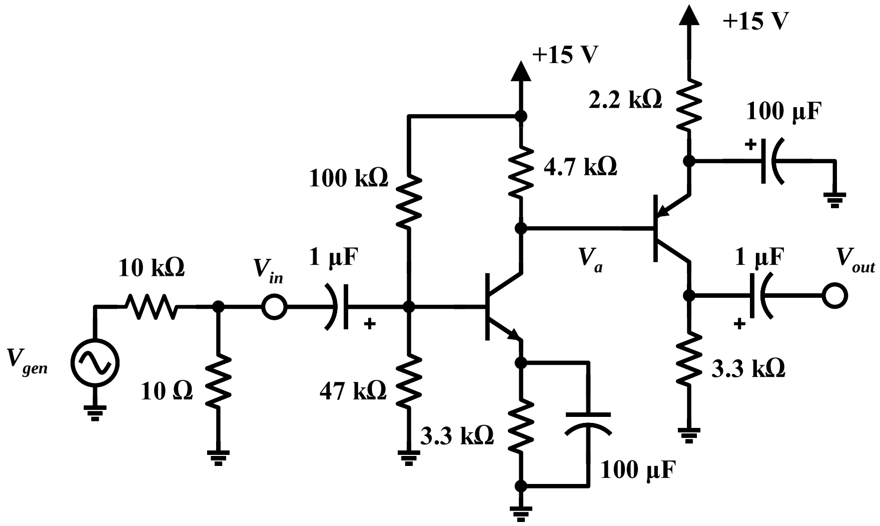

Figure 3-3 – Two-stage amplifier.

- □ Construct the circuit in circuit Figure 3-3. Note the supply voltage has been increased to 15 V. Measure and record the mid-band AC voltage gain $A_{vo} = V_{out} / V_{in}$ with a generator signal of 0.1V sinusoid at 10kHz. It may be difficult to see V_{in} on your oscilloscope because of the large step-down ratio of the voltage divider at the input (nominally a divide-by-1000). If so, increase the input signal briefly to establish the actual voltage division ratio, then use this information to calculate the V_{in} for a 0.1V generator input.
- □ Decrease the frequency to find the low-frequency cutoff, f_L. Record this and then reduce the frequency to $f_L/10$ and measure the gain again. Repeat for $f_L/100$. Can you explain your results?
- □ Now increase the frequency to find the high-frequency cutoff, f_H. Record this and then increase the frequency to $10 f_H$ and measure the gain again. Repeat for $100 f_H$ (if the function generator permits). Can you explain your results?

In your lab report, use your measured data to sketch a Bode plot for the gain-frequency response of this amplifier. Compare your results with the expected gain and cutoff frequencies.

Congratulations!
You have now completed Lab 2