Importance of Source and Drain Resistance to the Maximum $f_T$ of Millimeter-Wave MODFET’s

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Abstract—The usual approximate expression for measured $f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$ is inadequate. At low drain voltages just beyond the knee of the DC I-V curves, where intrinsic $f_T$ is a maximum for millimeter-wave MODFET’s, the high values of $C_{gs}$ and $C_{gd}$ combine with the high $g_m$ to make terms involving the source and drain resistance significant. It is shown that these resistances can degrade the measured $f_T$ of a 0.30-$\mu$m GaAs/AlGaAs MODFET from an intrinsic maximum $f_T$ value of 73 GHz to a measured maximum value of 59 GHz. The correct extraction of maximum $f_T$ is essential for determining electron velocity and optimizing low-noise performance.

Source and drain parasitic resistances ($R_s$ and $R_d$) are not usually expected to affect measured $f_T$. This assumption is not true at low drain voltages just beyond the knee of the dc I-V curves where intrinsic $f_T$ is a maximum. A typical example is shown in Fig. 1, where the measured extrinsic $f_T$ and the de-embedded intrinsic $f_T$ are plotted versus drain voltage for a 0.3 × 120-$\mu$m double-doped quantum-well AlGaAs/GaAs MODFET, similar to that reported by Hueschen et al. [1]. The MODFET $f_T$ data were extracted from S-parameters measured on-wafer at 5 GHz using a calibrated (Cascade Microtech Impedance Standard Substrate (ISS) HP8510 network analyzer with Cascade Microtech microwave probes [2]. The measured S-parameters were corrected for the 6-IF pad capacitance and then the extrinsic $f_T$ was extrapolated assuming a −20-dB/decade roll-off for the short-circuit current gain $|h_{21}|$ [2]. The intrinsic $f_T$ was extrapolated in a similar manner after first de-embedding the effect of the parasitic resistors from the measured S-parameters [3]–[5]. A maximum measured $f_T$ of 59 GHz is observed at a drain voltage of 1.1 V. After de-embedding the parasitics the maximum intrinsic $f_T$ is higher: 73 GHz. This value occurred at the lower drain voltage of 0.7 V where the extrinsic value was only 51 GHz.

The usual approximate expression for measured $f_T$ is generally assumed to be the intrinsic expression:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

which does not include $R_s$ and $R_d$ terms [6], [7], since at first inspection, impedances in series with the input and output ports only affect voltage, not current. Even though $R_s$ makes the extrinsic $g_m$ smaller than the intrinsic $g_m$ by a factor of $1/(1 + g_m/R_s)$, it also decreases $C_{gs}$ by the same factor and so should not affect $f_T$.

A more rigorous derivation for the short-circuit current gain of a FET [8] gave a better approximate expression for the extrinsic $f_T$:

$$f_T = \frac{g_m/(2\cdot\pi)}{[C_{gs} + C_{gd}] \cdot [1 + (R_s + R_d)/R_{ds}] + C_{gd} \cdot g_m \cdot (R_s + R_d)^2}$$

(2)

The additional terms in (2) can be explained as follows. Although the drain is effectively shorted to the source when calculating $h_{21}$, in the presence of $R_s$ and $R_d$, all of the current from $g_m$ does not pass through this current path; some flows through $R_{ds}$. The resulting resistive divider effect reduces the measured current gain by the factor $(1 + (R_s + R_d)/R_{ds})$. Also, the voltage drop across $C_{gd}$ is now larger than that across $C_{gs}$ because of the IR voltage developed across $R_s$ and $R_d$. The resulting Miller effect increases the effective output capacitance by a factor of $(1 + \frac{g_m}{R_s})$ where $R = (R_s + R_d)/(1 + (R_s + R_d)/R_{ds})$. These effects are shown schematically in Fig. 2.

Because $g_m$, $C_{gs}$, $C_{gd}$, and $R_{ds}$ are strong functions of bias (see Fig. 3 and 4), the discrepancies between the $f_T$’s predicted by (1) and (2) vary with drain bias as demonstrated in Fig. 1. As the drain voltage increases, $C_{gd}$ decreases and $C_{gs}$ increases while the total gate capacitance ($C_{gs} + C_{gd}$) is approximately constant (see Fig. 3). The intrinsic $f_T$, therefore, follows the behavior of $g_m$, which increases rapidly with increasing drain voltage reaching a maximum at approximately the knee voltage of the dc I-V curves (0.7 V; see Figs. 1 and 4). This value of $V_{ds}$ further decreases to 0.5 V after the dc correction for $I_{ds}$ ($R_s + R_d$), the maximum intrinsic $g_m$ and $f_T$ occurring just when the drain voltage is sufficient to saturate the electron velocity.
Since the intrinsic $g_m$ and $f_T$ reach their maximum value before $C_{gs}$ and $G_{ds}(1/R_{ds})$ reach their low saturated values, the effect of $R_t$ and $R_d$ on extrinsic $f_T$ dominates at this bias condition. For example, in this MODFET, when biased at maximum intrinsic $f_T$, $R_{ds}\cdot Z$ is only 5.1 Ω·mm compared to 1.2 Ω·mm for $R_t + R_d$; therefore the resistor divider effect reduces the extrinsic $f_T$ by 18 percent. At the same bias $C_{gs}$ is 23 percent of the total gate capacitance; therefore the Miller effect also reduced the extrinsic $f_T$ by 15 percent. The measured $f_T$ of 53 GHz is thus 30 percent lower than the intrinsic $f_T$ value of 73 GHz at $V_{DS}$ of 0.7 V. The correct interpretation of MODFET performance at maximum $f_T$ is required for correctly extracting electron velocity and optimizing low-noise performance. Note that it is easy to overestimate $R_t$ and $R_d$ during extraction which can lead to an overestimation of the intrinsic $f_T$.

The ratio of the parasitic delays to the transit delay is

$$\tau_{p} = g_m(R_s + R_d) \left[ \frac{G_{ds}}{g_m} + \frac{1}{1 + C_{gs}/C_{ed}} \right].$$  (4)

The resistor divider and Miller capacitance terms in (4) are plotted in Fig. 5. At maximum intrinsic $f_T$ these terms are 0.23 and 0.18, respectively. Charging delays of GaAs MESFET's biased in the saturated region are not significant and have traditionally been ignored. However, charging delays in short gate length MODFET's biased for maximum $f_T$ cannot be ignored until the parasitics are reduced in proportion to the reduction in intrinsic transit times. This point was recently made by Nguyen et al. [9] who attributed some of the high $f_T$ of 150 GHz for a 0.15-µm 25-percent indium pseudomorphic MODFET to reduced parasitic resistances.

At the low drain bias required for maximum intrinsic $f_T$, the ratios $g_m/G_{ds}$ and $C_{gs}/C_{ed}$ are both approximately 3 for this
MODFET. Since similar ratios have been measured on other MODFET’s and are expected to hold for most FET structures, the parasitic delays can only be reduced at low drain voltages by reducing the $g_m \cdot (R_s + R_d)$ term. For the parasitic delay to be less than 20 percent of the total delay the $g_m \cdot (R_s + R_d)$ product, $F$, has to be less than 0.4. This term is relatively large (0.8) for this and many other short gate length FET’s compared to the more familiar longer gate length MESFET’s because $g_m$ is higher. A higher $g_m$ is necessary for high $f_T$ because $C_{gs}/Z$ has to be approximately 1 pF/mm for fringing capacitance and aspect ratio considerations. To maintain a low $g_m \cdot (R_s + R_d)$ factor $R_s + R_d$ has to be reduced in proportion to the $g_m$ increase. A rule of thumb can be made for scaling $R_s + R_d$ by assuming the saturated velocity FET model:

$$
(R_s + R_d)Z = \frac{F}{g_m/Z} \cdot \frac{F}{2\pi f_T C_{gs}/Z} = \frac{FL_e}{\nu_s C_{gs}/Z}
$$

$$
= R_p L_e (\mu m) \Omega \cdot mm
$$

(5)

$$
F = g_m (R_s + R_d)
$$

(6)

where $L_e$ is the gate length and $\nu_s$ is the saturation velocity. For example, assume $F = 0.4$, $C_{gs}/Z = 1$ pF/mm, and $\nu_s = 2 \times 10^7$ cm/s; then $R_p = 2 \Omega \cdot mm$. This suggests that $(R_s + R_d)$ should be 2 $\Omega$ mm for a 1 $\mu$m gate length FET, and 0.66 $\Omega$ mm for a 0.3 $\mu$m FET instead of the 1.2 $\Omega$ mm reported here. In the MODFET reported here parasitic delay is 29 percent of the total delay.

**Conclusion**

De-embedding the microwave measurements from $R_s$ and $R_d$ was shown to both increase the maximum value of $f_T$ and decrease the drain voltage at the maximum. The usual approximate expression for $f_T$ is inadequate at low drain voltages just beyond the knee of the dc $I-V$ curves where intrinsic $f_T$ is a maximum. $R_s$ and $R_d$ have a significant effect on extrinsic $f_T$ at this bias condition because $R_{ds}$ is only a few times greater than $R_s + R_d$ and $C_{gd} \cdot g_m \cdot (R_s + R_d)$ is a substantial fraction of total gate capacitance. When MODFET’s are made with short gate lengths and improved material systems [9]-[11], the parasitic resistances should be decreased in proportion to the increase of $g_m$ to see all the increase in the intrinsic $f_T$.

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**References**


