FET Amplifier Design Project
Lab Project #3
UCSB/ECE218A
Winter 2007

Report will be due on March 16, Friday. Check sheet (verified by TA or Prof) must be turned in at the same time as the lab report.

Goals:
- Design, construction and evaluation of a 1.4 GHz low noise amplifier using the NE34018 Gallium Arsenide HJ-FET.
- Introduction to stabilization of amplifiers, biasing, and design for noise, gain and frequency

Reading: Notes set #5-9, Biasing notes, and ADS tutorials on Stability and Gain Circles and Noise Figure Analysis, PCB Layout information for Lab 3.
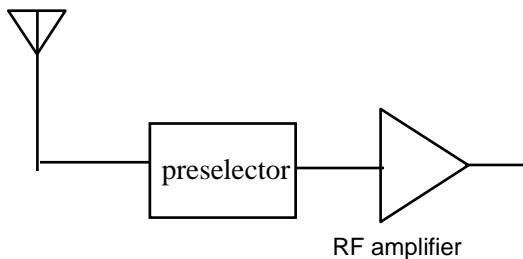
Safety Precautions:
> Ensure that your circuit is dc blocked before connecting to the spectrum analyzer, network analyzer, or other test equipment.
>
> The NE34018 is static sensitive. Observe handling precautions such as wrist strap, anti-static mat, and attaching part to circuit when other soldering is completed.

Background:

Bandpass RF amplifiers are often used in receiver front ends to improve sensitivity and noise performance. You will be designing this amplifier for the minimum noise figure while guaranteeing unconditional stability for any possible source or load impedance. You should obtain good return loss (< -10 dB) at the output.

RF amplifier

Specifications

S22	Better than –10dB @ min. NF frequency
Gain	> 15 dB @ min. NF frequency
Frequency	Min. NF @ 1.4 GHz +/- 100 MHz
Noise Figure	Maximum of 1.6 dB
Power Supplies	+ 3.5 volts; - 2.5 volts

Design Procedure: Complete HW #5 before building the amp!!!!

Design an amplifier at 1.4 GHz based on the NE34018 GaAs HJ-FET. You will find a data sheet on the web site. Bias the device with $V_{DS} = 2.0V$ and $I_D = 10$ mA. Note that this device is bilateral and potentially unstable over a wide range of frequencies.

Both an S-parameter model file (with noise parameters) and a nonlinear large signal model are provided on the web site because the ADS component library does not contain models for the NE34018. Refer to the comments at the end of this lab for more information on how to insert an S2P file in your design and how to create a subnetwork symbol for insertion in your schematic.

Type of file	File name	Where to put it	Useful freq. range
S parameter	NE34018C.s2p For VDS = 2V ID = 10 mA	ADS project data folder	500 MHz – 10 GHz (900 M – 4G for noise)
Large signal	NE34018_subnet.dsn	networks folder	DC – 6 GHz

(a) Use Agilent ADS to plot source and load stability circles for the NE34018. Simulate the device using the S parameter mode of simulation. You will see that the device is unstable over a wide range of frequencies (k < 1). Modify the design by adding some stabilization element(s) so that the device is unconditionally stable at the design frequency. (Refer to the Stability and Gain Circles tutorial) While it would be possible to match the device for maximum available gain, you may find that this leads to source or load impedances very close to the stability circle. It will be safer to back off on the gain to allow for more stability and a less sensitive design.

(b) Note that the device is bilateral. Determine Γ_S and Γ_L with power gain circles. Design the matching networks (**YOU MUST HAVE A DC BLOCKING CAPACITOR AT BOTH INPUT AND OUTPUT!!!!!**). Simulate again with the matching networks and verify that the gain, frequency for minimum noise figure, bandwidth and output return loss (|S22| in dB) meet or exceed specifications. You need to consider the non-ideality of your components with appropriate models in order to be successful in having your design work the first time. You should use the microstrip transmission line models described below to improve accuracy. If chip inductors are used, there are equivalent circuit models on the course web page for the 0603 Coilcraft chip inductors. There is a limited supply of these in the lab in a sample kit –use sparingly.

(c) Next you must decide how to introduce bias to the device. You may be able to use the matching networks, or you might want to consider a quarter wave high Z line. Use an active biasing approach to guarantee a stable bias point over supply variation, device variation and temperature. Refer to the bias circuit notes for examples. You will find some components in your parts kit for this purpose.

(d) Make sure that the out-of-band behavior of the matching networks does not put the device into an unstable region on the source or load planes. Verify that the device will be stable over a wide frequency range (10 MHz to 5 GHz. Use the large signal model below 500 MHz.) You should consider adding some additional stabilization element that provides resistive loading at low frequencies but not at high if stability at low frequencies is a problem. (Hint: a resistor in series with a shunt leg or in parallel with a series capacitor of the matching network can be effective at damping low frequency instabilities).

(e) Now, resimulate the entire amplifier using the nonlinear model for the NE34018, found on the course web page. This is a subnetwork ADS file. You can copy it into the networks directory of your project. Place it into the circuit using the components library > Subnetworks. Predict the 1 dB compression point through harmonic balance simulation.

Constructing the amplifier PCB:
We will be fabricating custom PC boards for lab 3 through the internet PCB vendor, ExpressPCB. Please read the instructions on PCB Layout for Lab 3. The boards are subject to the following restriction:

- The PCB dimensions must be 2 x 2.5 inches.
- Board material is FR-4. You should assume $\varepsilon_r = 4.5$.

You can access the layout software on the PCs in 5162 or ECI. Or you can download the software onto your own PC. In either case, visit http://www.expresspcb.com for an orientation on their layout software and board specifications. If you use your own PC, then you must also download the component footprint for the NE34018 that is found on the course website. Copy this file into the following directory:
        Programs\ExpressPCB\PCBComponents_Custom

When your layout is ready to submit, carefully check it against your schematic. Then email the .pcb file to: long@ece.ucsb.edu. I will submit all of the layouts for the class in one batch.
THE BOARD LAYOUTS ARE DUE BY 9 AM ON Monday, MARCH 5.

Build the amplifier. The NE34018 is static sensitive, so you should solder the device onto the board after you have assembled the rest of the circuit. Temporarily short the V_{DD} and V_{GG} connections to the ground plane while installing the device.

Testing the Amplifier

Measure your amplifier's performance to verify that your design meets specs. Compare measured with simulated performance. Demonstrate operation to the TA or Prof.

1. Set bias. Terminate input and output with a 50 ohm load or an attenuator, apply VGG first, then VDD to the amplifier, and set the bias current and drain voltage using the variable resistors. Before applying power, set R4 so that the FET will be in cutoff. Apply power and slowly increase VGS until the required drain current is obtained. Report the VDS, VGS and ID.

2. You must first verify that the amplifier is stable with 50 ohm source and load. Connect the amplifier output to the spectrum analyzer and the input to a signal generator. Adjust the analyzer for a span of approximately 1 MHz to 5 GHz. You should see no indication of output on the SA at any frequency when the generator is off, and only an output at 1.4 GHz when the generator is on.

3. Next determine:
   1. Gain and Input/Output Return Loss. (Make sure that the power level setting on the NA is small – well below the P_{1dB} input power[1]. P_{1dB} may be somewhere around -20 dBm.) Plot S_{11}, S_{12}, S_{21}, and S_{22} over the frequency range from 0.5 to 2 GHz
   2. Measure noise figure of the amplifier. Determine the frequency for minimum NF.
   3. Measure the input P_{1db} compression power at the frequency that gives you minimum NF. Plot Pout vs Pin.
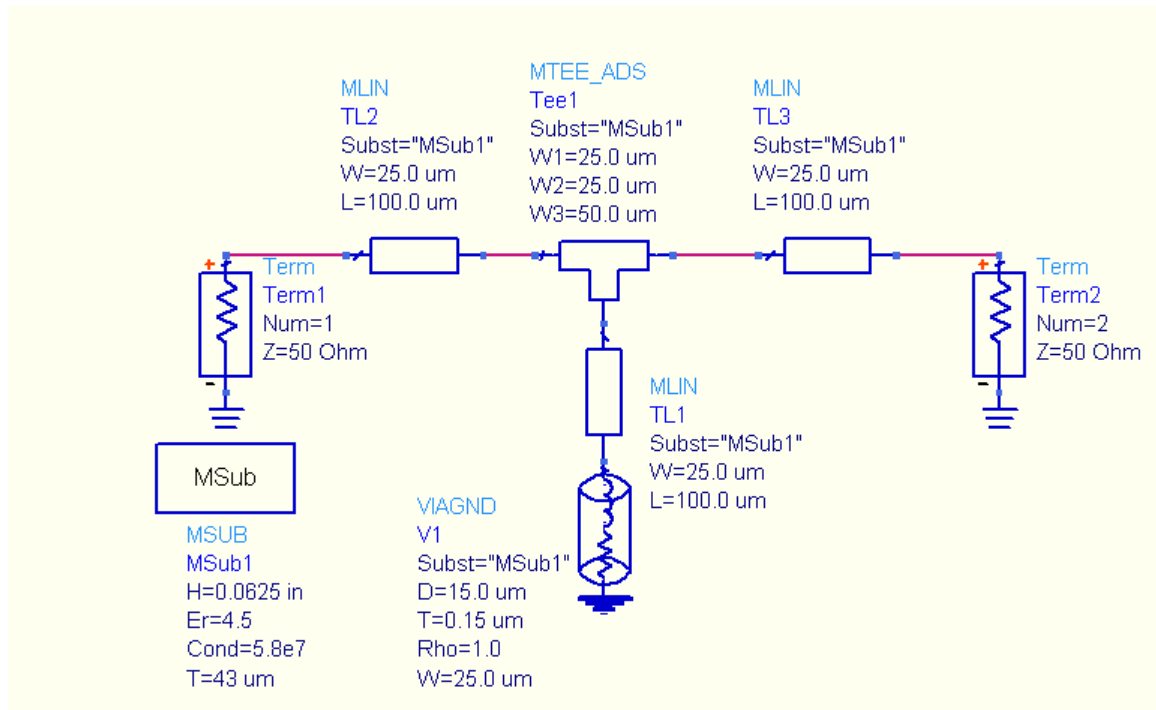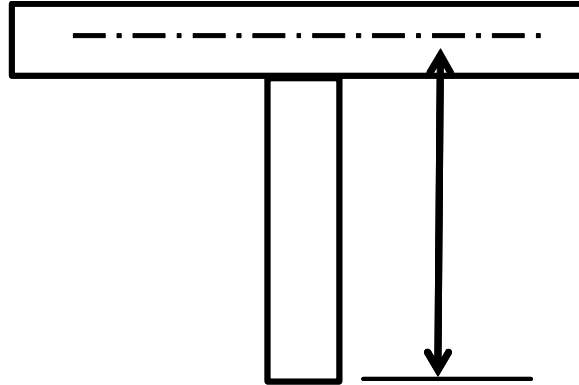   4. Measure DC power dissipation of your amplifier.

Active Bias Circuit (see Bias Circuit Design notes for details – matching network shown is just an illustration – not intended to necessarily be appropriate for the Lab 3 design). R2, R3 should be leaded resistors. R1 and R4 are trimmer pots. C1, C2 are tantalum polarized capacitors. They are used to provide a good ac ground at low frequencies for the bias circuit. Observe the polarity when installing. C3 – C5 are RF bypass capacitors.

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[1] The 1 dB compression power is usually specified as the power level at the input of the amplifier which compresses the transducer power gain by 1 dB.

C1

C3

Matching network

DC block

V_{DD}

R1

R3

VDS

D1

I_D

C5

GaAs FET, M1

V1

Q2

R2

R4

I_{C2}

V3

-V_{GG}

Matching network

C4

C2

AC Bypass cap

+

2N3904

TO-92

c
B
E

Same for 2N3906

Microstrip line modeling in ADS.

You have used the ideal transmission line TLIN and open and shorted stubs in the homework assignments. You should be aware that there is a more accurate set of microstrip line models and elements in another menu (TLines-Microstrip) and palette. These elements take into account some of the nonidealities of the line: corners, tees, and losses. Msub is used to describe the line and dielectric. MLIN is a series line section. MLOC is an open circuit stub; MLSC is a short circuit stub. Mcorn represents a right angle corner without a miter bend. MBend represents a mitered corner. MTEE is a T junction. There are also models for PCB via holes that should be used to model ground connections.

Note that the length of the stub is measured from the center of the transmission line at the T junction.
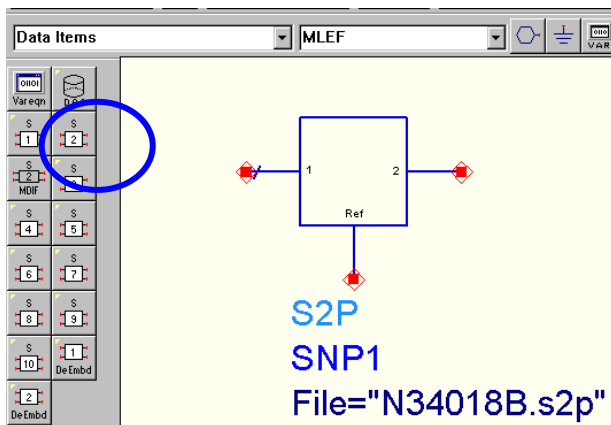

You should use models such as these when simulating the final version of your circuit.

Representing devices as an S2P file

In the case of the NE34018, the ADS component library does not contain a set of S parameters for the device. Instead, we can use an S2P file provided by NEC. The file for our device was measured at the VDS = 2V; ID = 10 mA bias point. An S2P file is simply a tab delimited ASCII text file containing S parameters measured on a 2 port device. The format is:

Frequency   S11   S21   S12   S22
In GHz   mag   ang   mag   ang   mag   ang   mag ang

Place an S2P block from the Data Items menu and identify the file name. ADS will look for the file in the ADS project's data directory.

Creating a schematic symbol for the NE34018 large signal model:

You should have copied the file NE34018.dsn into your networks directory on the ADS project. This file is in the form of a subnetwork. Pads have been assigned to the source, gate, and drain. While the entire file could be copied into your amplifier network, it is more convenient to represent it with a symbol. To do this follow these instructions after opening the NE34018 schematic:

1. Create Subnetwork symbol:
   View > Create/Edit Schematic Symbol
   The Symbol Generator panel opens up. The default symbol shown below should appear.
   > [You could select an alternate symbol if you click on the *Copy/Modify* Tab There is a library of symbols already available. But, you will need to be careful that it assigns the pads to the expected symbol ports.]
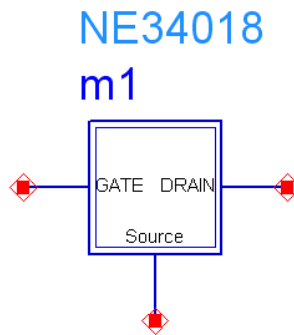
   To return to the schematic, choose *View > Create/Edit Schematic Symbol* (again) Save the file.

2. Name the subcircuit and set the design parameters

File > Design Parameters

General tab.   The component name will be shown, X in this example. Name the component instance something else, such as M. When the component is included in a schematic, each instance will be numbered sequentially. There are no design parameters that should be accessible from outside the symbol, so just close the panel.

3. To insert the NE34018 into the circuit, open the components panel, click on subnetworks, and the file name should be present. Click on NE34018, then return to the schematic. You can insert it just by clicking on the schematic. It should look like this:

Parts List – ECE218A, Lab3   Winter 2007:
1	SMA female board-mounted connector
1	SMA male board-mounted connector
1	NE 34018 surface mount transistor
2	2N3906 PNP BJT
1	2k Bourns 3386P potentiometer
1	5k Bourns 3386P potentiometer
2	4.7 uF Tantalum capacitor
2	0.47 uH RF choke
3	24" lengths of insulated wire (#24) for power supply connections

Checkout Sheet for Lab 3

You must demonstrate to the TA or Prof. the following:
1.   Device is biased to 2V; 10 mA
2.   Demonstrate stability with spectrum analyzer from 10 MHz to 1.8 GHz with the generator RF on and off.
3.   Zoom in on the output and verify that there are no sidebands.
4.   Demonstrate gain and noise figure specs are met at design frequency
5.   Demonstrate that S22 also meets spec at design frequency.