GaAs HBT RFIC Design Project
Design Project #1 Spring 2008
UCSB/ECE218B

This project is available to lab groups which have at least one group member willing to test the chip in the summer or fall quarter. 2 units can be given as ECE596 for this work. This is a very challenging but rewarding project that will require a lot of independent thinking. Get started right away.

Objective:

Design and layout a fully integrated RFIC image-rejecting (SSB) mixer. The mixer can be a double-balanced Gilbert configured with single-ended IF and LO inputs and RF output. To make this more interesting, the mixer will be designed as a SSB image reject upconverter with 1.2 GHz output frequency (USB). The IF input frequency will be 144 MHz.

Specifications for the design:

RF output frequency (USB)	1.2 GHz
IF input frequency	144 MHz
Pout @ 1 dB compression level	0 dBm
Conversion Gain (P_{RF}/P_{AVS_IF})	At least 15 dB
Image Rejection Ratio (IRR)	At least 25 dB

The effectiveness of the designs will be compared using the following figure of merit:

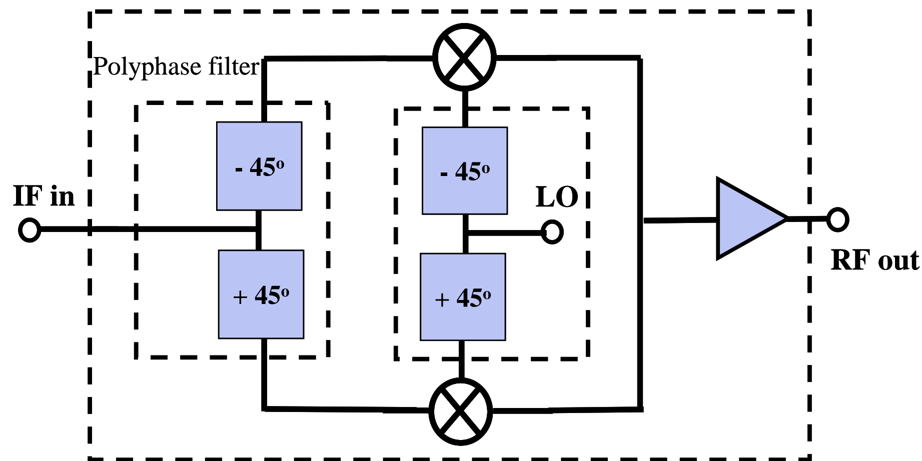
$$FOM = OIP3(dBm) - 10\log P_{DC}$$

Reading:

1. Triquint Semiconductor Design Manual: TQHBT3 process
2. Quadrature Mixing (course webpage)
3. Polyphase Filters (course webpage)
4. Harmonic Balance ADS simulation tutorial
5. ADS Mixer Design Guide Tutorial

1. Circuit implementation:

The block diagram illustrates the main circuit elements in the design. The phase shift networks should be integrated on-chip. A one or two-stage polyphase differential phase shifter is recommended for the IF branch for better amplitude balance and tolerance to component variation. The LO filter can be a simple RC low-pass/high-pass when the mixer is driven as a switch because the amplitude balance is not important. However, if you decide to not use the switching LO mode of operation, then you should also implement an LO polyphase filter.



For upconversion, it is necessary to phase shift the baseband or IF input to the mixer as well as the LO, then sum the mixer outputs as shown. The equation representing this is:

$$\cos(2\pi f_{LO}t)\cos(2\pi f_{IF}t)+\sin(2\pi f_{LO}t)\sin(2\pi f_{IF}t)=\cos[2\pi(f_{IF}-f_{LO})t]$$

This produces a lower sideband output. (homework: show how you can modify this to make it upper sideband).

2. Circuit Design:

You will be using the TQHBT3 Design Kit for simulation of circuits. (appendix 2)

- When creating a new project:
  File > New Design. Name your design schematic. Also, select the Design Technology File to be *Design Kit: TQHBT3* and check the "*Set as Project Default"* box.
- You will also need to place the *TQHBT3 Netlist Include* icon on the top level of your schematic to enable the device models.

To get started, design the Gilbert mixer. Assume differential input and output because the polyphase filter will give you a differential signal at its output[1] and differential signals are required at the mixer outputs. The Triquint HBT models are installed only in 5162D, not in ECI. Create a mixer subnetwork.

a. Biasing. Reduce the size of the HBT as described in Sect. 3. The biasing of the Gilbert cell inputs can be done with resistive dividers and DC blocking capacitors (do not oversize – these can take up a lot of area) or a fully DC coupled design can be produced through the use of emitter followers. The maximum emitter current for a one-finger device is about 8 mA. Use current mirror emitter pulldown biasing for all differential stages to minimize temperature variation of bias current. See appendix 4 below.

b. Stability. Analyze the mixer as a cascode amplifier by biasing one pair of LO transistors into cutoff (ground their bases). Make and rename a modified mixer

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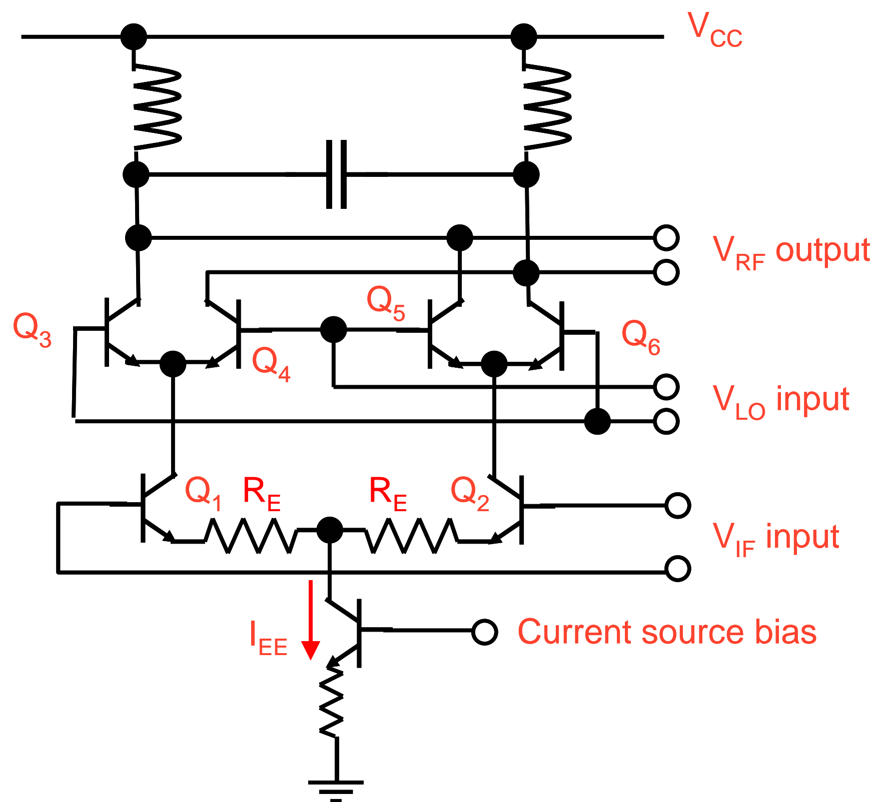
[1] F. Behbahani, et al., "CMOS Mixers and Polyphase Filters for Large Image Rejection," IEEE J. Solid State Cir., Vol.36, #6, pp. 873-887, June 2001.

subnetwork where two of the LO switch transistors are biased off all of the time. AC Ground the LO input and now you have a cascode amplifier. Use the same small signal S parameter stability analysis that you used in last quarter's amplifier designs to plot the k factor, mag(delta) and stability circles. You may find that it is necessary to add stabilizing resistors to avoid possible oscillation problems.

c. Gain. Use the differential Mixer Design Guide templates to evaluate conversion gain and gain compression. Use emitter degeneration to trade off gain for V_{1dB}. More on this in Sect. e. Be careful selecting load impedances that are realistic for an on-chip application in your simulations. If possible, use your output amplifier as the load. The off chip interfaces are 50 ohm, but on-chip should use higher impedances to conserve power. You may want to consider tuning the output if the conversion gain is rolling off at 1 GHz. The mixer output can be tuned by putting spiral inductors between the supply and the collectors of the upper tier in the Gilbert cell. Adjust the frequency by adjusting the inductance or adding extra capacitance between the collector nodes as shown below. The two mixer (I and Q) collector nodes can be joined together, sharing the same pullup inductors, to combine the I and Q at the output buffer.



d. Filters. The maximum reasonable capacitance for a MIM cap would be about 20pF. So, choose your R values in the polyphase filter (PPF) to be compatible. You will need to design an input driver for the filter to convert from single ended to differential and transform to low impedance levels. See [1] for more details. The source impedance must be much lower than R for the PPF to work correctly. The resistors must be scaled higher

as subsequent filter stages are added. Good results were obtained last year with a 2 stage PPF.

e. Input/Output: The input and output stages must be differential amplifiers. The input stage converts from single-ended IF and LO to differential signals needed for the polyphase filters and mixer inputs. Note the V_{1dB} of this stage. The total IIP3 of the chip depends on your gain distribution. You need to consider how much gain per stage and IIP3 per stage is required to get roughly even contributions from each stage to the total IIP3. This will guide your use of emitter degeneration for the I/O and mixer stages. The output stage must convert to a single-ended, 50 ohm output.

3. Triquint HBT:

We are using the Triquint TQHBT3 process. There is a standard size InGaP/GaAs HBT provided in this process (HBTS: 3 x 3 x 30 um). The layout is available as a standard cell in the ADS Layout library. This device area is intended as a unit cell for power amplifiers. I recommend that you reduce this to the minimum area making it a single emitter finger device (1 x 3 x 15 um^2) to reduce power dissipation and thermal effects. All HBTs must have the same emitter orientation.

You must read and observe the Electrical Design Rules, section 3 of the Triquint manual. Failure to follow these limits will lead to nonfunctional projects. Note that the simulator will not necessarily tell you if you are breaking these rules, so you must independently determine whether your design is correct.

1. Breakdown voltages: See section 1.1. (BVcbo = 24V; BVceo = 14V)
2. Maximum power dissipation per device (not likely to exceed this with small devices. It's limited by thermal resistance – Rth = 84240 $^oC/W/area(um^2)$ and junction temperature rise – 45°C above substrate; max T_J = 150C)
3. Maximum emitter current density: 1.5 x 10^4 Amps/cm^2

The InGaP/GaAs HBT has different behavior with temperature than a standard Si BJT. The beta drops with temperature [$\beta_F = 206 - 0.25\ T(K)$]. Vbe vs. T has a slope of – 1.3 mV/K and the typical Vbe is about 1.2V. The beta drop can lead to a phenomenon called "current collapse" in multifingered power devices[2]. Triquint shows that you can eliminate this condition if the device is operated at low Vce and/or by adding base series resistance. Refer to appendix 4.

Passive elements:

Since the chip dimensions are quite small, lumped elements should be employed rather than transmission lines. These will make use of the Nichrome (NiCr) resistors (tqhbt3_resw), MIM capacitors (tqhbt3_cap), and spiral inductors available in the Triquint process. Use the MRIND icon to simulate an inductor in your circuit. The dimensions can be determined by using the induct_fndy1.exe program. See appendix 3.

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[2] W. Liu et al., IEEE Trans. On Elect. Dev., Vol. 43, #2, pp. 245-251, Feb. 1996.

See Sect. 5 of the Triquint manual for data on these elements. Sample layouts are available in the ADS cell library. These can be modified or stretched as needed for your design.

The substrate thickness is 100 um. Substrate vias are allowed for our projects.

Diodes

There are 3 types of diodes available in this process. The Schottky diode is mainly used for level shifting. The DBC is a base-collector diode used for ESD protection. It could probably also be used as a varactor diode, but data on this application is not available. The base-emitter diode should not be used. They now recommend DBC for ESD protection. ESD protection should not be too important for our project since the chip will be probed, not packaged.

Pad layout

The chip will be tested using high frequency wafer probes; the parts will not be packaged. The probes are configured in a ground-signal-ground (GSG) pattern[3]. The probepads are 100 um square with a 150 um center-to-center pitch. Probe pad standard cells are available in ADS. Include the PAD menu item in your schematic to account for its capacitance in your circuit simulation.

You have a maximum of 4 GSG probe pads, one on each side of the chip. You can supply DC offset through the input and output pads if needed. This will require an external bias-T to separate the DC and AC paths. This eliminates the need for extra pads for DC biasing.

Observe on the pad frame drawing that the 4 GSG pad grounds should be connected in a ring or they can be locally grounded through substrate vias if you require more space.

Die size

The die size is a maximum of 2.25 mm x 2.25 mm. Keep in mind that the total area given to us on the fab run is 7mm x 7mm and we have at least 5 or 6 projects to include in this space.

Lab report and layout of the chip

You must complete the simulation of the circuit and a layout and submit a comprehensive report on your work. You will also be asked to present your circuit at a design review meeting on Friday, May 16. The report is also due at that time. The layout must pass the design rule check before it will be accepted.

The report must describe the design and chip layout, show simulation results, and address the following:

1. Stability of Gilbert mixer
2. Optimum LO voltage
3. Stability of bias conditions with temperature from 20 to 80 C.

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[3] http://www.ggb.com/40a.html

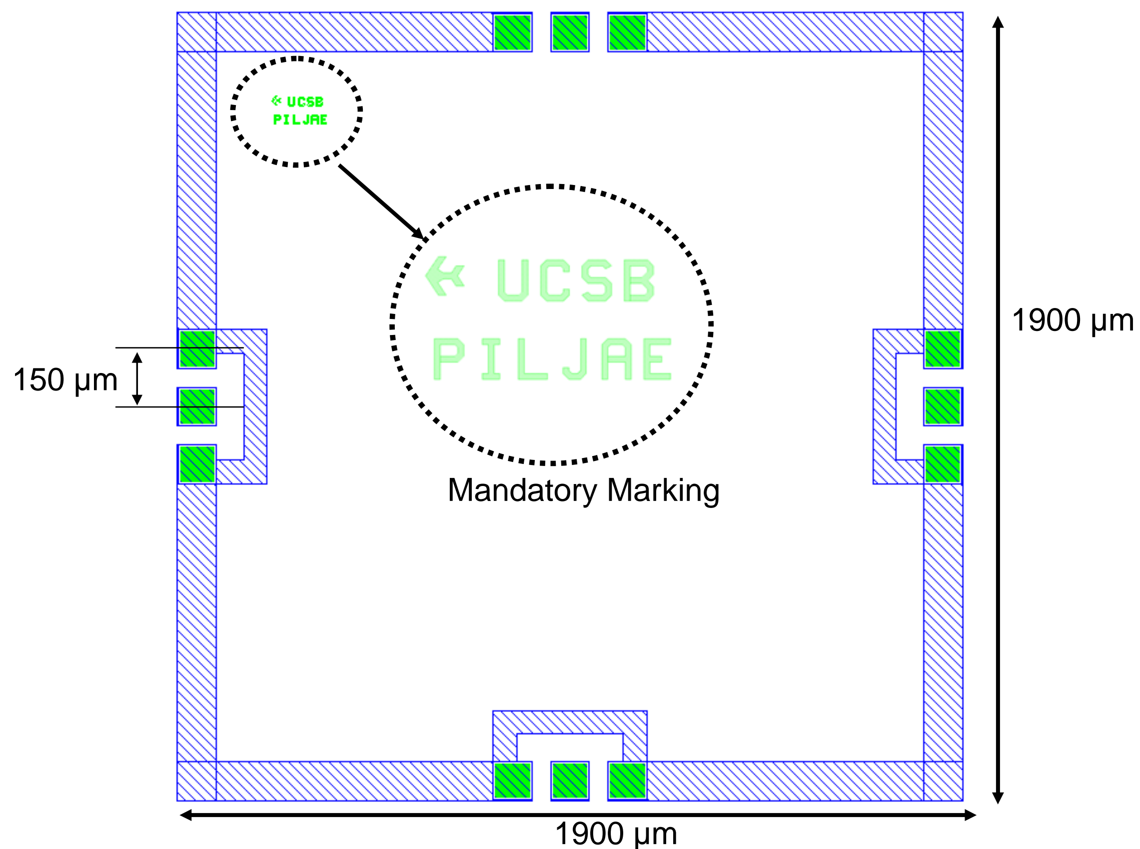
4. Image rejection ratio and its sensitivity to resistor and capacitor process variation and temperature.
5. Gain distribution and simulated value of P_{1dB} and IIP3.

Appendices

1. Chip layout and pads

Outline Layout:

Allowed die size for each group is 1.9mm x 1.9mm.
→ Your final submission should be enclosed with 2mm x 2mm tqhbt_CBDY layer.
4 input ports–IF, LO, RF and DC input – are needed.
For each port 150 µm pitch probe (GSG) pads are need for measurement.
Mandatory die sorting marking is required; simple and unique will be good.
→ Arrow-like die sorting mark will be distributed.

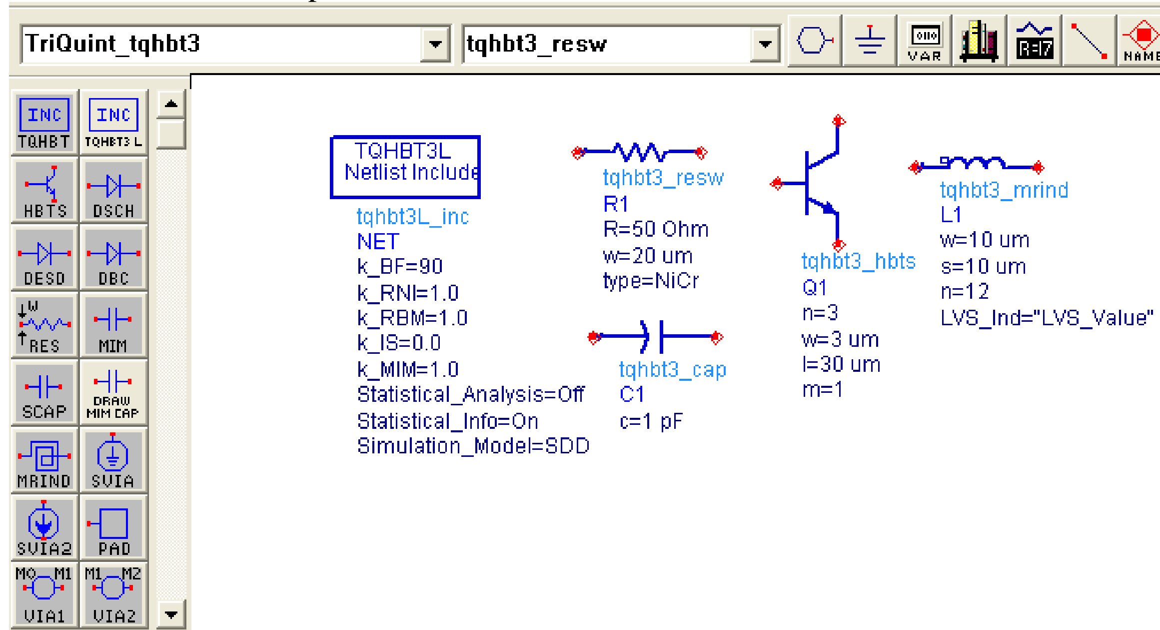


2. Using ADS to simulate the Triquint HBT in design files

1. First create a new project in the ADS main menu: File > New Project. Name the project, then you must select the Project Technology File: DesignKit TQHBT3.

2. You will find a TriQuint_tqhbt3 set of components in the pulldown component menu. You must place the TQHBT3 Netlist Include icon on your schematic in order for the simulation to run.

3. The HBT and some passive elements from the menu are shown below.



3. Inductors in the Triquint TQHBT3 Process

1. Use the mrind inductor model element in the Triquint_tqhbt3 menu for your initial simulations. You can use their inductor simulation tool to relate physical dimensions with an inductance.

2. Inductor simulation tool: (Download from web: Induct_fndy1.exe) This is a dos program that generates an equivalent circuit network for a given inductor physical dimensions. They claim that it works ok below half of the self-resonant frequency. Read the pdf file describing how it is used. The inductor would normally be implemented with M2. M2 is 4 um in thickness. The substrate thickness will be 100 um. Use the other default values shown in the application note.

3. The ADS layout tool will generate a spiral inductor for you if you provide the dimensions. Or, the MRIND inductor from the schematic can generate a layout.

4. Design of bias networks for HBT circuits

Temperature compensation is important for any HBT circuit because the higher power density associated with thesedevices leads to increasing device temperatures. The device junction temperature (Temp_J) is directly proportional to the power dissipation (PD) and is related by the thermal resistance Rth.

$$Temp_J = T_{substrate} + R_{th}P_D$$

The Triquint HBT model includes a thermal model. The substrate temperature, Tsub, of each device must be specified explicitly. Then, the model calculates the dissipated power and adjusts the DC currents and voltages according to the junction temperature under operating conditions.

The InGaP/GaAs HBT temperature dependence is different from Si bipolar transistors. Both have a Vbe that drops with increasing temperature, but they are opposites with regard to the current gain (beta). The HBT's current gain drops with temperature whereas the Si BJT increases with temperature. Thus the failure mechanisms and biasing requirements are different. Si BJTs will experience thermal runaway – a positive feedback condition where rising temperature increases the collector current. The HBT experiences a current collapse or reduction of current with temperature depending on the mode of biasing. The IV plot below shows how I_C drops with increasing V_{CE} as the junction heats up.

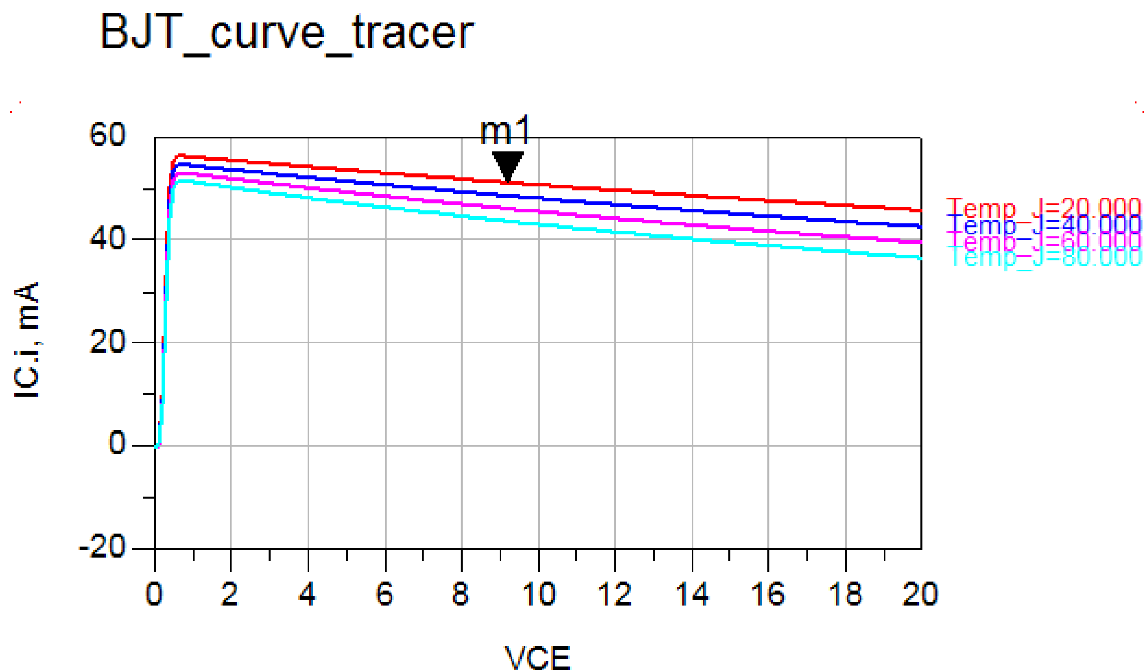


Figure 1. Collector current decreases with increasing temperature.

The reduction in current comes from the decreasing beta (current gain). This must be compensated if the PA is to have an operating point that doesn't drift with temperature.

If the device is biased with a pure current source, it can experience a catastrophic failure. As the temperature increases, V_{BE} drops and the reverse leakage current (negative) from the base-collector junction increases rapidly. The current source tries to keep the current constant, so forces more current into the BE junction and the device dies. If biased with a voltage source, the V_{BE} drop increases base current exponentially and the device gets fried.

One way to avoid this in HBTs is to use a base ballast resistor: put a resistance in series with the base of each HBT cell so that increasing base current causes a drop in V_{BE}, thus compensating for these effects. A current mirror is also helpful because its bias transistor, which should be located near the transistors it feeds, sees the same substrate temperature, and its V_{BE} decreases along with that of the other HBTs. For circuits that use smaller transistors than power amplifiers, the problem is not as severe. Keeping V_{CE} small to minimize heating and biasing with a current mirror should be sufficient. Triquint recommends adding emitter resistors to current mirrors to further improve stability of current with temperature. This can be easily tested by using a temperature sweep of the current mirror with a resistor as a fake load. The result of a swept temperature and sweep of the base resistors RB in Fig. 2 is shown in Fig.3.

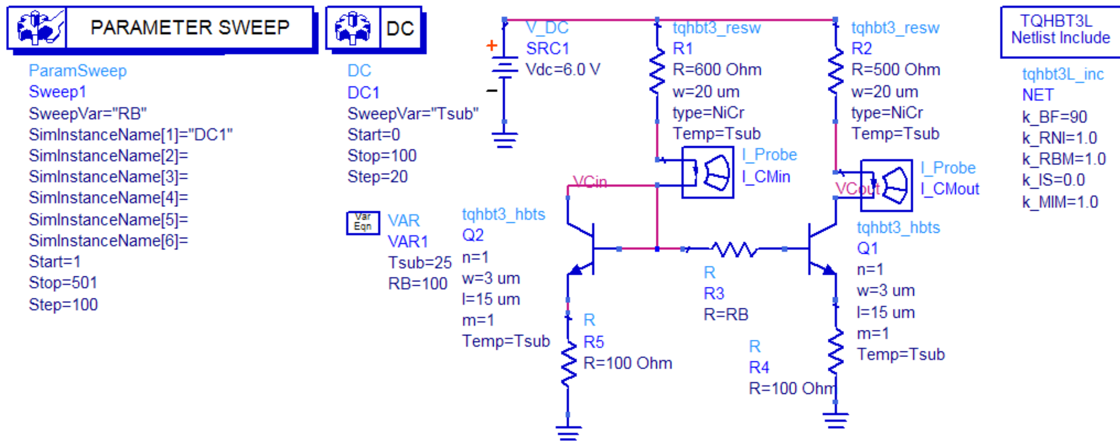


Figure 2. Dual sweep of substrate temperature and base ballast resistor RB.

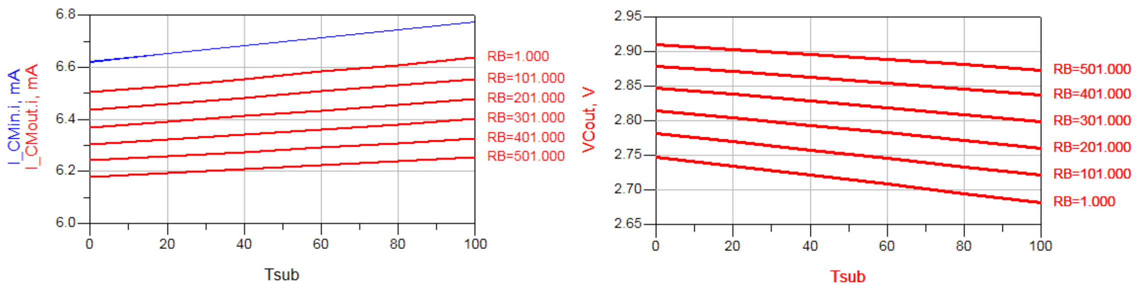


Figure 3. I_CMout is the output current of the current mirror. Note that the temperature variation is reduced with larger RB.

References:

1. W. Liu, “Failure Mechanisms in AlGaAs/GaAs Power Heterojunction Bipolar Transistors, IEEE Trans. On Elect. Dev, Vol. 43, #2, pp. 220 – 227, Feb. 1996.
2. W. Liu, et al., “The Use of Base Ballasting to Prevent the Collapse of Currrent Gain in AlGaAs/GaAs Heterojunction Bipolar Transistors,” IEEE Trans. On Elect. Dev, Vol. 43, #2, pp. 245 – 251, Feb. 1996.