Frequency Synthesizer Project

ECE218B Spring 2008

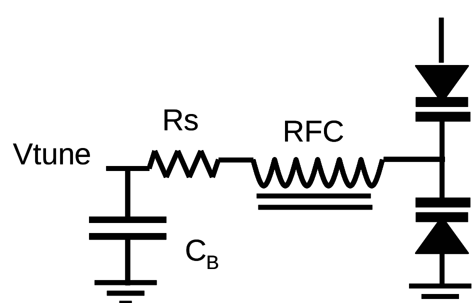
This project has two parts: VCO design and PLL design. The checkout and report for both parts is due 6/6/08.

1. VCO DESIGN. Design, build, and test a voltage-controlled oscillator (VCO). The intent is that the VCO can be used as part of a frequency synthesized local oscillator for an FM radio. You need to meet the following specs:

Output frequency tuning range	98 - 118 MHz (minimum)
Varactor tuning voltage range	2 to 12 volts
Supply voltage	+12 V
Output power	0 dBm in 50 ohm load
Second and third harmonic	-25 dBc minimum

1. The oscillator type that you will design is the common collector Colpitts using the 2N5179 BJT. Data sheet is on the course web page, and there is an ADS model in the Analog Transistor Library (pb_mot_2N5179_19921211).

2. Resonator Design. The electrical tuning of the oscillator will make use of the ZC839B hyperabrupt varactor diode. Connect two of these diodes back-to-back for improved harmonic distortion. Refer to the data sheet on the course web page**.** The varactor Q is typically 200 at 50 MHz and 3 volts reverse. You should avoid biasing the varactor under 2 volts reverse bias so that the Q remains high. Isolate the bias port with an RF choke, series resistor, and bypass capacitor (choose value for series resonance at 110 MHz).



You should implement the fixed capacitors in the resonator with zero TC (NP0) capacitors. There is a limited supply of NPO chip caps. Ask the TA for your required values. The inductor core material has a TC of +50 ppm/^{o}C.

Chip inductors are not recommended for the resonator because their unloaded Q is quite low, on the order of 20 to 30 at 100 MHz, therefore you will fabricate wirewound inductors on toroidal core material. The inductance of the toroidal inductor can be estimated by the equation below; use an A_L = 7.5 for the type 12 material with 0.125 OD.

Typical unloaded Q at 110 MHz is on the order of 100 and is better when turns are bunched together.

$$\#\, turns = 100\sqrt{\frac{L(\mu H)}{A_L\,(\mu H\ /\ 100\, turns)}}$$

Verify that your inductance is correct with the network analyzer to avoid needless frustration. The formula is only approximate.

A cylindrical wire coil can also be used, but will be sensitive to bending and position and will also have a temperature coefficient.

3. Do a detailed hand analysis of your oscillator, predicting startup conditions and the oscillation amplitude. Do not use high bias current for your oscillator – this is neither necessary nor desirable for good startup and stability and will increase power dissipation. Include the 5V voltage regulator to power your oscillator.

The hand analysis should be followed by ADS simulations before attempting to build the oscillator. Explore the bias current as a variable in the design. Make sure your design limits in cutoff (current limited) rather than saturation. Use the ADS diode model with the attached model parameters to represent the varactor. Do a small-signal open loop AC analysis to find the loop gain vs. bias current. A large-signal nonlinear analysis on the closed loop oscillator can be done by transient analysis or harmonic balance. Starting the oscillator in the transient simulator will require an impulse of current at the resonator since there is no naturally occurring noise to cause the oscillator to start. Compare analysis with the measured result.

4. The output from your oscillator must be buffered to avoid pulling the oscillator frequency with variations in the load impedance and to drive a low load impedance. Use a 2N5179 BJT as a buffer stage to provide this isolation and to drive the 50Ω output. Either a CE or CC stage can be made to work. The oscillator output amplitude will most likely be too high, so a series resistance between the oscillator output and the buffer amp input can be used to reduce the voltage swing. Make sure your bias conditions are within the acceptable peak current and voltage of the device according to the data sheet on the web site. The final application only requires 0 dBm (0.32V) into a 50 ohm load, so don't overdesign the buffer amplifier.
Design the buffer amplifier so that it will provide the required output drive power while using the least DC power.

You should perform a small signal stability analysis and modify the basic amplifier circuit to assure stable operation at the expected source and load impedances. Note that the amplifier need not be unconditionally stable, since you can control the Γ_S and Γ_L.

5. Implementation. You can use the generic VCO PCB to implement your oscillator. Solder down your components, keeping leads short, and build the oscillator. You will need to use both leaded and chip capacitors and resistors. Remember to use the NP0 caps for resonator components. Some layout examples can be found on the course website.

You will need some additional leaded components beyond what is in the parts kit for implementation of your design. Prepare a parts list of what you will need beyond your parts kit, and take this to the electronics shop.

Include the hand analysis, the ADS simulations, and well-documented final design in your report.

The following measurements should be made and documented in the report:
You can check out a wideband 10X probe from the TA for oscilloscope measurements.

1. Electrical tuning range Plot frequency vs. Vtune. Use a frequency counter for this measurement for more accuracy. Calculate the tuning rate at low, mid, and high ends of the frequency range.

2. Measure RF Output power and DC input power

3. Output spectrum:

A. Harmonics. Use the spectrum analyzer to determine the amplitude of each harmonic. Be careful to set the attenuation to avoid overloading the analyzer. If the 2nd and 3rd harmonics are strong (<20 dBc) your oscillator is probably voltage limiting instead of current limiting and the biasing should be changed to improve harmonic suppression. Use the oscilloscope to determine the limiting mode. Or, the buffer amplifier may be overdriven. Add more resistance in series between the oscillator and the base connection to the buffer amp.

B. Sidebands. These might be caused by parasitic oscillations or the "squegging" effect. They are usually caused by improper bias circuit design that allows a low frequency feedback path to cause a spurious oscillation. You need to get rid of them through proper bypassing and isolation methods. You will only be able to see them by using a narrow resolution bandwidth on the spectrum analyzer. You must show that you have checked your oscillator for sidebands at an appropriate setting.

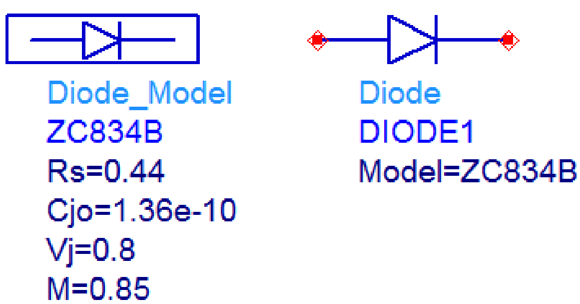
C. Spurious outputs (UHF oscillations). Measure the amplitude and frequency of any non-harmonically related output and try to identify its source and eliminate it.

4. Tuning voltage coefficient. Determine $K_v = \Delta f/\Delta V_{tune}$ by measurement of Δf for a small ΔV_{tune} at the low, middle, and high ends of the tuning range.

Parts Kit (To obtain additional leaded components, prepare a parts list for the shop.)

2	2N5179
2	ZC834B Varactor diode (SOT-23 package)
1	LM2931Z-5.0 voltage regulator
4	6.8 uH leaded inductor (RFC)
1	100 uF/25V radial electrolytic capacitor (for LOW freq. VDD Bypass)
1	0.1 uF ceramic leaded cap
1	T-12-12 (green/white) powdered iron core (for resonator) (For data on this core material see the web site for the class)
1	Generic VCO PC board
1	board mounted SMA female connector (for output)
2'	#30 enameled wire
2	2 ft. twisted pair of insulated wire (for tuning port input and for power supply connection)

Model parameters for the ZC834B Varactor Diode.



ADS uses the SPICE diode model. This model uses the equation below to describe the capacitance of a reverse-biased pn junction diode:

$$C(V) = CJO\left(1 - \frac{V}{VJ}\right)^{-M}$$

CJO = Diode capacitance at V = 0
VJ = built-in voltage of diode (default value 0.8V)
M = grading coefficient. (typically 0.5 for abrupt junction)

The diode equivalent circuit also includes a series resistance Rs due to the resistance of the semiconductor material and contacts. The varactor data sheet specifies this through the unloaded Q defined as

$$Q = \frac{reactance}{resistance} = \frac{1}{\omega C R_S}$$ at frequency ω and at a specific reverse bias voltage.

2. Frequency Synthesizer.

The goal of this section is to develop a frequency synthesized local oscillator for the FM broadcast band using your VCO. The LO will be locked to a stable crystal reference frequency (10.000 MHz) by a frequency synthesizer chip.

The frequency synthesizer board is provided. You will begin by interfacing your VCO with the synthesizer chip. Fully evaluate the synthesizer performance.

PART 1. Frequency Synthesizer

Implement the synthesizer shown in Fig. 1 and evaluate its tuning and noise characteristics. You will use the MC145170-D2 CMOS frequency synthesizer chip, a 10.00 MHz reference crystal, and an LMC6482 CMOS dual rail-to-rail op amp. A type 2 third-order loop should be used. (read the lecture notes and Vaucher[1] if more explanation is needed). Refer to data sheets for details on use of the chips. A PC board is provided for this exercise.

The VCO and synthesizer are on separate boards for convenience of testing, but be sure you use coax or twisted pair wiring to interconnect the VCO control voltage input to the loop filter output when interconnecting the boards to avoid noise pickup which would modulate the VCO. Also, note that your VCO tuning voltage input port RC time constant will add an extra pole to the PLL. <u>*You need to make sure it doesn't interfere with stability.*</u>

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***** Note that CMOS chips are easily destroyed by static charge. This has been a problem in the past. **Do NOT handle the CMOS chip unless you are wearing a grounded wrist strap.** Once the chip is installed, you should handle your board only while wearing this strap as well.

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[1] C. Vaucher, "An adaptive PLL tuning system architecture combining high spectral purity and fast settling time," IEEE J. Solid State Cir, Vol. 35, #4, pp. 490 – 502, April 2000. (on course web page)

Synthesizer specs:

Frequency step size	200 KHz
Frequency range	98 - 118 MHz or greater
Overshoot	< 30%
Reference Spurs	Better than 40 dBc
Settling time	1 ms to 1%
Output Power	0 dBm (50 ohms)
Crystal reference frequency	10.00 MHz

Signal levels:-

A	Pulses. 0 to 5 V. Max current sink/source = 0.36 mA
B	Control voltage. 2 to +12V (to VCO)
C	AC coupled. > 500 mV peak-peak into 50 ohms.

Power supply: +5V for MC145170-2. +12V for the opamp. As always, good bypassing at both low and high frequencies is essential for all components.

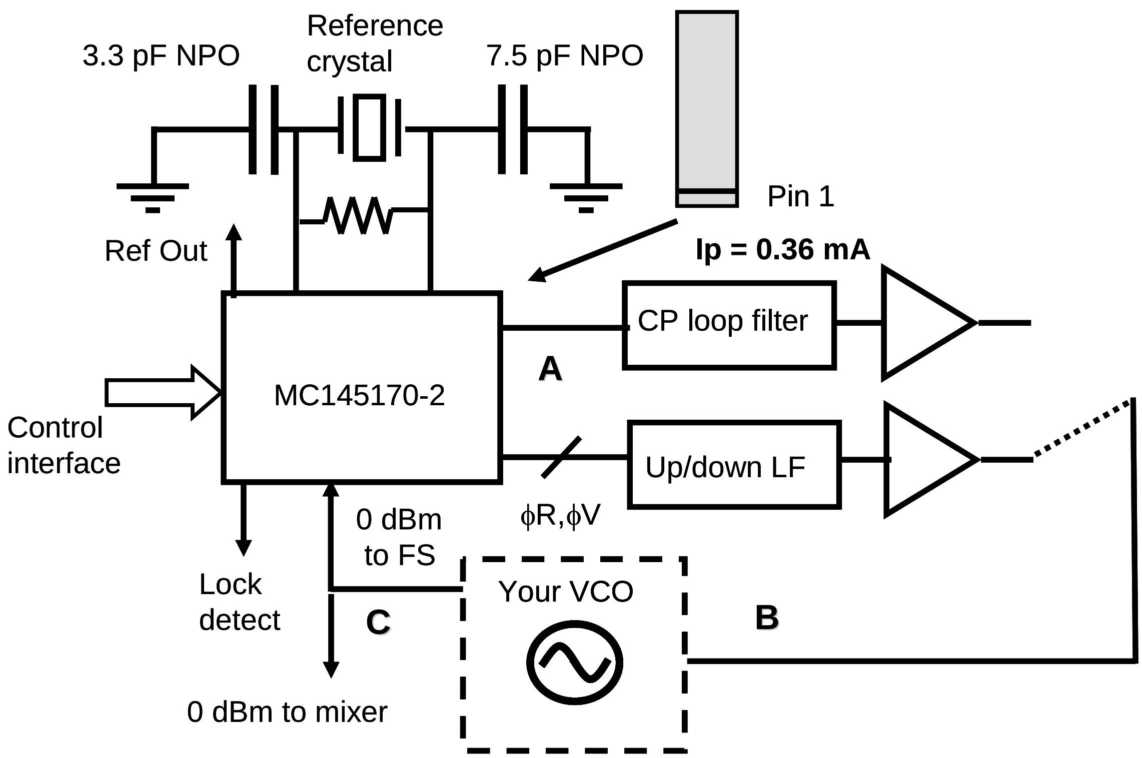

Figure 1. Block diagram of frequency synthesizer test board interfaced to VCO. Evaluate the synthesizer with either type of phase detector/loop filter.

Frequency control. There are 3 serially loaded registers on the FS chip that are set by the PIC controller card. This controller contains some firmware that can be addressed through the PC serial interface. A short description of how it works is at the end of this lab assignment.

The C register is a configuration register. See p. 15 of the data sheet. This allows selection of phase detector type and polarity, lock detector and Ref Out frequency. This must be set up first using a decimal number corresponding to the 8 bit C register word. The R register sets the divide ratio for the reference frequency. The N register sets the divide ratio for the feedback path divider.

Phase Detector and Loop Filter: The PLL includes two optional phase detectors: charge pump and phase/frequency (up/down). These require two different loop filter types as described in the lecture notes. In either case, design for worst case using the actual K_O measured at 98 and 118 MHz along with the corresponding N values.

The loop filter shown below in (a) can be used with the phase/frequency detector outputs. The input low pass filter network is required because the phase detector produces a strong 200 kHz rep rate pulse stream when the synthesizer is changing frequency. This filter will produce a third-order system.

- Use the design procedure described in the class notes and ref [1].
- Verify your design using ADS.

You may need to experiment with these to determine the best performance tradeoffs. *Watch out for any additional poles added due to low pass filtering networks at the input of your varactor tuning port on the VCO.* R1 should be no less than 15 kΩ in order to satisfy the maximum current output limit (0.36 mA) of the phase detector.

The charge pump filter (b) also includes a higher frequency pole created by C4. This makes the loop a third-order loop, so the pole frequency must be selected as described in class. Use ADS PLL Design Guide to verify your design. The current pulse amplitude coming from the phase detector is + or – 0.36 mA. The peak voltage of the pulse is 5V, so the opamp buffer should have enough gain to provide the 12V needed for your VCO. Include opamp gain as part of K_V in the ADS simulation. Again, beware of extra poles in your VCO tuning port.

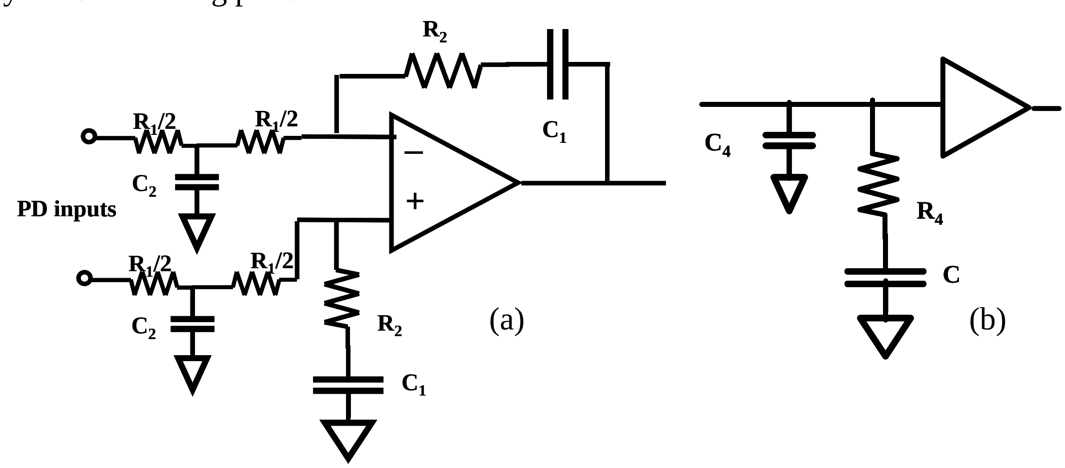

Figure 2. Loop filters for phase/frequency detector (a) and charge pump phase detector (b).

PART 2. Make the following measurements on your synthesizer:

1. Tuning range. Vary the N counter moduli to find the maximum tuning range of your synthesizer. You can use the tuning knob or the "radio mode" to set this frequency. What limits the tuning range?
2. Tuning rate. Use the toggle mode to jump between two frequencies. Test at 98, 108, and 118 MHz. Use $\Delta N = 10$ to avoid losing lock during the transition. Measure settling time and overshoot by observing the VCO tuning voltage on the oscilloscope and note the time constants. Modify your loop filter design if necessary to obtain a smoothly damped response. Report the shape and time constants observed. If time permits, try both types of loop filter/phase detector.
3. Noise spectrum. Observe the output on the spectrum analyzer. Zoom in on the fundamental signal and report and comment on the observed noise spectrum (evidence of phase noise? Reference sidebands?)
4. Compare measurements with simulations. Explain differences observed.

ECE218B Frequency Synthesizer lab parts list: Spring 2008

1	MC145170D2 CMOS Frequency Synthesizer chip
1	LMC6482AIN CMOS Opamp
1	10.000 MHz crystal (HC-49 package) Digikey X443-ND ECS-100-18-4
2	10 uF tantalum
1	0.1 uF leaded ceramic capacitor
1	1 Meg leaded resistor
1	board mounted SMA female connector
2	twisted pair of insulated wire (#24 or 26) 18 inches long
1	PC board (will be provided)
1	8 pin header
4	standoff posts + screws

5/12/08

Microchip PIC Based Microcontroller Board
Kyle Wilson, Computer Engineering, 2003

How it works.

The Microchip PIC18F252 is the heart of the board. Powered by a 10Mhz external crystal, it contains an internal PLL which multiplies the external clock by 4 to get an internal clock of 40Mhz. A digital encoder is used as an input to the system, while a 2 line, 8 character LCD display is used as an output along with an RS232 serial interface.

The digital encoder has two outputs which are pulled high by 10K resistors. These outputs are in quadrature format, which allows the system to determine which direction the encoder is being turned. If a pulse from one pin is high at any instance, and the other pin is low, the system can determine which direction the knob is being turned. By counting these pulses, the amount the knob is rotated can also be determined. In order to handle the input from this encoder in an efficient way, each encoder output is connected to an interrupt on change pin of the microcontroller. When an input signal changes state on this type of input pin on the microcontroller, an interrupt is generated. As a result, an interrupt is roughly generated each time the knob is turned slightly. In software, each time this event occurs, an internal counter is either increased or decreased, depending on which direction the knob was turned. With this counter value, the system can use it to determine how much the knob has been turned and add this offset to the N value it is controlling on the PLL circuit.

The LCD display is connected to the microcontroller over a parallel 4-bit bus with two control signals: E and RS. All data to be displayed and special LCD commands are sent over the 4-bit bus, while the E input signal determines if the LCD is enabled to accept data, and the RS signal determines whether the input data is data to be displayed or is a command word. Since everything is quantified in bytes, two transfers have to occur to transfer a full byte over the 4-bit bus. When the system is first turned on, the LCD must be initialized and setup using special commands to determine character size and enable/disable certain features. After this process has been completed, data can be displayed on the LCD. Certain timings must be met to ensure proper initialization and data transfer to the LCD.

The RS232 serial interface with the microcontroller is done through the USART. This module allows data to be sent and received at different baud rates. When this capability is combined with a level shifter, like the MAX232, the microcontroller can interface with the RS232 serial interface on a personal computer and data can be sent and received using any terminal program. For this project, a baud rate of 19.2kbps was used and is compatible with HyperTerminal, which is found on most Microsoft Windows installations.

Configuring HyperTerminal for Serial Communications.

Most user interaction with this project is done through the serial port. The HyperTerminal program that comes with Windows can be used to communicate with the board over a standard serial cable (NOT a NULL serial cable). When HyperTerminal is started, a new connection can be created in which you select which COM port the board is connected to and lastly the baud rate (Bits per second) at which to communicate with the board. The baud rate that should be used is **19200** and all other settings can be left at default. These settings can be saved in a preferences file so that a new connection does not have to be made each time. One is provided on the CD.

How to use the User Interface.

When the board is first powered on or reset, the menu is displayed. This menu describes all the appropriate actions you can take where each command consists of one letter. Commands can only be entered when a prompt '>' is displayed on the last line of the terminal. To view the menu at any time when a prompt is available, simply hit the 'm' key and the menu will be displayed.

1. Configuration Mode allows you to set the C, N, and R values on the PLL circuit. All values are decimal and the default values are shown in brackets [ ]. To simply keep a default value, do not enter anything in the terminal and just hit enter. These values are kept, except for the N value, until they are changed again in this mode. The N value can be modified by both the Toggle Mode and Radio Mode.

2. Toggle Mode allows you to toggle between two N values at a specified time interval. When you enter this mode, it will ask for a *Delta N* value. This value will be added onto the current N value and the board will cycle between the current N value and the current N value plus the delta N value. After the delta N value is configured, the *Interval* time must be specified in µs. This time is roughly the amount of time between each time the N value is toggled. Typically, values below 400µs will not be stable. After the interval time has been specified, the two values will be toggled with the specified interval until the 'q' key is hit to stop the toggle mode and return to the prompt.

3. Radio mode allows you to fine tune the N value at a specific interval as set by the R value. In this mode, the encoder knob is used to fine tune the output frequency and this frequency is displayed on both the LCD and the serial terminal. The C, N, and R values used in this mode are adopted from the values set in the Configuration Mode. The frequency interval at which the overall frequency changes is determined through dividing 10 Mhz by R. This mode can be exited at any time by pressing the 'q' key.

4. At the prompt '>', the current configuration can be viewed by pressing the 'd' key. This will display the current values for C, N, R, and Fif. To change these values, simply enter the Configuration Mode.