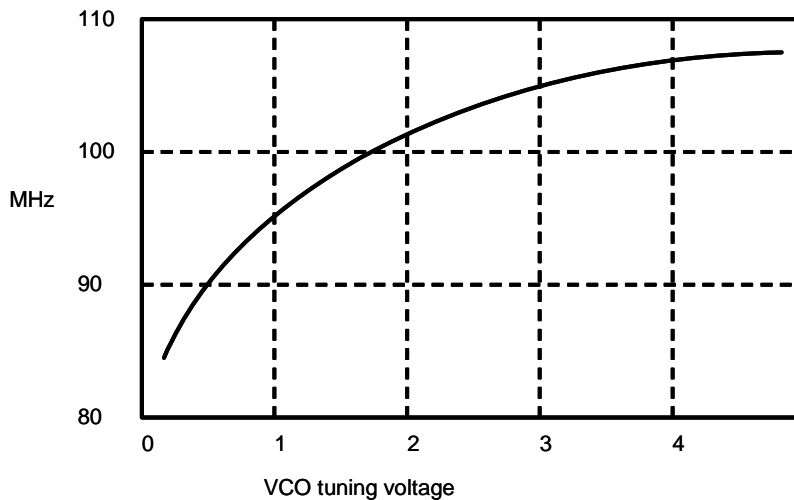
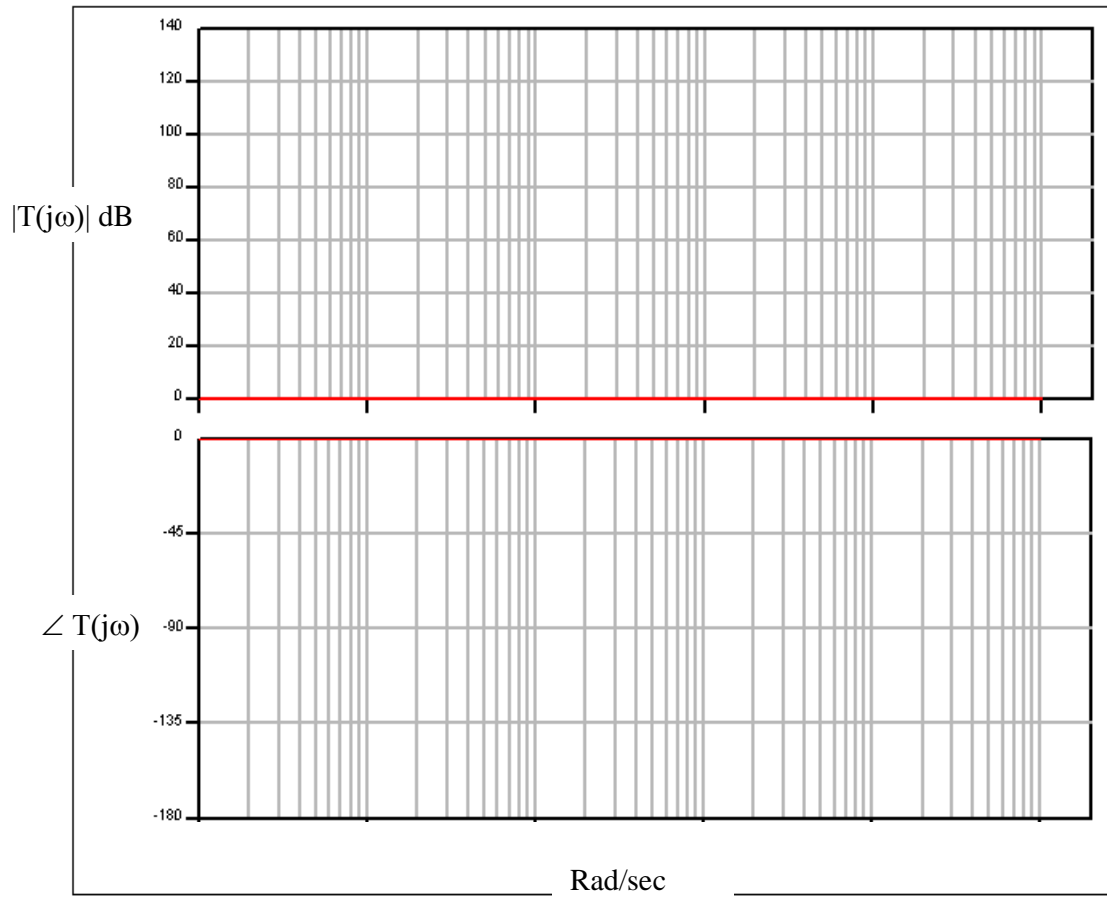


1. a. The phase detector produces pulses with 5 Volt amplitude whose width varies with phase difference over a range of $\pm \pi/2$ radians. Determine K_D .
- b. Determine K_O at 90 and 105 MHz.

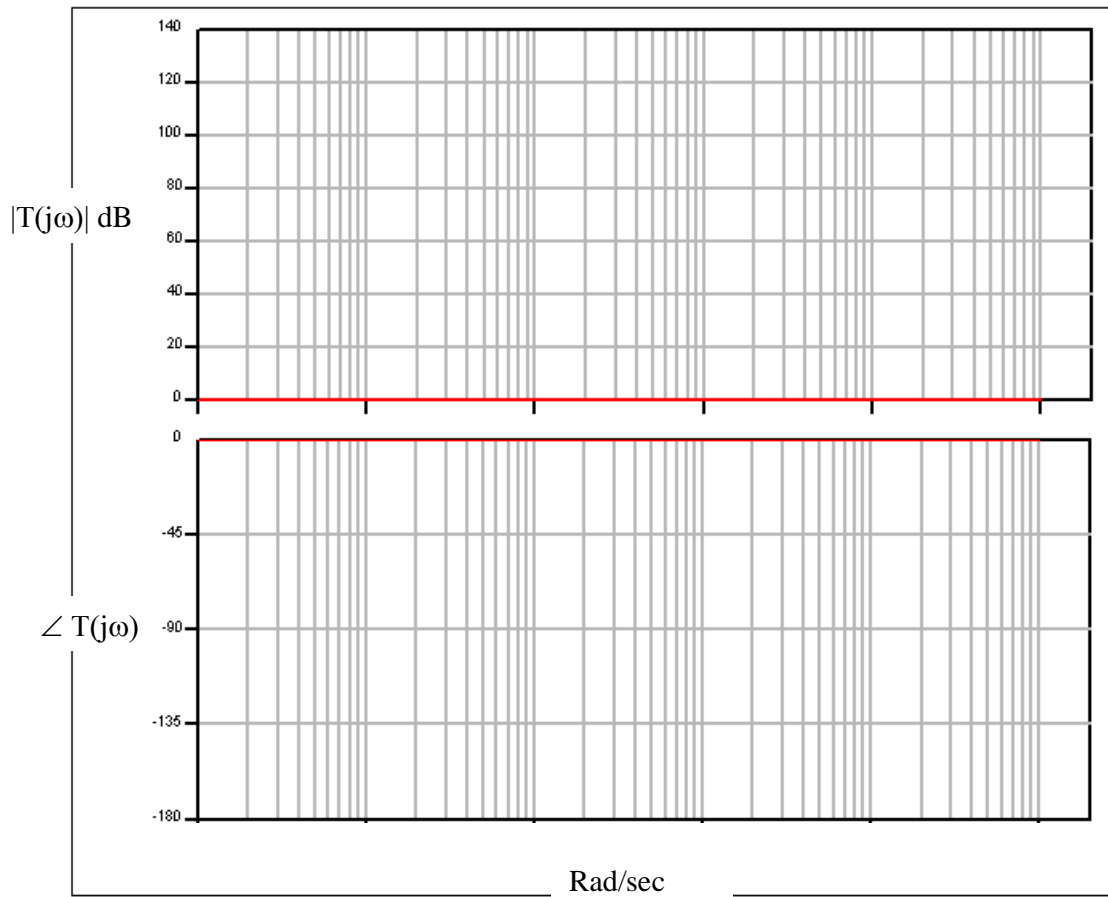
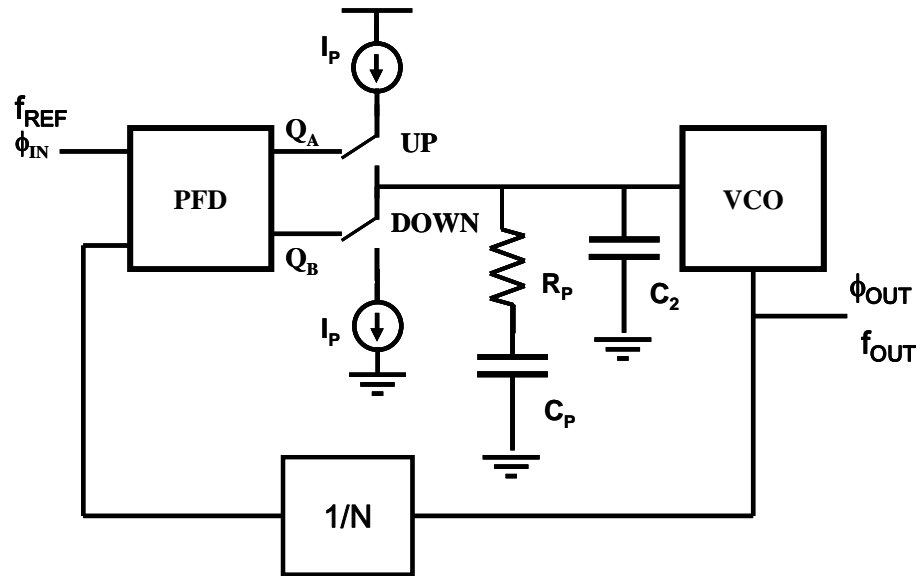


- c. If the reference frequency is 100 kHz, what value of N is required for output frequencies of 90 and 105 MHz?
- d. Design a type 2 second-order system with $\zeta = 1$ at the worst case frequency and a settling time of 100 μ s. Determine component values for the loop filter shown above. Find ω_n and ζ at the other frequency extreme. Assume a maximum output current from the phase detector of 0.1 mA.
- e. Use the Bode plot of the loop gain to estimate the crossover frequency and phase margin of this PLL at 105 MHz. Estimate the reference spur suppression.
- f. Sketch the root locus of the PLL phase transfer function. Show actual pole locations for the case above.

g. Now, split R1 in half and add an additional capacitor (C2) to ground at the center. Design for a third pole frequency of $10\omega_n$. Estimate the new phase margin and reference spur suppression. Simulate using the ADS PLL design guide to verify your phase margin and to find the transient response.



2. a. Now, using the same VCO, design a third-order PLL with the same frequency and settling time specifications using a charge pump. $I_p = 0.36 \text{ mA}$.



b. Verify with ADS.