8-bit Flash ADC

Pipeline detail

Fig. 2. Pipeline detail.

Reduced error rate due to cascaded latches

ENOB vs. input amplitude

Fig. 10. Effective number of bits versus full-scale range for 1-, 50-, and 100-MHz analog input frequencies, all at 200 Ms/s. Input amplitude was adjusted for each range.

2 stage 10 bit ADC

94 comparators instead of 1024

Figure 1: Block diagram of a 10-b, 1GS/s ADC.

2 stage ADC dynamic performance

Figure 5: Measured ADC performance at 500 MS/s with 49 MHz input.

Figure 6: Measured ADC performance at 500 MS/s with 200 MHz input.

Subranging ADCs

• Area and power efficient
• Reduced number of comparators
• Suitable for pipelining
  – Increased clock rate but higher latency
  – Interpolation, folding also can be used
• Uses simple CMOS diff amps
2 step 8-b subranging ADC

Output of 4-bit CADC
- selects between 15 reference subranges of 32 LSBs for FADC
- gives 4 MSBs
FADC has 5 bits to provide overrange – digitally correct for errors in CADC up to +/- 8 LSBs

Coarse ADC Operation: offset compensation
Φ1 reset for ½ clock cycle produces low Z at amplifier input.
Store Vref,j + Voffset on C
Φ2 then activates amplifier. The difference between VT/H and Vref then is sensed by the amplifier with the same offset.

Switch charge Injection compensation

- Charge injection on reset ($\phi_1$) is signal-independent
- $\phi_1$ opens slightly before $\phi_{1d}$ so that signal-dependent charge injection is minimized

CADC amplifier

- Full differential reduces substrate noise
- Cascode improves speed
- Current sources in parallel with $R_{load}$ increases $gm$

Fine ADC operation

Fig. 5. Operation principle of the FADC.

Fig. 7. Effect of finite on-resistance of the reset switches at high conversion rates.

Fig. 8. Implementation of the reset switches in array A and B of the FADC.

2X Interpolation of ref ladder

Reduces number of comparators, requires fewer ref voltages

Fewer subranging switches needed

Fig. 9. Implementation of 2× interpolation of the reference ladder voltages.

Another 2X interpolation

Charge redistribution is used to generate intermediate reference voltage

Fig. 10. Implementation of another 2X capacitive interpolation of the reference ladder voltages.

FADC pipeline

- Interpolation is introduced at A, B and C
- Only 17 ref voltage taps
- Capacitive loading of switches and amplifiers is reduced proportionally

Fig. 4. Block diagram of the FADC.
Active 2X interpolation

2X in row B
2X in comparator

Fig. 11. Simplified schematic of a differential-pair amplifier providing 2X interpolation.

Capacitive averaging

- **RESET:**
  - Each cap charged $V_{in,0}$ and $V_{in,1}$

- **AMPLIFY:**
  - Charge redistribute
  - Node voltage is the average of $V_{in,0}$ and $V_{in,1}$.

- Decreases influence of switching noise and random mismatch
  - which is uncorrelated
- Better SNR

![Capacitive Averaging Circuit Diagram](image)

*Fig. 12. Implementation of 2X capacitive averaging.*

4X averaging of A stage; 2X averaging of B

Fig. 13. Distributed averaging topology, providing 4X and 2X averaging of the amplifiers in array A and B, respectively.

CMOS MS Comparator

Fig. 10. Implementation of master-slave comparator, optimized for a low bit error rate.

BJT Comparator

Folding ADC

Fig. 4. Block diagram of a single folding system.

Fig. 8. Triangular waveform with rounding-off effect.
Double Folding ADC

90 degrees out of phase

Rounding error is corrected in fine ADCs by nonlinear R ladder taps.

Range overlap reduces nonlinearity due to rounding error

Fig. 6. Signal waveforms of the double folding system.

Double folding circuit

Fig. 7. Simplified circuit diagram of the double folding system.

References


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