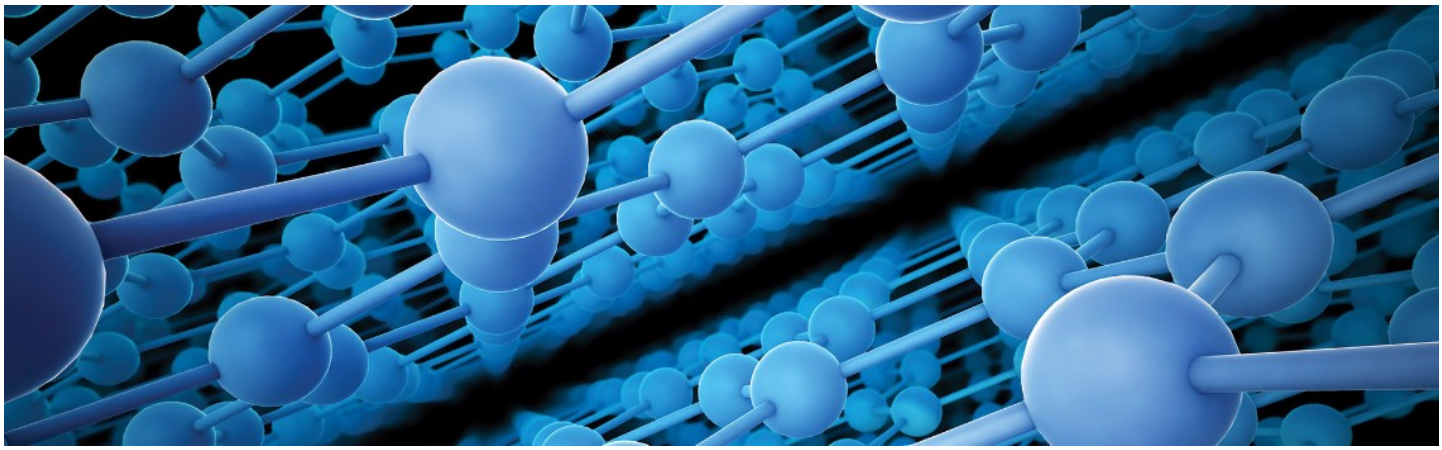
Graphene Gets GaAs Onto Silicon



What's the trick to growing high-quality GaAs on silicon? It's inserting a layer of graphene between them.

BY SHAMSUL ARAFIN FROM UCLA

Our computers don't operate anywhere near their potential. Instead, their microprocessors spend a lot of time waiting for data. Even if we invest in the state-of-the-art – an Intel Core i7 processor with high-speed RAM or liquid cooling – the problem persists, because the speed of the computer is not governed by the processing power, but by the physical connections between the processor and the incoming data.

The solution, which is well known but challenging to implement, is to turn to photonic integration. By taking this path, trimming the power consumption can go hand-in-hand with a hike in system performance: Greater speed, wider bandwidth and superior reliability. What's more, by using photons rather than electrons, more efficient data transfer is possible from module-to-module or chip-to-chip.

Given these advantages, it is easy to understand why there is a worldwide research effort underway to replace the existing, old-fashioned, electron-carrying copper with a technology that routes photons around chips. Super-fast computers could follow, but this requires the pairing of silicon substrates containing matured CMOS electronic circuits with a material that can emit light.

Light-emitting GaAs is the leading candidate for monolithic integration with silicon, and since the 1980s efforts have been underway to bring these two materials together. Accomplishing this is no mean feat, however: Anti-phase domain boundaries can formation during growth of polar GaAs on nonpolar silicon; and a high density of threading dislocations can result from a combination of a 4.1 percent lattice mismatch and a 62 percent thermal expansion coefficient mismatch between these two materials.

At the University of California, Los Angeles (UCLA), our team led by Kang L. Wang, the Raytheon Professor of Electrical Engineering, is working in collaboration with colleagues at UC Irvine and UC Riverside to develop a growth technique that can deposit GaAs on silicon using an intermediary material – graphene. With this bridging material, MBE can form ultra-smooth, almost-epitaxial films of GaAs on top of a single-layer sheet of carbon atoms that sports many attributes, including breath-taking electron mobility, high conductivity, and great flexibility and strength.

The approach that we have taken is often referred to as van der Waals epitaxy, and thanks to the one-atom thick pure-carbon buffer layer, we are relieved of material-related intrinsic challenges, such as lattice mismatch and thermal expansion coefficient mismatch. The very weak physical bond between the MBE-grown GaAs and the graphene buffer layer is the key to this success, because it can accommodate thermal mismatch and strain due to in-plane lattice mismatch (see Figure 1).

Our efforts follow in the footsteps of the pioneers of van der Waals epitaxy, Atsushi Koma's group from Akita Prefectural University, Japan. In the mid 1980s, that team constructed layered material systems, such as selenium/tellurium and $NbSe_2/MoS_2$, with this growth technology.

Since then, there has been a growing acceptance of van der Waals epitaxy as a useful route to heteroepitaxy. Recently, even heterostructures with a lattice mismatch as high as 40 percent have been grown with reasonably good crystal quality. The technique has also been extended to enable the growth of three-dimensional materials on top of layered materials by researchers at IBM T. J. Watson Research Center.

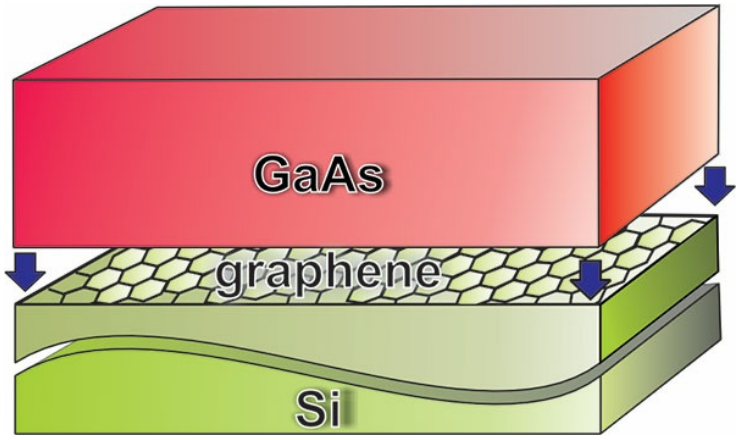


Figure 1: An intermediary single graphene layer allows the growth of GaAs on silicon.

Although production of inexpensive, large-scale graphene is now possible, we have used a mechanical exfoliation technique to deposit graphene onto silicon substrates. This approach begins with a 5 minute rinse of a 1 cm by 1 cm piece of silicon in acetone and isopropanol, before graphene flakes are mechanically exfoliated onto non-HF-treated silicon by the well-known scotch-tape technique. The silicon substrate with the monolayer of graphene is then cleaned in acetone and isopropanol to remove any residual organics from the exfoliation process (see Figure 2 for images of the mechanically exfoliated graphene).

The quality of the epitaxial growth hinges on the nucleation step, which influences film properties, morphology, homogeneity, defect densities, and adhesion. Growth of our nucleation layer was performed using a room-temperature-deposited gallium-prelayer and a very low growth rate. We set the GaAs growth temperature to just 350 °C to avoid islanding and to enhance the nucleation process. This yielded ultra-smooth GaAs thin films on graphene-on-silicon that can serve as a nucleation (seed) layer for subsequent growth.

Quality of our as-grown films has been assessed by Raman spectroscopy, which exhibited two GaAs Raman signature peaks corresponding to the TO and LO vibrational bands at 268 cm^{-1} and 292 cm^{-1}, respectively (see Figure 3(a)). The forbidden, but intense TO- mode results from defects in the nucleation layer, indicating the need for further improvement in material quality.

A comparison of the quality of our films with those formed by conventional growth is possible by comparing full-width at half maximum (FWHM) values of X-ray diffraction rocking curves (see Figure 3 (b)). The results of this are very encouraging, with 25 nm-thick films made by us having a FWHM of 240 arcsec, which is the same value as micron-thick GaAs films deposited on silicon by conventional means. This two-orders-of-magnitude improvement is due to mitigation of the lattice and thermal mismatch between GaAs and silicon by the graphene buffer layer.

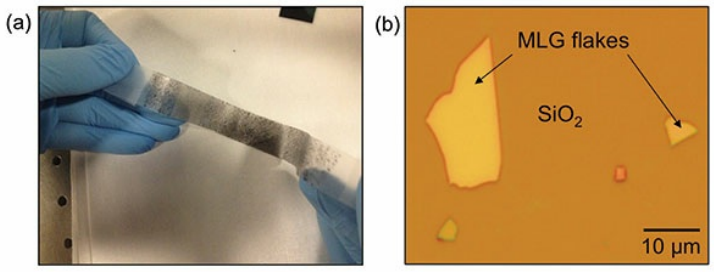


Figure 2: (a) Mechanical exfoliation of multi-layer graphene (MLG) flakes using scotch-tape, and (b) optical microscope image for the exfoliated MLG lying around a silicon substrate with a native oxide. Figure adapted from Alaskar et. al. (2014)

We have built on this success by creating a two-step nucleation process, followed by a raising of the temperature to 600 °C to grow a further 200 nm of GaAs. A polycrystalline film with a faceted surface results, due to thermal degradation of the nucleation layer (see Figure 4).

We have tried to prevent the island growth in the high-temperature epitaxy step by increasing the nucleation layer thickness to 100 nm.

However, this has not been successful, suggesting that the GaAs/graphene interface is not stable at high temperatures – and that's unfortunate, because high temperatures hold the key to crystalline GaAs, and to the suppression of defects and dislocations through migration.

It is our view that the root of the problem is the low adsorption and migration energies of gallium and arsenic on multi-layer graphene, which lead to cluster-growth at high temperature. However, it may be possible that by optimising the growth parameters, in terms of the pre-layer, or by turning to an alternative van der Waals material, it would be possible to produce a single-crystal GaAs thin film on silicon. We are looking into this, and also considering a low-temperature or modified deposition technique that would eliminate three-dimensional islands at high growth temperatures.

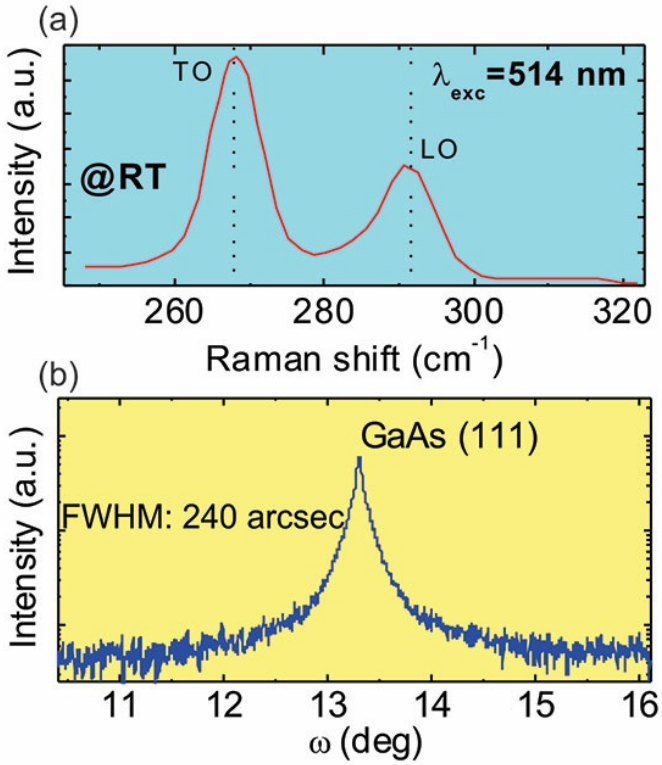


Figure 3: (a) The room-temperature micro-Raman spectrum for the low-temperature-grown GaAs nucleation layer, and (b) the X-ray diffraction rocking-curve scan of the GaAs (111) peak for such nucleation layer. Figure adapted from Alaskar et. al. (2014)

As our growth of graphene on GaAs improves, it could lead to cheaper, high-performance light sources. What's more, it might pave the way for the formation of other III-Vs on silicon, such as InP and GaSb, and ultimately spur a vast range of lower cost, high-performance semiconductor devices.

Before this might happen, we expect that thanks to its compatibility with current silicon planar CMOS technology, our novel growth technique will be used in the silicon photonic industry. Here it could be used for the realization of an electronics-photonics integrated circuit on a single chip, for applications ranging from on-chip photonics to optical transceivers, free-space laser communications and microwave photonics.

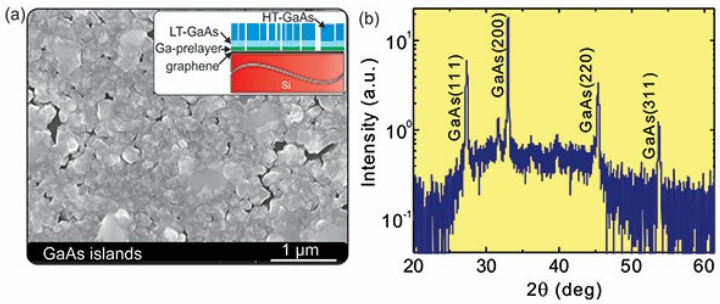


Figure 4: SEM image of (a) 200 nm high-temperature grown GaAs on top of a 25- nm--thick nucleation layer, with a gallium- prelayer showing cluster growth and (b) X-ray diffraction ω/2θ scan for GaAs grown by the two-step growth scheme, showing polycrystallinity with the presence of GaAs (111), (200), (220) and (311). Figure adapted from Alaskar et. al. (2014)

Such efforts form part of a global effort to develop electronic integrated circuits that incorporate optical emitters and detectors and will underpin the transition from CMOS to optics. The silicon industry is searching for ways to introduce optical capabilities onto the silicon IC, and our GaAs-on-silicon technology is one option for doing this in an economically viable manner.

Shamsul Arafin now works at UCSB

> ***Further reading***
> *Y. Alaskar et. al. Adv. Funct. Mater.* ***24*** *6629 (2014)*
> *J. Kim et. al.N at. Commun.* ***5 4836 (2014)***