A Chip-Scale Heterodyne Optical Phase-Locked Loop with Low-Power Consumption

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Abstract: A chip-scale heterodyne optical phase-locked loop, consuming only 1.3 W of electrical power, with a maximum offset locking frequency of 17.4 GHz is demonstrated. The InP-based photonic integrated receiver circuit consumes only 166 mW.

OCIS codes: (250.5300) Photonic integrated circuits; (060.2840) Heterodyne; Optical phase-locked loop; (060.5625) Radio Frequency Photonics

1. Introduction and Design of the Heterodyne OPLL

There has been significant effort for realizing highly-integrated chip-scale optical phase-locked loops (OPLLs) in the last decade along with the development in the photonic integration. Traditional free space optics creates loop delays in the order of tens of nanoseconds, which makes the loop bandwidth small. However, with the improvement in photonic integration, OPLLs can be realized with loop bandwidths in the order of hundreds of MHz [1] or even more than 1 GHz [2]. This makes OPLLs attractive and they can be used in a wide range of applications including coherent receivers, high sensitivity detection, laser linewidth narrowing, millimeter and THz wave generation and optical frequency synthesis [3-5]. In previous works, offset locking ranges up to 25 GHz [6], large loop bandwidth exceeding 1 GHz [2] and residual OPLL phase noise variance as low as 0.03 rad^2 [1] were demonstrated for the chip-scale OPLLs. However, these OPLLs consume almost 3 W of electrical power [2], being unsuitable for the real life applications. In this work, a chip-scale heterodyne OPLL with a total power consumption of 1.3 W is designed and demonstrated utilizing a novel indium phosphide (InP)-based photonic integrated circuit (PIC) and commercial-off-the-shelf (COTS) electronic ICs. The PIC receiver contains a widely-tunable (50 nm) compact Y-branch laser, a 180° hybrid (MMI) and two photodiodes. This is offset locked to narrow-linewidth (100 kHz) external-cavity laser (ECL) up to a range of 17.4 GHz with an RF synthesizer.

The low power consumption PIC is integrated with COTS electronic ICs in order to realize the highly-integrated OPLL. An optical microscope image and the schematic of the receiver PIC is shown in Fig. 1(a) and (b), respectively. The PIC incorporates a compact Y-branch laser formed between a high-reflectivity coated back mirror and a pair of Vernier tuned front mirrors. The output from one mirror leads to the coherent receiver used for offset locking, while the other output forms the optical output signal from the backend integrated system. The Y-branch laser has a compact cavity with short gain and mirror sections, requiring low current and therefore low drive power. It is tuned via Vernier effect and has been designed for high efficiency at 30º C ambient. The measured tuning range exceeds 50 nm with >50 dB side-mode suppression ratio.

The low power receiver PIC is connected with SiGe-based COTS ICs including a limiting amplifier and digital XOR as a mixer/phase detector. The limiting amplifier has a 3-dB bandwidth of 17 GHz with 30 dB of differential gain. The digital XOR operates up to at least 12.5 GHz input RF frequencies. The limiting amplifier limits the signal coming from photodiode pair to logic levels, which enables the system to be insensitive to any optical intensity fluctuations. A second order dual-path loop filter was used to get high loop bandwidth. This was achieved by employing a fast feedforward path which increases the system frequency acquisition range. Fig. 1(b) and (c) displays the architecture and a microscope image of the whole OPLL system, respectively. The PIC, electronic ICs and the loop filter are all integrated on an aluminum nitride (AlN) carrier, and wire-bonded. The system size is approximately 1.8 cm by 1.6 cm. Total delay is less than 300 ps, and the loop bandwidth is approximately 500 MHz.

2. Results and Discussion

Total power consumption of the OPLL system excluding the thermoelectric controller power is measured to be 1.318 W, which is the lowest power consumption for an OPLL to the best of authors' knowledge. In this system, the PIC consumes only 166 mW, and the COTS control electronics consume 1.152 W. Table 1 demonstrates the power consumption of every component and the total power consumption. This result is considerably better than the previous result reported in [2].

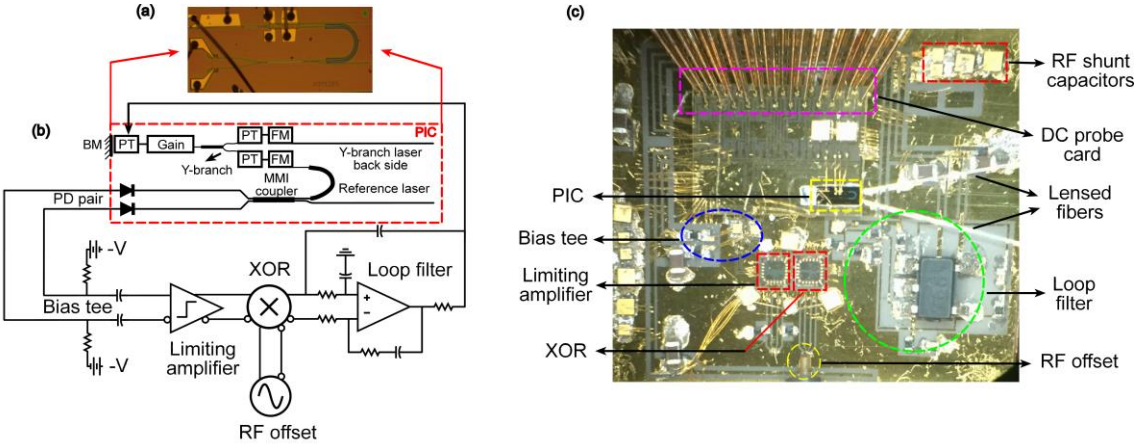

Figure 1. (a) An optical microscope picture of the PIC, (b) the schematic of the receiver PIC with the architecture of the OPLL system, and (c) a microscope picture of the OPLL system (PT: phase tuner, FM: Front mirror, BM: Back mirror, PIC: photonic integrated circuit, PD: photodiode)

Table 1. Power consumption of individual components and the total OPLL system

Photonic Integrated Circuit (Component / Power (W))	**Gain**	**Phase tuner**	**Photodiodes**	**Total**
	0.154 W	0.008 W	0.004 W	0.166 W
Electronic Integrated Circuits (Component / Power (W))	**Limiting Amplifier**	**XOR**	**Op-amp**	**Total**
	0.594 W	0.462 W	0.096 W	1.152 W
Total Power Consumption				**1.318 W**

Experimental setup shown in Fig. 2 was prepared in order to demonstrate the offset locking. The reference ECL was coupled into the PIC using lensed fiber and added to the tunable laser output from the lower Y-branch arm in the MMI coupler. Light from the top arm of the Y-branch laser was coupled out of the PIC for monitoring purposes. The optical spectrum of the reference laser together with that from the Y-branch laser were measured by an optical spectrum analyzer (OSA). At the same time their beat-note was measured by an electrical spectrum analyzer (ESA) through a high speed photodiode.

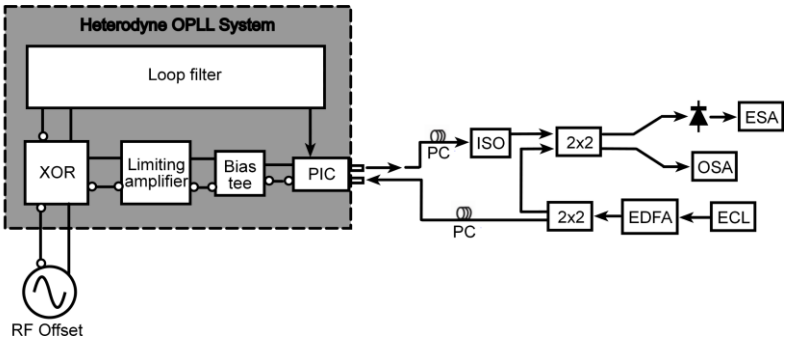

Figure 2. The test setup of the OPLL system. (ECL: external cavity laser, ESA: electrical spectrum analyzer, OSA: optical spectrum analyzer, PC: polarization controller, ISO: isolator)

The experiment demonstrates phase locking between the Y-branch laser and the reference laser. Fig. 3(a) shows the optical spectrum when the Y-branch laser and the reference laser are offset locked at 11 GHz, as determined by the RF frequency synthesizer. The OSA spectral separation between the lasers is ~ 0.09 nm which corresponds to 11 GHz. The beating tone of the locked lasers is shown in Fig. 3(b) both before and after the locking circuit is activated. The relative linewidth of the locked beat note at 11 GHz is in the order of sub-Hz, which is limited by the resolution bandwidth of the ESA. The beat note has a linewidth in the order of a MHz before the locking—that of the unlocked Y-branch laser. (With 20 km of fiber between the upper and lower external 2x2 couplers to de-correlate the ECL from the PIC output in time, the locked PIC linewidth becomes ~ 100 kHz—that of the ECL.) Fig. 3(c) shows a series of electrical spectra for the different offset locking conditions up to 17.4 GHz. Observed noise peaks are 400-500 MHz away from the main peak, and this suggests that the loop bandwidth of the system is approximately 400-500 MHz.

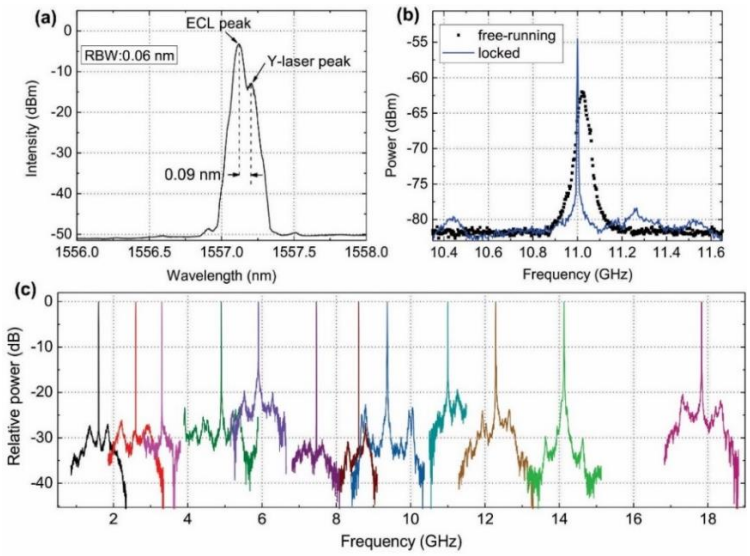

Figure 3. (a) The optical spectrum when the Y-branch laser and the ECL are offset locked at 11 GHz with a wavelength separation of 0.09 nm; (b) corresponding RF spectra measured at a 100 kHz resolution bandwidth (RBW), showing the locked beat note together with the unlocked case at 11 GHz, and (c) offset locking at multiple frequencies at a RBW of 3 MHz

3. Conclusion and Future Work

In this paper, a highly integrated heterodyne OPLL with a record power consumption of 1.3 W is demonstrated and on-chip widely-tunable Y-branch laser is offset locked to ECL up to a range of 17.4 GHz. This OPLL can be used in coherent receivers and optical frequency synthesizers. Without using any complicated digital signal processors (DSP) and high-speed analog-to-digital converters (ADC); low cost, low power short to modest distance communication systems can be realized using this kind of OPLL. In addition, this OPLL can create an opportunity to create chip level optical frequency synthesis with low power consumption.

With some straight-forward improvements in the COTS electronics, we expect to reduce the power consumption to below a Watt. Furthermore, application specific ICs consuming a few hundreds of mW power levels can be designed by using lower node CMOS processes, and this should enable such an OPLL with less than half a Watt of power consumption. If this system were to be interfaced with a self-referenced micro-resonator based optical frequency comb generator, a wide-band optical frequency synthesizer with a total volume of less than a cubic centimeter and a total power consumption of less than a Watt should be possible. This will create a new era in optical communication, sensing and imaging.

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4. References

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