University of Ulm

INVESTIGATIONS INTO MATRIX-ADDRESSABLE VCSEL ARRAYS

Master Thesis

by

Shamsul Arafin

Faculty of Engineering Science
Institute of Optoelectronics

ulm university universität
uulm

INVESTIGATIONS INTO MATRIX-ADDRESSABLE VCSEL ARRAYS

Master Thesis

Submitted by

Shamsul Arafin
Matriculation No. 611852
Communication Technology
March, 2008

Presented to

Institute of Optoelectronics

Examiner: Prof. Dr. -Ing. K.J. Ebeling
Supervisor: M.Sc. Abdel-Satter Gadallah

I hereby declare that I have completed this work independently and using only the aids included. Any passages that have been extracted or cited from other sources have been referenced appropriately.

Ulm, March 31, 2008.

.....
(Shamsul Arafin)

This work is dedicated to-
my loving parents and my youngest sister.
Their love and selfless support made this work possible.

Acknowledgements

First, all praise to God, the most Gracious and most Merciful, whose help and guidance is ever dominating throughout my life.

I would like to express my sincere gratitude to Abdel Satter Gadallah, M.Sc., for being my advisor. Throughout this work I got the invaluable support, perfect guidance, useful suggestions, magnificent cooperation, continuous support, effective advice, proper supervision and consistent encouragement from him. I am really grateful to him for his great assistance during the thesis period.

I was fortunate to be supervised by Dr. -Ing Rainer Michalzik with his gentle guidance, strong encouragement and great motivation.

I am deeply indebted to Prof. Dr. -Ing. K.J. Ebeling granting me the opportunity to do my M.Sc. thesis in his department.

I specially thank her whose contribution in this work was unforgettable and whose helping attitude was admirable, whose guidance was very spontaneous. She is none but Dipl. -Ing. Andrea Kroner.

I would like to convey my heartfelt thanks to Dipl. -Ing. Hendrik Roscher, Dipl.-Ing. Ihab Kardosh, Dipl.-Ing. Wolfgang Schwarz, Sussane Menzel and all other members of the Optoelectronics Department for their continuous support during the thesis period.

I am also grateful to Dr. Katrin Reimer and Prof.Dr.-Ing.Hermann Schumacher for organizing the necessary financial support during these six months.

I would also like to remember his name whose presence made me active and jubilant during the thesis period. He is my colleague and friend, Ahmed-Al Samaneh.

Finally, I appreciate my family's support and love in the two years' M.Sc. program.

Contents

1 Introduction **1**

1.1 Motivation 1

1.2 Thesis Outline 2

2 VCSEL Modeling **3**

2.1 Introduction 3

2.2 Device Structure 3

2.3 Band Diagram 4

2.4 Refractive Index 5

2.5 Standing-Wave Pattern 6

2.6 Reflectivity Spectrum 6

2.7 Summary 8

3 2-D VCSEL Arrays **9**

3.1 Introduction 9

3.2 Independent Addressing 10

3.2.1 Advantages 10

3.2.2 Disadvantages 10

3.3 Matrix Addressing 11

3.3.1 Advantages 11

3.3.2 Disadvantages 12

3.4 Strategy of MA Array Fabrication 14

3.5 Summary 17

4 Mask Design for Matrix Addressable Array **18**

4.1 Introduction 18

4.2 Mask for Mesa Etching 19

4.3 Mask for N-Contact Bondpad 21

4.4 Mask for Column Isolation 23

4.5 Mask for P-Contact Ring 24

4.6 Mask for Polyimide-1 25

4.7 Mask for Polyimide-2 . . . 26
4.8 Mask for Polyimide-Safety . . . 27
4.9 Mask for P-Contact Bondpad . . . 28
4.10 Summary . . . 30

5 Matrix Addressable Array Fabrication 31
5.1 Introduction . . . 31
5.2 Mesa Formation . . . 31
5.3 Selective Lateral Oxidation . . . 34
5.3.1 Oxidation Rate Dependencies . . . 35
5.3.2 Electrical and Optical Confinement . . . 35
5.4 Column Isolation . . . 36
5.4.1 Electrochemical Reaction . . . 38
5.5 N-Contact . . . 39
5.6 P-Contact Ring . . . 41
5.7 Polyimide Step . . . 42
5.8 P-Row Contact . . . 48
5.9 Summary . . . 49

6 Matrix Addressable Array Characterization 50
6.1 Introduction . . . 50
6.2 Electro-optical Characterization . . . 50
6.2.1 Experimental Setup . . . 51
6.2.2 Classification of Unit Cell . . . 51
6.3 Important Results Depending on the LIV Characterization . . . 53
6.3.1 Oxide Aperture Shape . . . 60
6.3.2 Calculation of D_a . . . 60
6.4 Calculation of Sheet Resistance . . . 60
6.5 Processed Wafer Characterization . . . 61
6.6 Optical Spectra . . . 62
6.7 Summary . . . 64

A Simulation Script 65

B Standing Wave Pattern of E-Field Amplitude Calculation 68

C Reflectivity Spectrum Calculation 69

D Mask Layout Using AutoCAD 71

E Instructions for Cleanroom 75

F Process Overview 104

G Epitaxial Structures 109

Bibliography 111

Chapter 1

Introduction

1.1 Motivation

Vertical-cavity surface-emitting laser (VCSEL) is one type of special promising laser which can be superior by its excellent performance among all existing semiconductor lasers at the present time. For the last few years, this has become the most attractive device for the fabrication of large two-dimensional (2-D) arrays of compact coherent optical sources due to number of performance and manufacturing advantages, e.g. low threshold current of 8.7 μA [1], low threshold voltage of 1.33 V [2], high packing density [3], higher power conversion efficiency at 50% [4], on-wafer testing, single mode operation and so on. These 2-D arrays are of great potential importance for various optical interconnection schemes [5], 2-D optical scanners [6] and display technology. All applications mentioned here require convenient optical or electronic addressing technique to communicate each VCSEL on-chip.

There are different methods available for addressing the VCSELs in the 2-D array. Among them, matrix addressing is one method of interest by which each VCSEL in an array can be electronically addressed and at the same time much larger array can be fabricated without having any problem since it requires less number of metal connections at the edges of the chip, unlike its individual addressing counterpart which requires large number of metal connections. The main drawback of 2-D matrix addressable array is that the devices fabricated in the array share contact-lines for which some control is lost over which devices can be turned on at a given time but that can be overcome by well known multiplexing techniques.

Recently this matrix addressable array has got great importance due to plenty of attractive applications like confocal microscopy [7], non-mechanical particle movement by optical tweezers [8, 9], and video imaging where large number of parallel optical sources with desired beam profile are needed. Matrix addressable VCSEL array can be the strong candidate to be implemented in these demanding applications since matrix addressing technique is capable of producing larger and denser 2-D array easily than independent

addressing. Here comes the supremacy of matrix addressing over independent addressing technique. However, by this time there have been some works done on this matrix addressing by the research community. Von Lehman *et al.* [10] showed the way to fabricate matrix addressing 32 x 32 array for the first time in 1991 and then Morgan *et al.* [11] fabricated 10 x 10 array in 1994 and then finally Choquette *et al.* [12] in 2002 also successfully fabricated this matrix addressable 64 x 64 array where they monolithically integrated the photodetectors.

The present thesis is devoted to the investigation into matrix addressable VCSEL array fabrication and the characterization afterwards. The entire work is carried out on the sample designed for the standard wavelength regime around 850 nm, grown by solid source molecular beam epitaxy (MBE) on undoped GaAs substrate. In this thesis work, at first one prototype mask is designed for matrix addressable 4 x 4 arrays which is smaller but denser because the pitch size is 125 μm. Then using this mask, eight lithographic steps associated with other necessary works e.g. oxidation of AlAs layer, wet chemical etching, metallization, lift-off etc. are performed for fabricating the arrays, followed by the characterization of the devices which includes measurement of light-current-voltage curves, uniformity of the arrays and so on.

1.2 Thesis Outline

In chapter 2, one typical VCSEL fabricated in the matrix addressable 4 x 4 array is numerically modeled depending on the sample recipe file where the description of device epitaxial layers was written. In chapter 3, some fundamental principles of matrix addressable arrays making the comparison with other addressing techniques have been summarized. At the same time the design approach of this work has been depicted by some schematic diagrams along with useful explanations. In chapter 4, the full description of the mask layout has been provided from where the design approach in this work gets revealed. In chapter 5, the experimental results and important relevant comments based on the device fabrication procedures have been described. The characterization and the measurements of the devices fabricated in the array are illustrated then in chapter 6. The thesis is then concluded by chapter 7 where the summary of this work and recommendations for future work contain.
Appendix A includes the source code used in SimWindows-V.1.5.0 to obtain the band diagram of the unbiased and biased VCSEL structure and the refractive index profile as well. Appendix B and C provide the mathematical equations necessary for calculating the standing-wave pattern of the electric field and the reflectivity spectrum of the full VCSEL structure respectively. Appendix D contains some handy tips and rules-regulations for drawing the mask layout in AutoCAD. All the necessary instructions need to be known in advance for working with the sophisticated devices in the cleanroom is attached in Appendix E. Appendix F provides all the process sequences maintained while fabricating the arrays. Finally Appendix G summarizes the epitaxial layer structures of the sample.

Chapter 2

VCSEL Modeling

2.1 Introduction

VCSEL modeling refers to the numerical analysis of device structure. In other words, the analysis of important characteristics of VCSEL depending on the materials grown by MBE machine is termed as VCSEL modeling. In particular, this modeling includes the band diagram, band diagram with biasing, refractive index profile, standing-wave of electric field intensity pattern and reflectivity spectrum of the full VCSEL structure. Though these are not only the modeling parameters, but these parameters are enough to get a general idea of the internal structure of the device.

In this chapter, the characterization parameters extracted from the information of MBE-grown sample (so-called recipe file which contains the specifications of all epitaxial layers) will be reviewed which are simulated in different software (e.g. MATLAB, SimWindows, REFLEX) and the results are discussed here as well.

2.2 Device Structure

A schematic drawing illustrating the cross-section of a VCSEL fabricated in the array is provided in Fig. 2.1. All the epitaxial layers were grown on a 500 μm semi-insulating GaAs substrate. The VCSEL contains three quantum wells made by GaAs material (having a low bandgap) each of which is 8 nm in thickness separated by barrier layers made by AlGaAs material (having a high bandgap) each of which is 10 nm in thickness to form the heterostructure. It is obvious that the VCSEL designed in this configuration will be for top emitting since the substrate material (GaAs) is absorptive. This also leads to grow higher number of n-DBR (Distributed Bragg Reflector) mirror pairs than p-DBR mirror pairs in order to get a much higher combined reflection from the bottom n-mirror side so that light can emit from the top side. A Bragg mirror pair consists of two layers with high and low refractive indices where each layer has one quarter of wavelength thickness. By

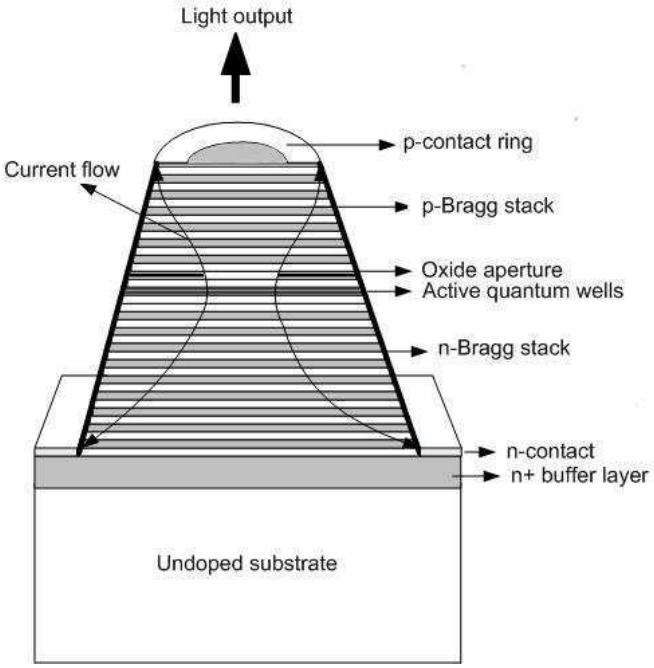


Figure 2.1: *Schematic cross-section of VCSEL structure.*

repeating these two layers in an alternating manner, constructive interference is achieved which ultimately increases the total reflectivity of the structure. In particular, these two layers are grown in this design with a graded interface just by varying the Al content; as a result, electrical resistance gets reduced. In this design the active region, i.e. three quantum wells along with barrier layers, is sandwiched by top 23 pairs of C-doped (p-type) mirror stacks and bottom 38 pairs of Si-doped (n-type) mirror stacks. Close to the active region, AlAs layer (i.e. high Al content) of 32 nm is grown to form the native oxide for current and carrier confinement. It is noteworthy that there is also a 2 μm highly doped n^+ buffer layer just at the top of the substrate is grown on which the n-contact will be photolithographically defined. Furthermore, a highly doped of some ten nm thick p^+ layer was also grown as topmost layer to facilitate the electrical conduction where the p-contact will be formed. In addition, the epitaxial layer structures of the sample used in this work is summarized in Appendix G.

2.3 Band Diagram

Fig. 2.2 shows the band diagram of the full VCSEL structure without any biasing, i.e. the Fermi level of n-region will remain completely aligned with p-region. The zoom-in showing of the microcavity active region is also provided in Fig. 2.2 where three QWs are located. But Fermi level misalignment will take place as soon as biasing is applied in the device which is shown in Fig. 2.3. This non-equilibrium condition resulting from the forward biasing can be depicted by so-called quasi-Fermi levels. Now the electrons will

be allowed to go into the QW from the n-region and holes from the p-region ultimately lead to stimulated action. These band diagrams with and without biasing are obtained by using the semiconductor simulation program SimWindows-V.1.5.0 (cf. appendix A).

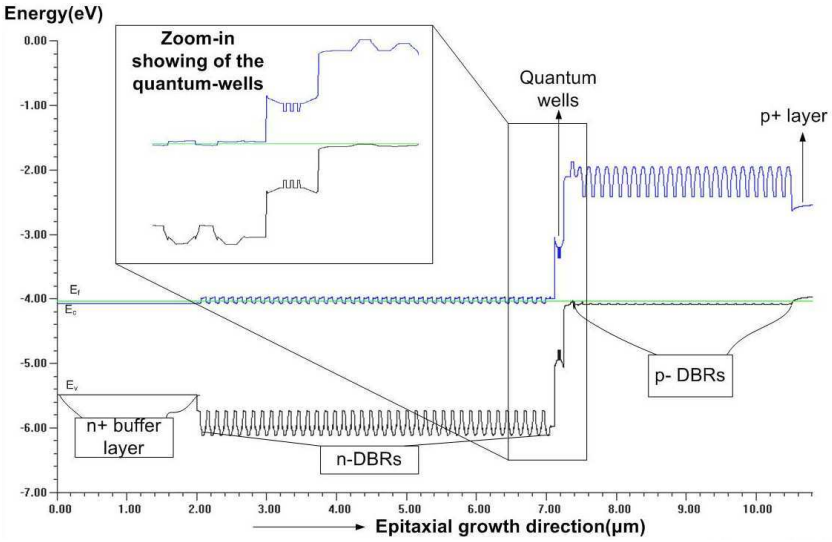


Figure 2.2: *Band diagram of the full unbiased VCSEL structure.*

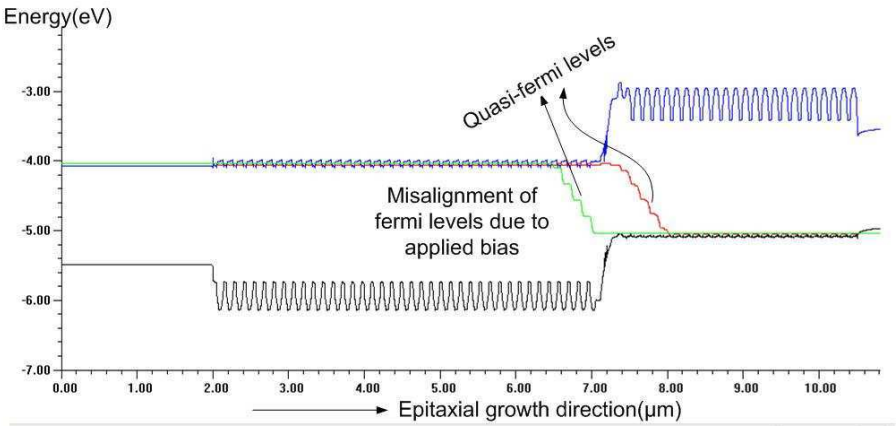


Figure 2.3: *Band diagram of the full VCSEL structure with 1 V forward bias.*

2.4 Refractive Index

The refractive index profile of the full VCSEL structure is shown in Fig. 2.4 where the active region with higher refractive index is surrounded by the region with low refractive index results the optical guiding. It is seen that in the Bragg reflectors there is no sharp interface, i.e. jumping from high refractive index to low refractive index directly; continuous grading

has been introduced instead, in order to reduce the potential barrier and thus the electrical resistance. This refractive index profile of the device can be calculated by using the same program SimWindows (cf. appendix A).

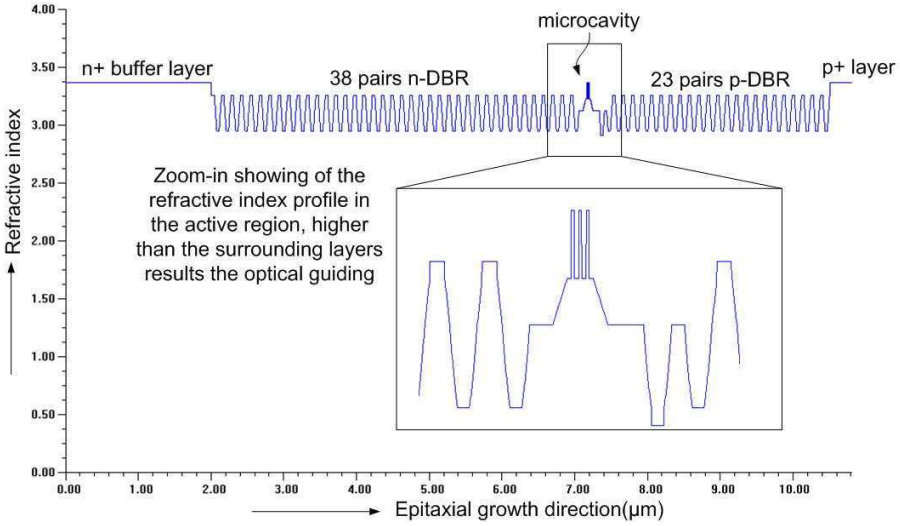


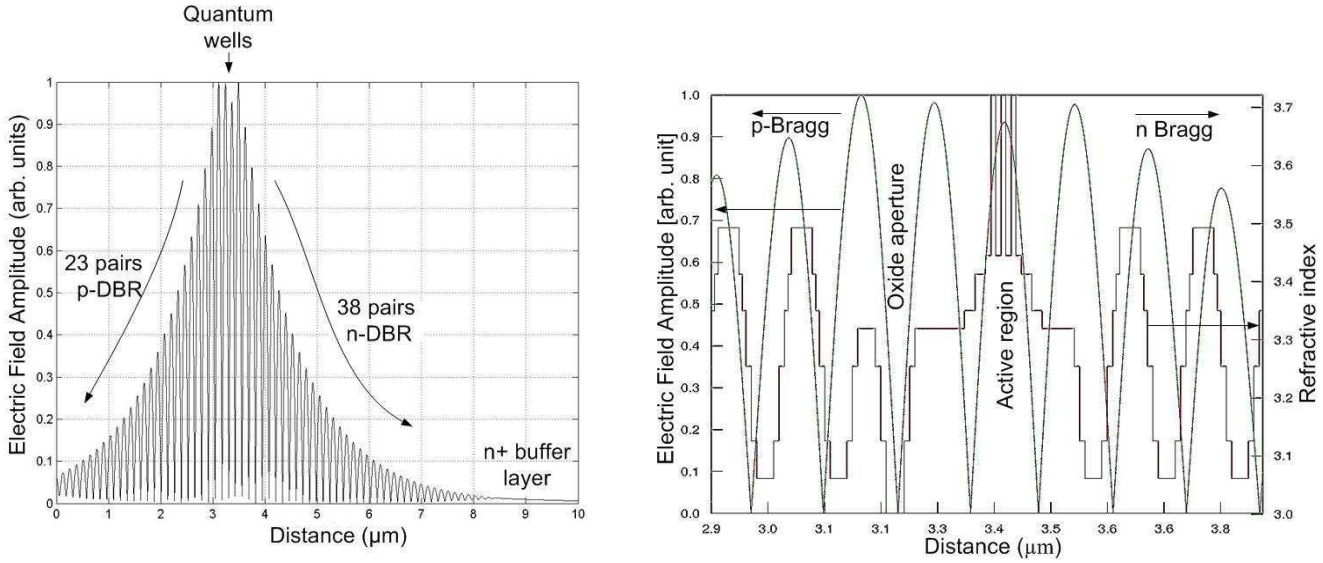
Figure 2.4: *Refractive index profile of the full VCSEL structure.*

2.5 Standing-Wave Pattern

Fig. 2.5(a) shows the standing-wave pattern of the electric field intensity of the full VCSEL structure that contains three active GaAs QWs in the center, 38 pairs bottom Bragg reflector, 23 pairs top Bragg reflector including n^+ buffer layer. It is obvious that there is pronounced resonating action produced in the device since the field amplitude is much higher at the active region due to higher reflectivities at the mirrors. On the other hand, the field amplitude gradually decays at both mirror side. Fig. 2.5(b) shows a close-up view of the same standing-wave pattern at the active region including the refractive index profile where we can see that the active region has been placed in such a position of the device where electric field intensity peak appears which necessitates the λ-length cavity. These two figures are obtained by using the one-dimensional simulation program REFLEX where the material recipe file (.INR file) was given as input. The necessary equations used to simulate this program are attached in Appendix B.

2.6 Reflectivity Spectrum

The reflectivity spectrum calculated from full VCSEL structure gives very important information about the lasing wavelength of the device. Fig. 2.6 shows the spectrum where we see the spectral width of the high-reflectivity stop-band which can be controlled by the materials employed. At the center of the stop-band we also see a dip, having a lower



(a) *Standing-wave pattern of the electric field of a full VCSEL structure.*

(b) *Standing-wave pattern close-up of the active region including the refractive index profile.*

Figure 2.5: *Standing-wave pattern of VCSEL.*

reflectivity, indicates the resonance wavelength just like a Fabry-Perot resonator. Though the emission wavelength designed for this sample was 850 nm which is standard for high speed data communication but due to many reasons, it is difficult to achieve this exact wavelength. This reflectivity spectrum was numerically calculated by transfer matrix method using MATLAB. The necessary equations implemented in the source code are given in Appendix C.

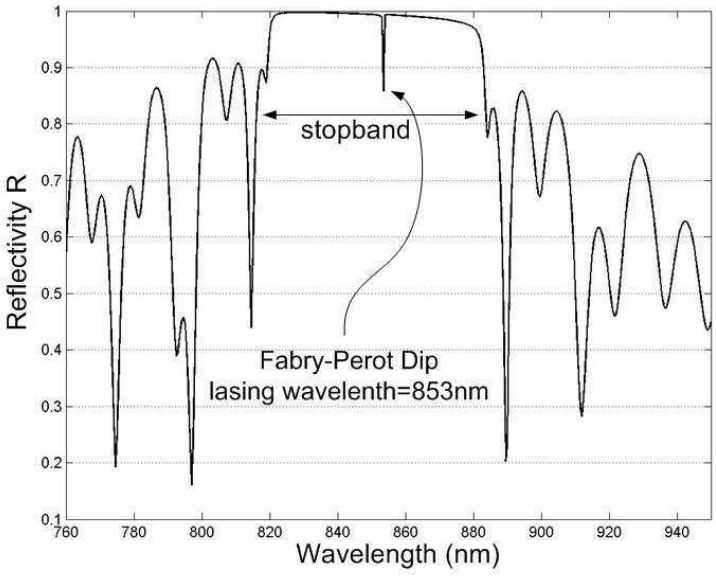


Figure 2.6: *Reflectivity spectrum of the full VCSEL structure designed for emission wavelength 850 nm. The reflectivity dip at the centre signifies the resonance wavelength.*

Just after the epitaxial growth, the measurement of reflectivity spectrum is extremely helpful because it tells about the emission wavelength to be obtained from the sample. In most practical cases, the emission wavelength at the center of the sample is not same with the periphery of the

sample; some deviation was noticed for this sample.

2.7 Summary

In this chapter, the important modeling parameters of VCSEL have been presented based on the epitaxial layers. The importance and the significance of these parameters are also briefly discussed in this chapter. In addition, the simulated outputs for these parameters obtained by using the different software are inserted here.

Chapter 3

2-D VCSEL Arrays

3.1 Introduction

Producing the VCSELs as an array in single chip containing thousands of VCSELs is not difficult at all. The technology of 1-D and 2-D VCSEL array fabrication in the last decade have advanced rapidly just because of the ease of producing 2-D VCSEL array. Why 2-D VCSEL array is important? 2-D VCSEL array has plenty of major applications; optical interconnection is one of the most important applications, beside the parallel data processing over optical fiber for short distance communication, optical data storage and so on. In fact, for short distance data transmission where the number of coupled elements will be needed, VCSEL has become the first choice as a device there nowadays. But the problem arises when the time comes to communicate them, i.e. each of the VCSEL in 2-D VCSEL array need to be addressed. So far work has been carried out on four different addressing schemes. Those are as follows:

- Independent addressing
- Matrix addressing
- Direct addressing
- Optical addressing

Out of these different addressing schemes the first two methods have been demonstrated by many people many times on many applications.

In this chapter, the principles of different addressing techniques for 2-D VCSEL array along with their merits and demerits have been summarized. In addition to that, the strategies of fabricating the matrix addressable arrays in this thesis work is discussed including some schematic diagrams from which one can easily get some feelings of the whole work.

3.2 Independent Addressing

This is the most straightforward way of addressing the VCSEL in an array which is schematically illustrated in Fig. 3.1. In fact, this type of addressing needs a p-contact at the top of the devices. That's why the metallic traces have to be defined for each VCSEL which will connect the anode of the device to the bondpad located at the edge of the chip. On the other hand, the bottom doped substrate (ground contact as common) can be used for n-contact of all devices. Array of this kind has been demonstrated by Von Lehman *et al.* [13] in 1991 and Giaretta *et al.* [14] in 1997 and Hendrik Roscher [15] in 2002 and so on.

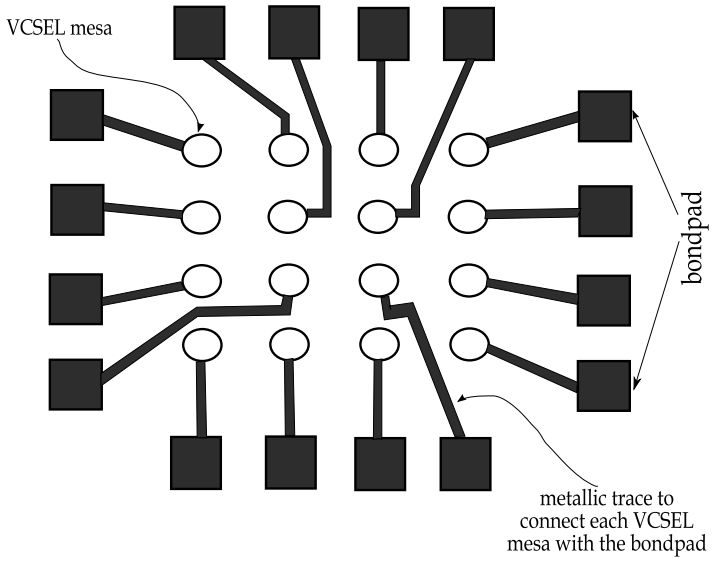


Figure 3.1: *Schematic diagram of metallization pattern for 4 x 4 individually addressed array.*

3.2.1 Advantages

1. Each of the VCSEL can be operated independently, i.e. any single device, any combination of the device and all of the devices can be turned on at the same time without any additional circuitry.

2. 2-D array fabrication is comparatively easier.

3.2.2 Disadvantages

The array size will be limited due to the complicacy created by many bondpads and metal traces. Because for each VCSEL there will be one dedicated metallic trace and bondpad should be defined. In a generalizing way, for M x N array, we will need M x N metal lines and the same amount of bondpads, obviously a big number which require a lot of space in the chip.

3.3 Matrix Addressing

This is another promising method for addressing the VCSEL in the 2-D array. This type of addressing is little bit complicated because each device will not have its own independent metal line and bondpad connection to be turned on, but common cathode and common anode connection will be defined in column and row for addressing the device, instead. Fig. 3.2 demonstrates the schematic diagram of the typical metallization pattern of 4 x 4 matrix addressing. In fact, a VCSEL located at the intersection of the n-metallization line and p-metallization line will be turned on in this method. In most practical cases, the p-contacts of the devices over a row and the n-contacts of devices down a column are connected together. Then by applying a positive voltage to the desired row and an equal negative voltage to the column, the VCSEL at the intersection would be turned on. Array of this kind has been demonstrated by Von Lehman *et al.* [10] in 1991, Morgan *et al.* [11] in 1994 and Choquette *et al.* [12] in 2002 and so on.

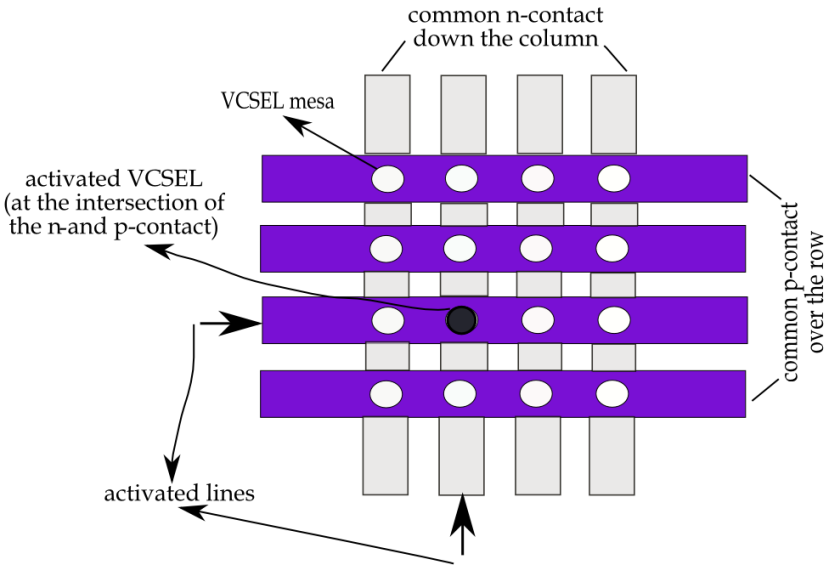


Figure 3.2: *Schematic diagram of metallization pattern for 4 x 4 matrix addressed array.*

3.3.1 Advantages

1. It is already understood that the main problematic issue in the 2-D VCSEL array is that the number of metal traces and bondpads to communicate the single or multiple VCSELs. The larger the array, i.e. the higher number of VCSELs, the higher the complicacy because more metal lines and bondpads would be needed then which can be realized by the independent addressing. Matrix addressing in this case shows a magnificent performance by reducing the number of metallic traces and bondpads. In a generalizing way, for M x N array, we will need M + N metal

lines and the same amount of bondpads, obviously much less than the independent addressing which saves a lot of space in the chip lead us to fabricate a large array (e.g. 32 x 32 array). To fabricate 32 x 32 array, only 32 + 32=64 metal lines are required in matrix-addressable array whereas 32 x 32=1024 metal lines are required in individually addressable array, i.e. 960 would be needed additionally - really a lot. This is the supremacy of Matrix-Addressing method over Independent-Addressing.

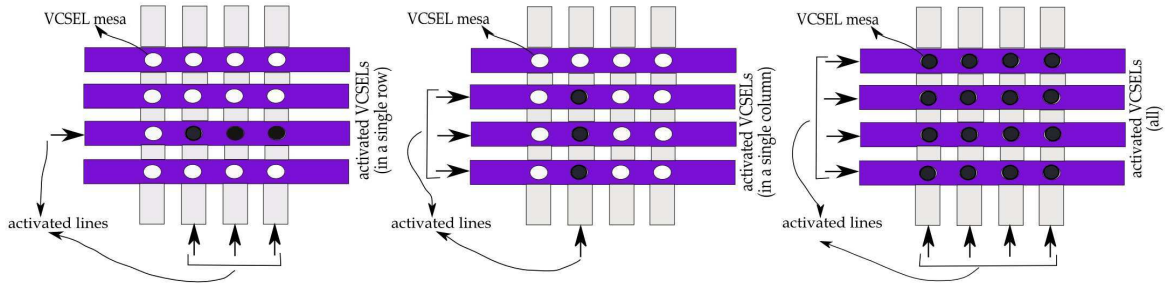


Figure 3.3: *Different schemes of Matrix Addressing technique to address the devices. Any number of devices in a single row (the leftmost), in a single column (at the middle) and all the devices at a time (the rightmost) can be turned on.*

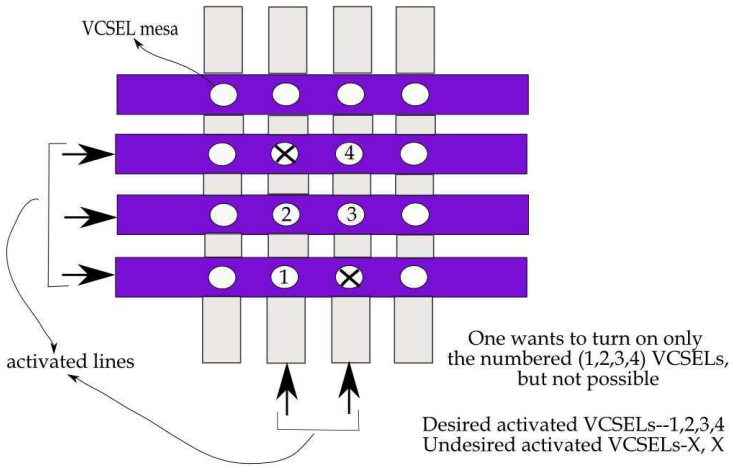


Figure 3.4: *Limitation of matrix addressing technique where we can see that random multi-element addressing over the array is not possible.*

2. Chip size can be minimized since less number of bondpads will be required.

3.3.2 Disadvantages

1. The main disadvantage in this type of addressing method is that the lack of controlling the VCSELs in the array. Matrix addressing allows only the following schemes

in the array:

- Single VCSEL (Fig. 3.2)
- Any number of VCSELs in a single row or in a single column (Fig. 3.3)
- All of the VCSELs at a time.(Fig. 3.3)

So, it is clear that random multi-element addressing is not possible here as shown in Fig. 3.4. But some additional circuitry (e.g. multiplexer) can help to operate the VCSEL array randomly which involves cost and effort and may be complicacy will get increased. For example, any character is formed by multiplexing the display

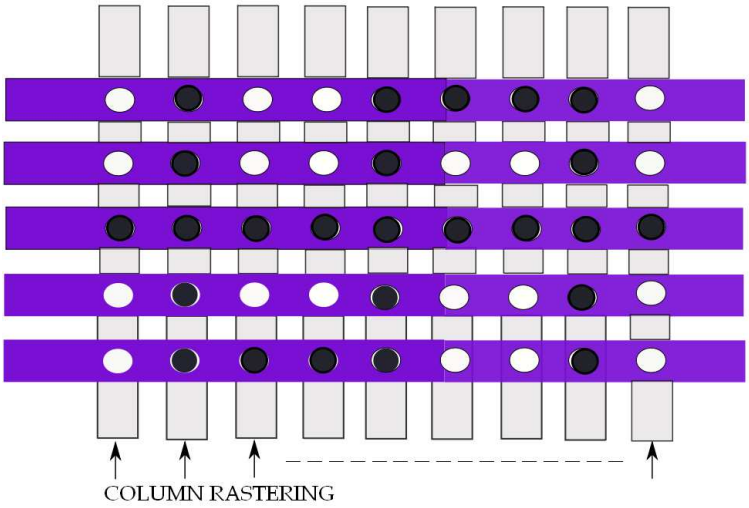


Figure 3.5: *Photograph of the symbol '$'(rotated by -90^0) produced by column-row rastering the laser array.*

columns with the scanning logic. Each of the nine columns (shown in Fig. 3.5) are selected individually while placing the data in the character generator for that column on the rows. This process is repeated until all columns of the matrix have been activated [11]. In this way, matrix addressing overcomes the limitation mentioned earlier.

2. 2-D array fabrication is not so easy.

3. The p-contacts of devices along a row and the n-contacts of devices down a column are connected together. Then by applying a positive voltage to the desired row and an equal negative voltage to the column, the VCSEL at the intersection would be turned on. Other devices along the row and down the column would see only the half voltage of this device. It is necessary to make sure that the threshold voltage of all devices fabricated in the array has to be less than half of the desired operating voltage [16].

4. One of the most challenging issues in MA[1] VCSEL arrays is the larger effective series resistance [12].

3.4 Strategy of MA Array Fabrication

How the sample will be processed and what strategy (the process sequences) will be followed for fabricating the MA VCSEL array in an optimized way, the rough blueprint of that was determined in advance especially before drawing the mask. Of course, it will help us to understand and to develop some feelings about the present work. The following discussion provides the information of the planning regarding the processing steps, starting from the mesa formation just after getting the sample till the last step of the metal contact.

According to the proposed method, at first, the sample will be etched down till n^+ buffer layer (8-9 μm deep) resulting the mesa of the devices as indicated in Fig. 3.6. Then those devices can be selectively oxidized for current and optical confinement. Later, the sample should be metallized selectively which will serve as common n-contact so-called column pad area. In fact, the n-contact metallization should be done down the full column (except the circular device region) on top of the n^+ buffer layer. This process will be followed by the etching for the column isolation grooves by removing the n^+ buffer layer which will electrically isolate the columns as displayed in the upper part of Fig. 3.6. Now the passivation between n- and p-contacts and planarization of the sample surface should be made by the polyimide. In carrying out the planaraization of the sample, the trenches so-called column isolation grooves defined by etching (mentioned earlier) should be filled-up at first as shown in the lower part of Fig. 3.6. Then the rest of the region should be planarized by the thicker polyimide which resulted from the deep 8-9 μm mesa etching as indicated in the upper part of Fig. 3.7. Lastly comes the metallization for p-contact. For that, row pad areas have to be formed which will act as common p-contacts of the devices located in one row as illustrated in the lower part of Fig. 3.7. Note that, the p-contact metallization should be done over the full row except the small circular region where the devices are located so that light can escape from the top of the device since the design is based on top emission.

[1]MA = Matrix Addressable

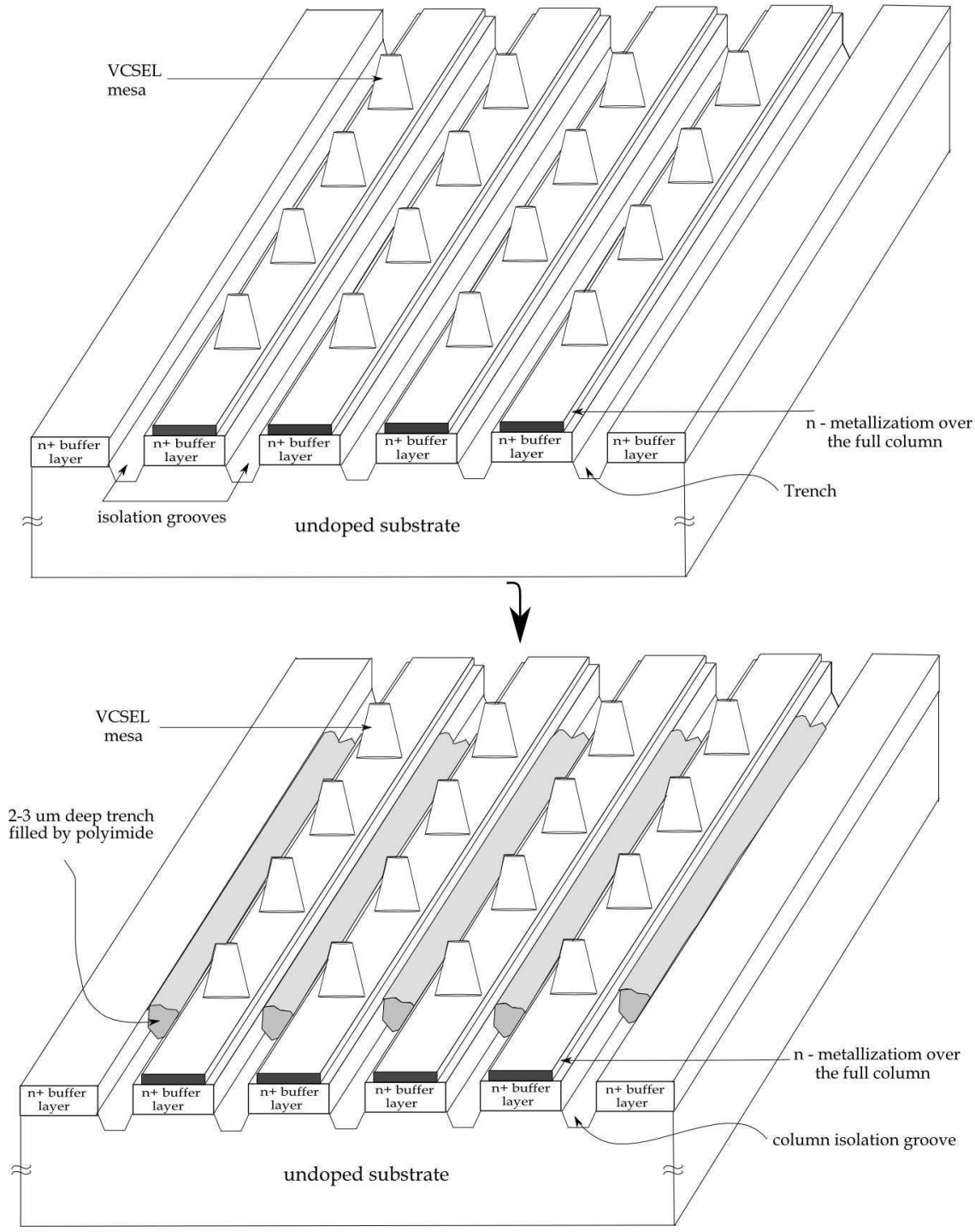


Figure 3.6: *Illustration showing the fabrication procedure of 4 x 4 VCSEL arrays where the formation of the mesa, column pad area for common n-contact of the devices, isolation trenches in the above figure and then the way of filling-up the trenches by the polyimide in the lower figure.*

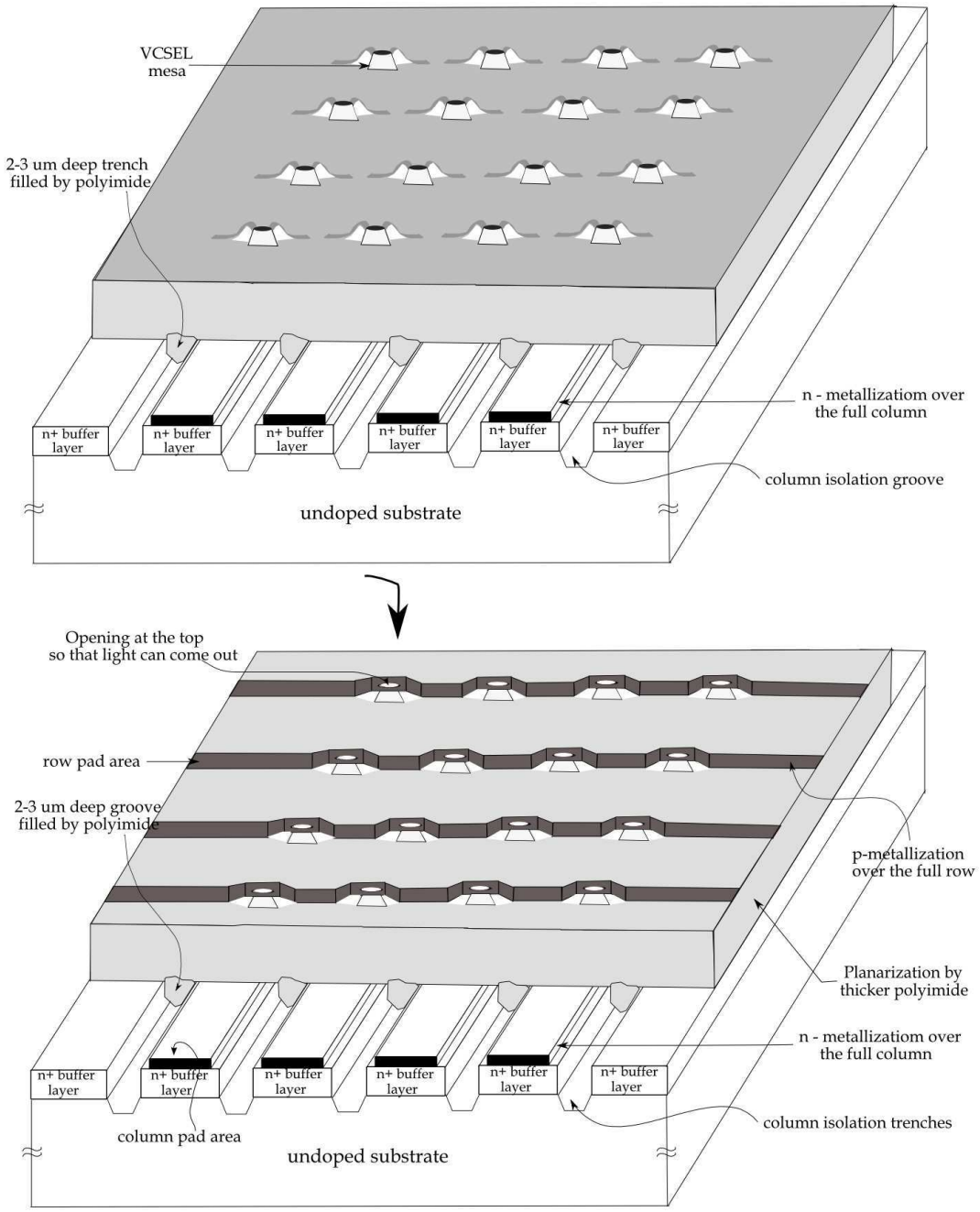


Figure 3.7: *Illustration showing the fabrication procedure of 4 x 4 VCSEL arrays where the selective planarization of the sample surface having 8-9µm deep etched region by the thicker polyimide in the above figure and the formation of row pad area for common p-contact of the devices in the lower figure.*

3.5 Summary

In this chapter, the important discussion concerning the matrix addressable array and its supremacy over other addressing techniques have been presented with some illustrations. Besides, this chapter will be followed by the 'Mask Design' where the design approaches will be discussed directly assuming that one has already the understanding about the basic theories and the design approach of this thesis work. Moreover, this chapter will be very helpful to follow the ideas, views and comments introduced in the next chapter. Finally, a very brief summary of the basic steps for processing of the MA array including some schematic diagrams are outlined here.

Chapter 4

Mask Design for Matrix Addressable Array

4.1 Introduction

In designing the matrix addressable VCSEL arrays, the first and the most important task is the mask design which needs high accuracy especially in dimension of the structures. The mask contains the high resolution transparent-opaque images on one side of the surface which is required to get a certain pattern on the sample. In particular, the important factors (e.g. lateral undercut of wet chemical etching), special parameters of different photolithographic steps (e.g. alignment in mask aligner) need to be considered in the mask design in order to get a good yield of the devices. So, the mask design plays an important role in fabricating the devices successfully.

Traditionally, for the layout of the mask the computer aided design tool, AutoCAD[2] was used. AutoCAD produces the data format .DWG file which is converted into GDSII file by the manufacturer company to write the structure on Quartz glass[3] by E-beam lithography.

Fig. 4.1 shows the entire layout of the mask drawn in the AutoCAD. There are eight blocks in the layout which implies that eight or may be more than eight photolithographic steps are necessary to fabricate the matrix addressable VCSEL arrays. The dimension of each block is 1.55 cm by 1.55 cm which is sufficient to cover the half of the quarter of 2" wafer. Or in other words, half of the quarter of 2" wafer can be processed by each block of the mask. In addition, the name of each block in the layout will tell the purpose of corresponding block which has to be carried out in the fabrication. Moreover, the blocks of the layout were designed to be usable with both type of photoresist, positive and negative, depending on the requirements. The details of the design can be viewed by zooming in

[2]Some handy tips of drawing the mask layout efficiently in AutoCAD are given in Appendix D which might be helpful for the beginners.

[3]Quartz is the second most common mineral in the Earth's continental crust. It is made up of a lattice of silica SiO_2 tetrahedra. Source:-http://en.wikipedia.org/wiki/Quartz

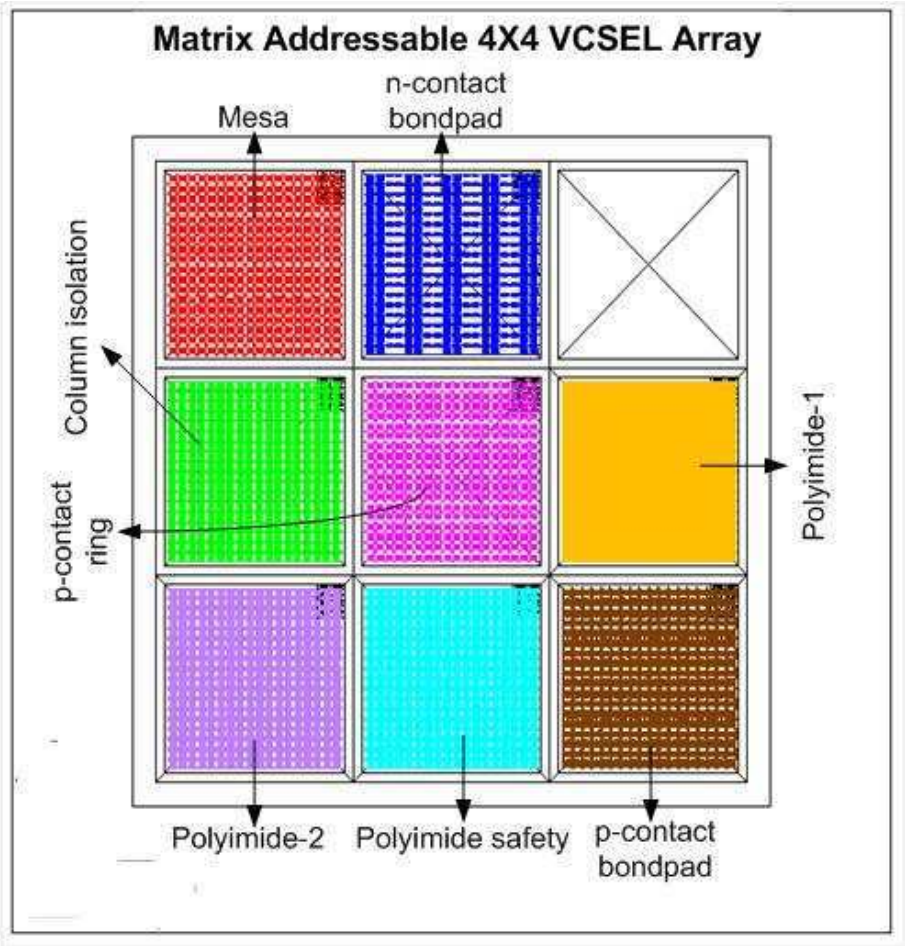


Figure 4.1: *Entire layout of the mask drawn in AutoCAD, there are eight different blocks defined for eight different photlolithographic steps for processing the Matrix Addressable 4 x 4 VCSEL Array.*

on the typical three-inch mask as displayed in Fig. 4.1.

In this chapter, the description of the mask design along with the necessary explanations, the relevant issues taken into account, the dimensions of the structures drawn in the layout are outlined including the figures. It should finally be noted that this was a prototype photomask that was designed to conduct the processing which can be the harbinger of next work.

4.2 Mask for Mesa Etching

The name of this block itself is telling that the mesa of VCSEL arrays will be formed by etching (e.g. wet chemical etching) to expose the AlAs layer for oxidation which is 3/4 µm in depth - quite conventional, but in this step we etched down till n^+ buffer layer instead of

just AlAs layer to avoid the difficulty. Difficulty in this sense that the different etch depths will create some problem in getting the surface planarized afterwards. For example, if we would make the etching upto AlAs layer in this step and then anyway we have to etch till n^+ buffer layer and then again etching is necessary to isolate the columns resulting three different etch depths.

The four VCSEL arrays of each having 4 x 4 structures with different mesa diameters are shown in Fig. 4.2. Each 4 x 4 array will be called as one unit cell from now. However, the advantage of etching down till n^+ buffer layer is that the sample becomes completely ready for oxidation and at the same time for the latter step, n-contact metallization without any further processing, e.g. wet chemical etching. Besides, there are four alignment marks at the corner of each array as well, which will help to align the structures with the structures defined already in the sample by the earlier photolithographic step. The shaded part as displayed in Fig. 4.2 indicates that the region covered with chrome which will block the UV light during UV exposure. So, the shaded region will be protected by the resist after development if positive resist is used.

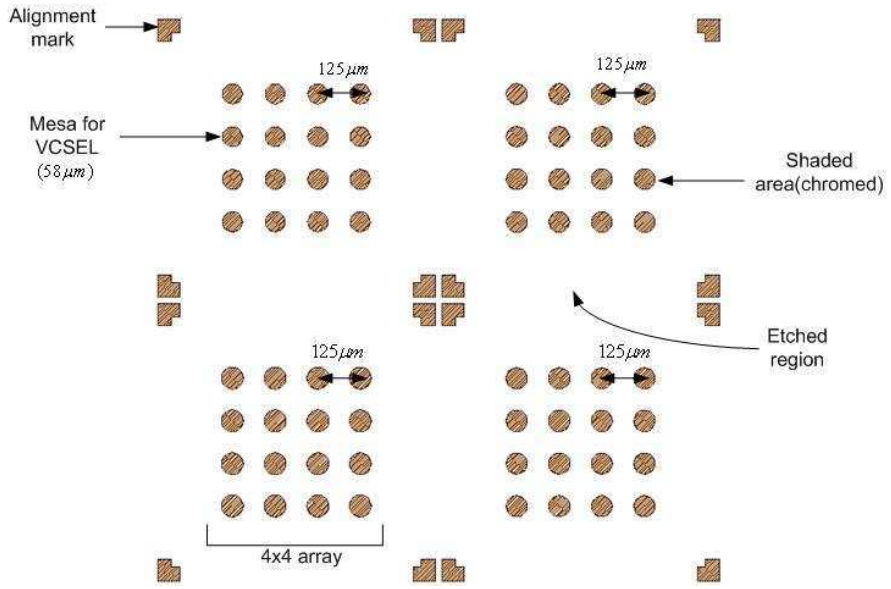


Figure 4.2: *Close-up showing of the block, MESA, in the mask layout.*

In this mask the four different circles distinguished by the dimensions, i.e. 58 μm, 60 μm, 62 μm and 64 μm in four different regions separated by alignment markers are drawn. The circles of these different dimensions will give the active diameters 4 μm, 6 μm, 8 μm and 10 μm respectively after oxidation which are necessary for the following reasons:

1. Standard for data communication used in short distance fiber-optical links.
2. Single mode[4]

[4]Yang *et al.* reports that the 10 μm square laser with the special type of epi-layer structure operates in a

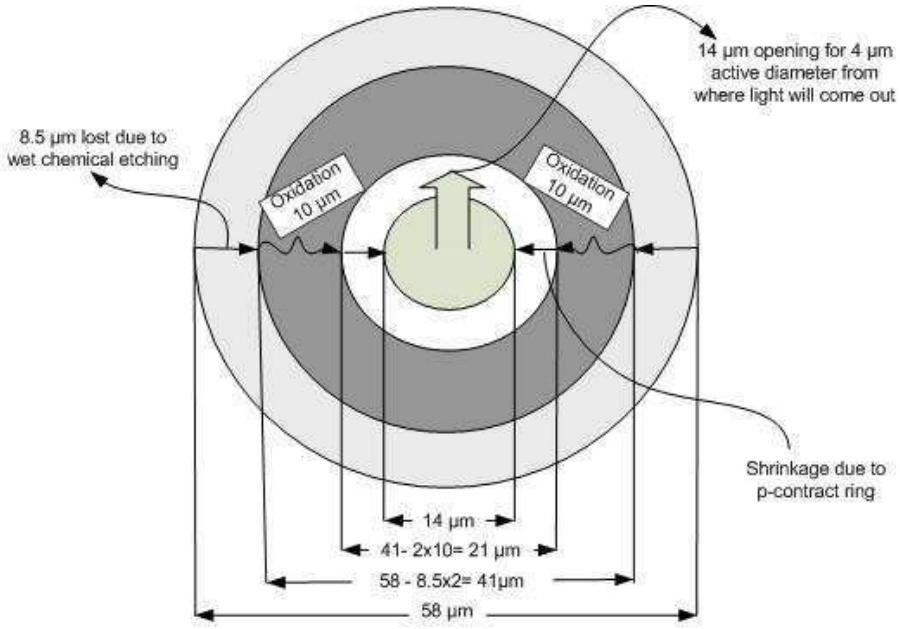


Figure 4.3: *Explanation of the dimension used in calculating the mesa circle diameter.*

3. Gaussian beam allows simpler optics.
4. Less heating problem since less threshold current is necessary.
5. Excellent device reliability.

Why the circle, having the diameter 58 µm, is drawn in the mask to get the active diameter 4 µm? There are some factors which were considered to calculate this dimension mentioned below:

- Lateral undercut for wet chemical etching
- Oxidation
- p-contact ring
- Safety factor

These are illustrated in Fig. 4.3.

4.3 Mask for N-Contact Bondpad

The n-contact metallization for matrix addressable arrays is also quite different from the conventional one because this metallization will not be done in the whole backside of the wafer, one full column except the region of the device or only the rectangular areas at the

single mode with 20 dB of transverse mode suppression [1].

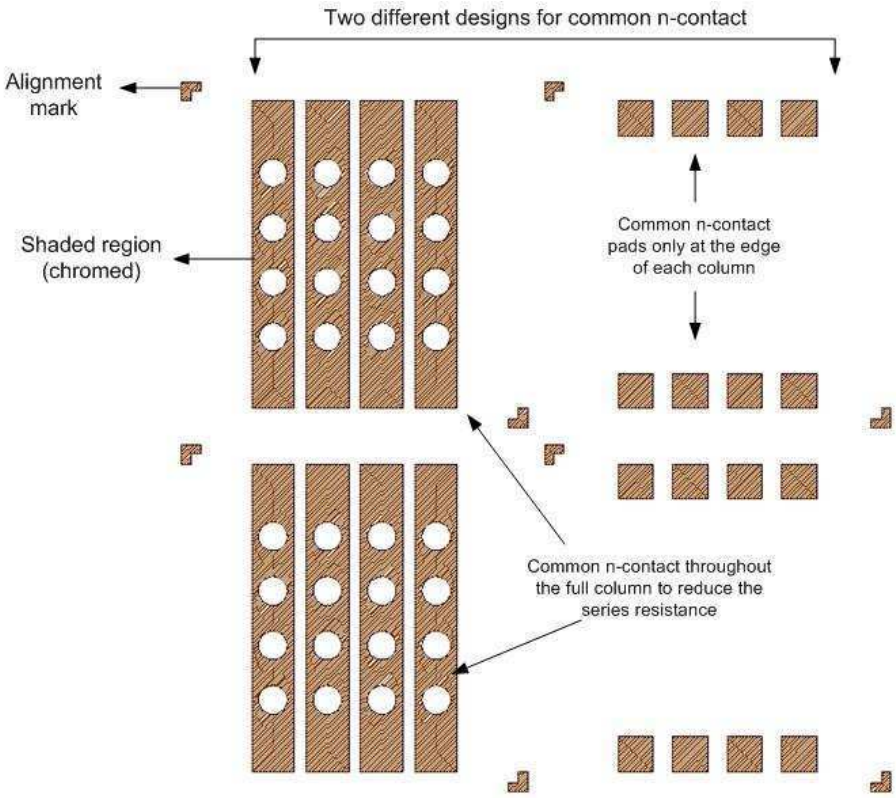


Figure 4.4: *Close-up showing of the block, n-contact bondpad, in the mask layout where there are two different designs.*

edge like bondpad will be metallized, instead. Actually, the overlying n^+ layer on top of the semi-insulating substrate will be patterned by this mask.

One of the most challenging issues in Matrix Addressable VCSEL arrays is the larger effective series resistance [12]. Taking this into account, two different types of n-contact metallization were designed. One of them is the metallization over the full column except the VCSEL circular region (left part of Fig. 4.4) which is very good from the viewpoint of series resistance. Another is just at the edge of every array like bondpad (right part of Fig. 4.4) where the needle will be placed on for electrical conduction. In addition, to reduce the series resistance, the bondpads were provided in both sides, i.e. top and bottom side of the arrays results increasing the total number of cathode bondpads to 8 instead of 4 for 4 x 4 array.

There are two alignment markers at the opposite corner of each array instead of having four because these two alignment markers (shown in Fig. 4.4) will help us in aligning the profiles with the profiles of the subsequent steps which may not be correct since the alignment markers produced at the mesa formation step is the most correct one, like a reference. These will be visible in the next steps as well even if we do not make any met-

allization which can be helpful for alignment purpose. In other words, the two alignment markers in n-contact metallization step will be metallized and the other two alignment markers (not drawn in Fig. 4.4) already produced in the mesa formation step will be visible which will be quite helpful during the alignment from the third photolithographic step.

Since this is a metallization step, we need to design the mask in such a way so that we can get the negative tone, i.e. shaded area will not be protected by resist, consequently only the shaded area will be metallized. The negative tone is very necessary to get a negative slope of the resist which ultimately makes the lift-off process easier.

4.4 Mask for Column Isolation

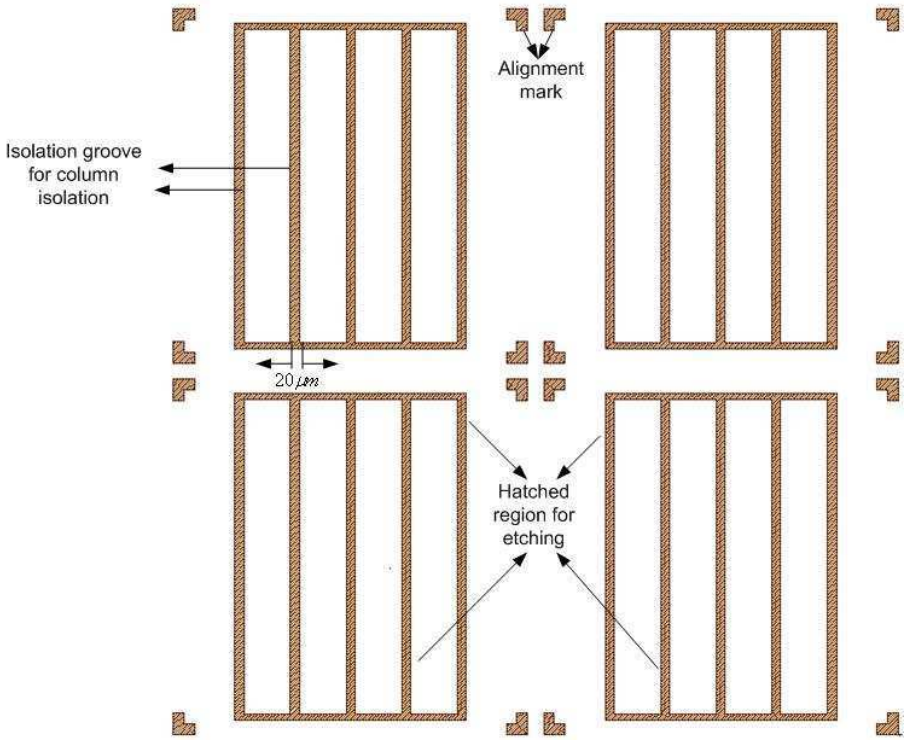


Figure 4.5: *Close-up showing of the block, Column Isolation, in the mask layout.*

This mask is also for etching but not so much deep like mesa etching, only 2-3 μm will be etched here. This etching will help us to reach into the undoped (intrinsic / insulating / not conducting) substrate by removing the n^+ buffer layer in order to isolate the four columns of 4 x 4 arrays. In this way, the four columns will become separated electrically by defining the trenches of width 20 μm. It should be stressed that not only the five vertical lines are drawn but also the horizontal lines at the top and bottom are necessary for perfect isolation between adjacent columns as demonstrated in Fig. 4.5.

This mask was designed for using the negative photoresist. Accordingly, the shaded area, i.e. chromed region will be ready for etching down till insulating substrate which implies that all the region except the chromed ones are protected by resist after development. As an alternative, the opposite design could be done, that is most of the region except the columns will be covered by chrome which forces to use the positive photoresist in order to get the desired pattern. If it were the case, then we would have faced a great problem in aligning by the mask aligner. Because large region covered by chrome in the mask means that the structures in the sample (already defined in the 2nd lithographic step) will not be clearly visible under the mask during the alignment. Because the chromed region will block to see through over the sample.

4.5 Mask for P-Contact Ring

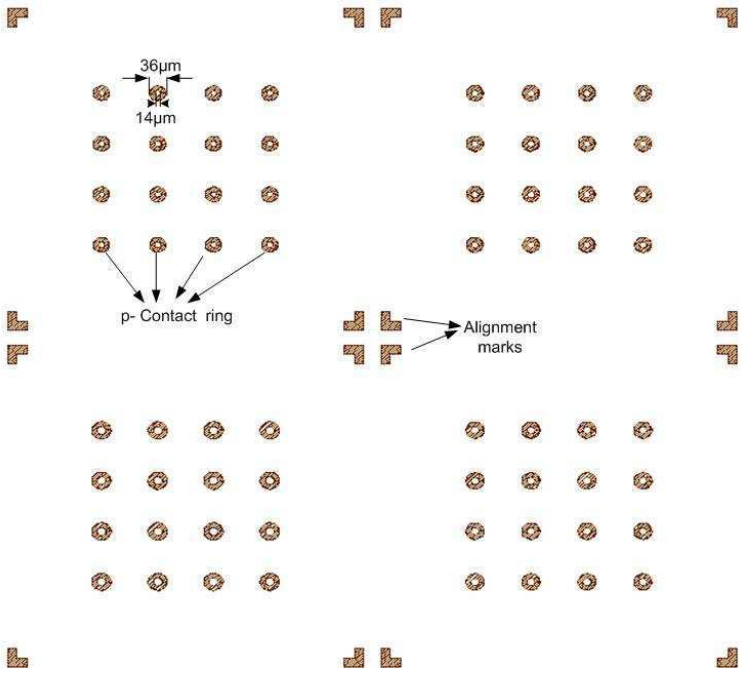


Figure 4.6: *Close-up showing of the block, Contact ring, in the mask layout.*

This mask is just for the metallization of the p-contact ring of each individual device. The aperture window in the contact ring must be included to allow the beam to escape. There are four different types of ring sizes as shown in Fig. 4.6 depending on the size of the mesa diameters.

It is clear that the shaded area will be metallized here as usual. The design for the contact ring with an outer diameter of 36 µm and inner diameter of 14 µm for the mesa diameter of 58 µm (the smallest one), whereas the mesa diameter size after etching till n^+ buffer layer will be like 41 µm for the first approximation since the lateral undercut is almost equal to

the etching depth. We are getting 2.5 μm in both sides as tolerances which will ultimately help us for good alignment in the mask aligner. The dimensions of the four alignment marks at the corners of each array have to be modified which should be different from the previous photolithographic step due to the lateral undercut in wet chemical etching there.

4.6 Mask for Polyimide-1

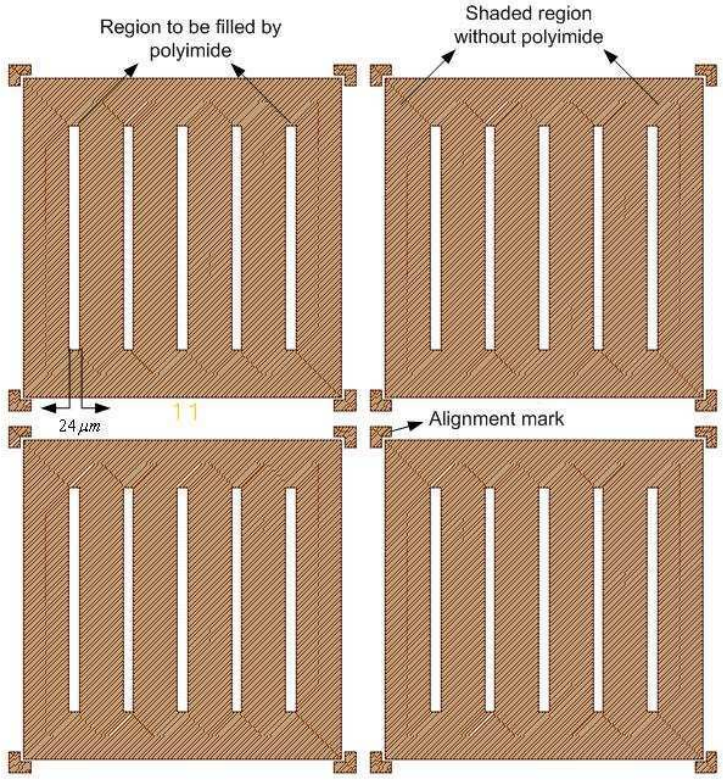


Figure 4.7: *Close-up showing of the block, Polyimide-1, in the mask layout.*

Now it is the time to planarize the surface by polyimide before the formation of the row pad area providing common p-contact. In addition to the surface planarization, polyimide plays also an very important role in facilitating the top contact metallization leads to prevent the short circuit by isolating from n-contact.

There are two different etch depths, one results from the mesa etching and another is from the trenches for column isolation. Basically this mask is designed for the latter one by which the trenches can be filled by the polyimide which is part of the first planarization. Logically, the name of the mask has been kept as polyimide-1 which will fill-up the only column-isolation grooves, i.e. 2-3 μm in depth.

From Fig. 4.7, we see that there are two different regions, shaded (should be covered by chrome) and unshaded, where the unshaded region will be filled by polyimide since the polyimide shows the behaviour like negative resist, i.e. the exposed area will be insoluble to the developer. Thus, the partial planarization by polyimide will be done in this step. Note that, the width of each column, i.e. unshaded area, is 24 μm which will be filled by polyimide (shown in Fig. 4.7) little bit wider than the trenched region, i.e. 20 μm due to the usage of the negative photoresist in the step, "column isolation" discussed in sect. 4.4.

Large region covered by chrome in the mask creates a problem during the alignment, mentioned earlier. But the opposite design is not possible in this case since the polyimide behaviour can not be made as positive tone.

4.7 Mask for Polyimide-2

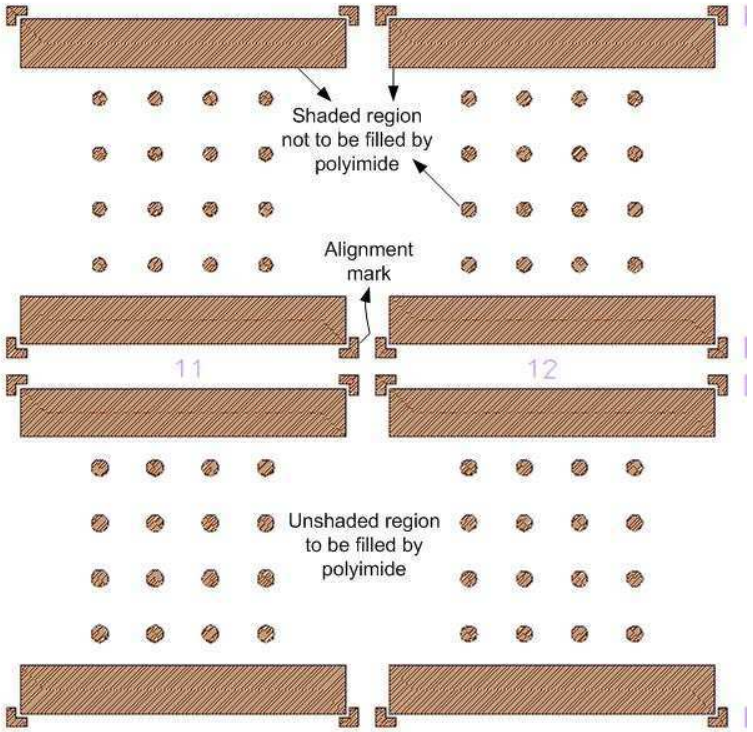


Figure 4.8: *Close-up showing of the block, Polyimide-2, in the mask layout.*

In the next polyimide mask the rest of the region which is 7/8 μm down from the top of the mesa has to be planarized by spinning the thick or thin polyimide (if thin polyimide, using multiple times) and then removing the polyimide from that region photolithographically defined by this mask. Fig. 4.8 shows that, this polyimide mask contains circles with four different dimensions in four different arrays which indicates that the VCSELs top part from where the light will come out and two rectangles at the two opposite sides where

the underlying n-contact pads are located will not be covered by polyimide.

However, the overlap between the p-contact ring (the outer circle diameter is 36 μm) and the polyimide mask-2 (the circle diameter is 31 μm) is 2.5 μm in both sides. It is known that here, also the unshaded area (shown in Fig. 4.8) like the polyimide-1 step are filled-up by the polyimide.

4.8 Mask for Polyimide-Safety

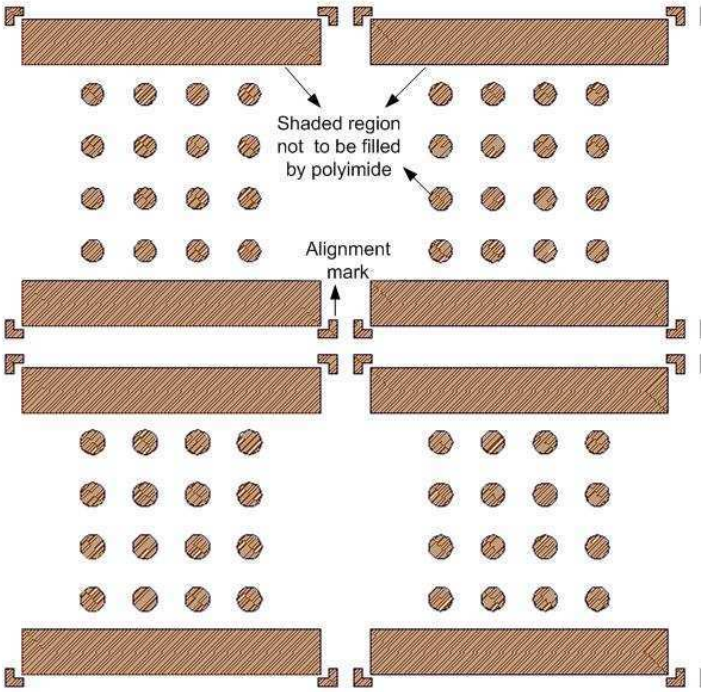


Figure 4.9: *Close-up showing of the block, Polyimide-safety, in the mask layout.*

This mask is designed just for safety. Because while designing the mask it was not certain that how many masks will be needed for planarization. Or in other words, how many steps should be carried out in planarizing the surface that was unsure. It is true that, the lesser the number of steps , the lesser the time and effort will be needed and the higher the yield of the devices on the sample. Because more lithographic steps or more processing obviously degrade the quality of the sample and some devices might get damaged in each processing. So it is recommended that the number of steps should be as less as possible. On the other hand, plnaraizing the surface in a single step staying from 8-9 μm down is not so easy task. Because filling-up so much depth by the polyimide will result some undesired effects like metal breaking (discontinuity of metals after p-metallization) due to extra raise in the mesa overlap region or due to lowering of the polyimide beside the mesa

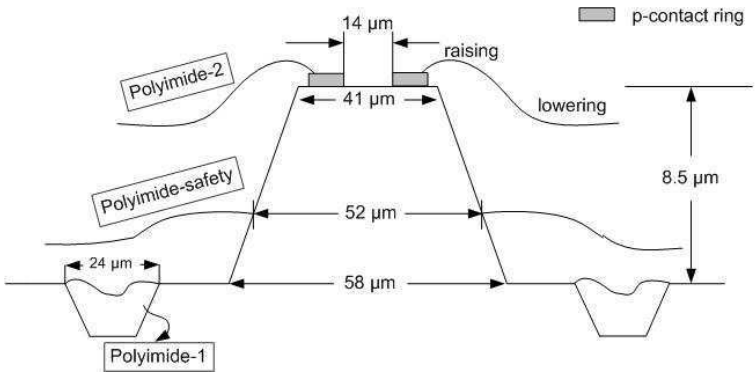


Figure 4.10: *Schematic diagram of the design of different polyimide masks including the dimensions.*

top. In order to reduce the uncertainty one extra mask, polyimide safety mask (shown in Fig. 4.9) is designed. The shape of this mask is exactly the same like polyimide-2 but differs from the dimension of the circle diameters. Basically this mask is designed by planning the planarization steps of polyimide in three steps. So the circle diameter has a greater dimension which indicates that half of total etch depth (8-9 µm) will be filled-up by the polyimide in this step. Then the rest will be done by polyimide-2.
Moreover, how the planarization by the polyimide will be done in three steps and where the "polyimide-safety" will play a role that have been demonstrated in Fig. 4.10.

4.9 Mask for P-Contact Bondpad

This mask is for the p-contact metallization over the full row and at the same time maintaining some isolation between the devices of two adjacent rows. The shaded areas, i.e. the row pads areas except the small circles inside will be metallized as displayed in Fig. 4.11. In fact, the circles inside the row pad areas will be just the opening of each VCSEL which is 18 µm (mesa diameter 58 µm) in diameter whereas 14 µm is the inner diameter of p-contact ring. This 2 µm in both sides is just for tolerance from alignment point of view. So ultimately 6.5 µm is the overlap between the p-contact ring and p-contact bondpad which is sufficient for electrical current conduction. Of course, the higher the overlap, the better the performance in conducting current through the devices. But the pitch size of the devices which are 125 µm - the limiting factor in this case.

In a tabular format, the diameters of the circles for different photolithographic steps drawn in the mask layout (starting from the mesa till p-contact circles inside the p-contact bondpad) are summarized in Table 4.1.

In addition, the same information has been illustrated in Fig. 4.12 schematically.

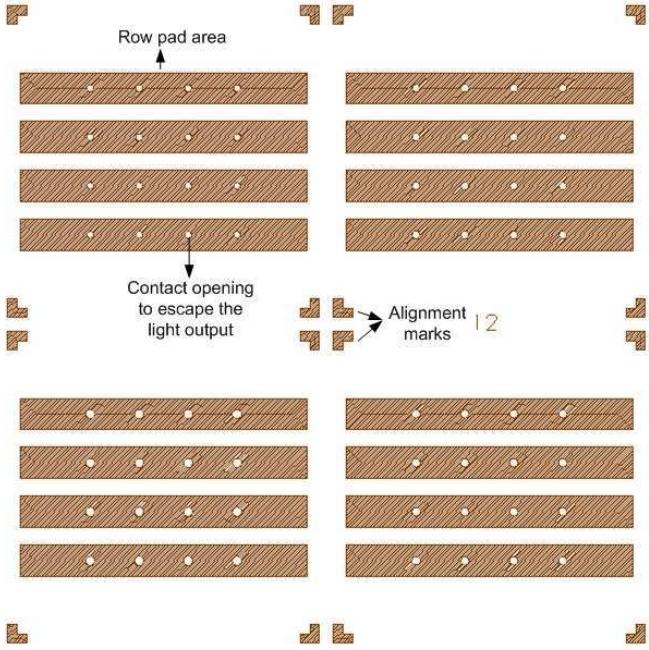


Figure 4.11: *Close-up showing of the block, p-contact bondpad, in the mask layout.*

Mesa(μm)	n-contact (μm)	p-contact ring (inner-outer) (μm)	Polyimide-2(μm)	Polyimide-safety (μm)	p-contact (bondpad) (μm)	Output (active) (μm)
58	62	14-36	31	52	18	4
60	64	16-38	33	54	20	6
62	66	18-40	35	56	22	8
64	68	20-42	37	58	24	10

Table 4.1: *Dimensions of different circles drawn in the mask layout in a tabular format.*

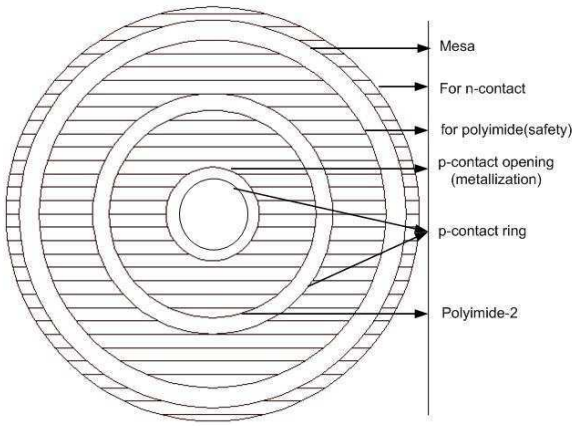


Figure 4.12: *Schematic diagarm of the dimensions of different circles drawn in the mask layout.*

4.10 Summary

In summary, the mask design approach for fabricating the Matrix Addressable 4 x 4 VCSEL array has been presented in this chapter. This prototype mask design, discussed in this chapter, inevitably will help to fabricate these arrays very successfully in the next future. Because all important issues need to be considered while designing the mask, all the problems which might come in fabricating this array are also outlined in this chapter.

Chapter 5

Matrix Addressable Array Fabrication

5.1 Introduction

Now VCSEL array needs to be fabricated depending on the designed mask. In fact, this is the most important and critical step where real problems have to be handled with great intelligence because the design what we implemented in the mask that can not be changed any more. Thus, keeping the mask structures completely unchanged and facing plenty of practical problems, the processing should be continued in order to get the arrays with a large number of good devices. In addition, one can get the chance to compare his existing ideas and views of fabricating this array used in designing the mask with the reality which will help in making some further improvements afterwards.

In this chapter, all the processing steps done in the cleanroom for fabricating the VCSEL array are outlined with the practical figures and schematics. This will be quite helpful for the readers to understand all the practical steps starting from the formation of the mesa till the metallization of p-contact over the full row. Besides, the problems and the difficulties in fabricating the devices and the solutions of those are also highly illustrated in this chapter.

5.2 Mesa Formation

In fabricating the 2-D MA VCSEL array, the first task is to form the mesa for the devices which can be defined by wet chemical etching or dry etching. But both of these etching methods have some advantages and disadvantages. For example, wet chemical etching is cheap, easy to do and almost no damage due to purely chemical nature but this process has very poor anisotropy and poor control in etching. On the other hand, dry etching (e.g. RIE) has very high anisotropy but it creates some damage on the sample and it is expensive as well. Considering these merits and demerits, wet chemical etching was used to define the mesa.

Standard wet chemical etching of III-V semiconductors occurs by oxidizing the semiconductor surface and etching the oxide. Typically this is achieved by submerging the semiconductors in a liquid mixture consisting of an oxidizing agent and a complexing (oxide etching) agent [17]. Obviously the basic process consists of using hydrogen peroxide H_2O_2 as the oxidizing agent to form GaAs-oxide compounds at the GaAs surface (oxidation step), that are then removed using an acid (H_2SO_4).

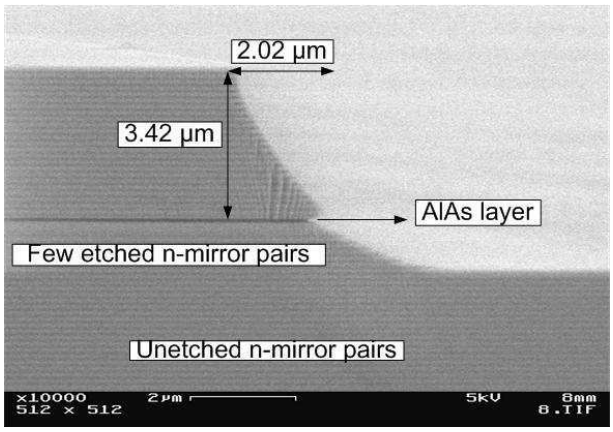


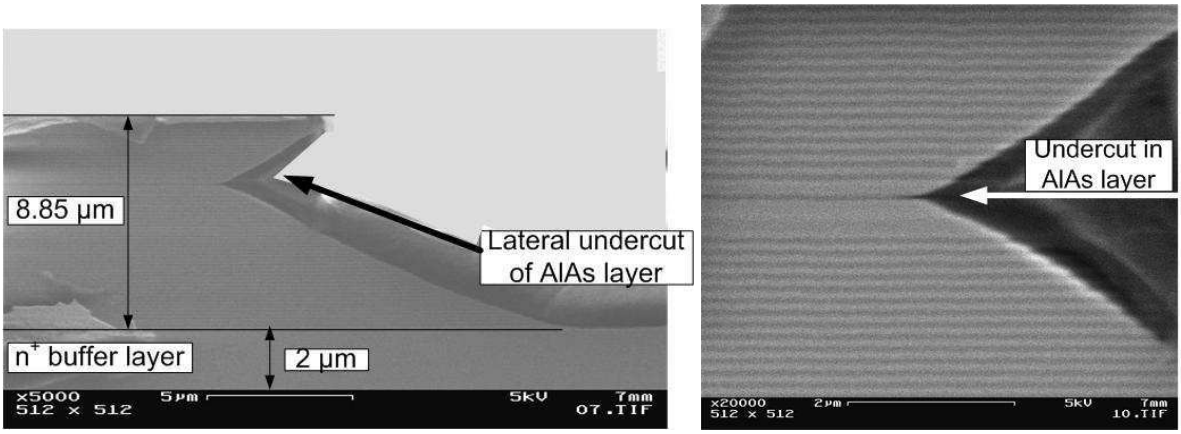
Figure 5.1: *SEM photograph (10,000x) of the cross sectional profile of mesa which shows that the etching was performed just till AlAs layer for oxidation, though few n-mirror pairs underneath AlAs layer were also etched.*

Fig. 5.1 shows the typical cross sectional profile of mesa where the perpendicular etch depth is 3.42 µm (from the top p^+ layer to AlAs layer) and the lateral undercut due to isotropic nature is 2.02 µm which one was assumed earlier. The etching was done in acidic solution ($H_2SO_4 : H_2O_2 : H_2O$) for 3 minutes to reach little bit down to AlAs layer which is sufficient for oxidation taking the etching rate 1.2 µm/minute into account.

But as mentioned earlier, the etching should be continued till n^+ buffer layer in this work which is located under n-mirror pairs. It means that all the p-mirror pairs, AlAs layer, active region, all n-mirror pairs should be etched to reach in n-doped buffer layer. A question comes, then how the cross-sectional profile looks like. Will it be just like the typical case, illustrated in Fig. 5.1 but just extending more down or different?

To get the answer the same acidic solution was used for etching but the duration of etching was too long, 7 minutes instead of 3 minutes. Again the cross-sectional profile of the mesas was examined in SEM machine but this time the profile was little bit interesting and obscure.

From Fig. 5.2 we see that there is a huge lateral undercut in AlAs layer which completely changes the shape of the cross-sectional profile of mesa structure. Then it becomes clear



(a) *SEM photograph (5000x) of the cross sectional profile of mesa* (b) *SEM photograph (20,000x) of the cross which shows that the etching was performed till last n-mirror sectional profile of mesa close to the AlAs layer pairs for oxidation.*

Figure 5.2: *Cross-sectional profile of etched mesa.*

that this is the typical mesa profile in the acidic etchant which was done at the room temperature and for long time, 7 minutes. The reason of this event is that the lateral etching rate of AlAs layer is much faster than the other layers which causes the lateral undercutting of the layers close to AlAs layer [18]. For a short time etching (until the AlAs layer is approached by the etchant) the etchant used at the room temperature behaves like a diffusion one, and a diffusion profile is created which is shown in Fig. 5.1.

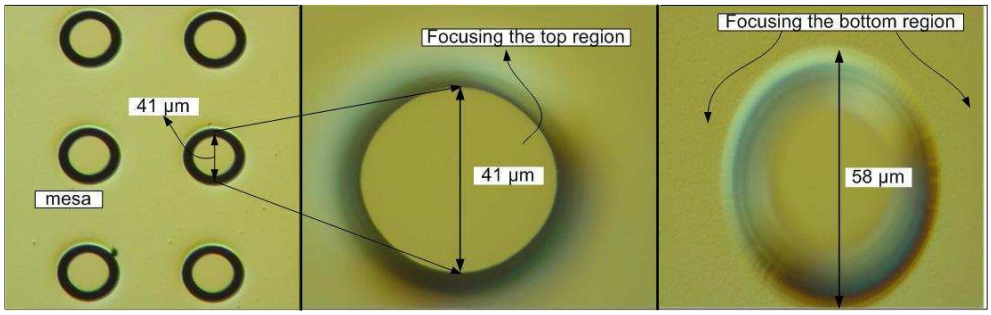


Figure 5.3: *Optical microscope image (20x) of the top view of the mesa having smallest diameter after wet chemical etching (the leftmost). Image (100x) where mesa top has been focused(the middle one). Image (100x) where mesa bottom has been focused (the rightmost).*

It should be stressed that during mesa formation by wet chemical etching, in order to expose AlAs layer, there is a symptom can be found by looking at the sample well which is extremely helpful for knowing the location of the epitaxial layers. The symptoms gets well-pronounced after about 2 minutes 40 seconds (3.16 µm down from the top) when the sample will be completely becoming black for a long time from the bright condition then

it can be realized that AlAs layer is reached. After a while the sample will start to be full of bright-dark regions again since the etching is still ongoing and then after almost 6 minutes 45 seconds there is one very interesting symptom was found which can be used as a indicating factor for stopping the etching. In particular, that bright-dark regions like the stripes of Zebra in the sample is indicating that the n-mirror pairs are being etched and that stripes will disappear after about 6 minutes 45 seconds from which it was realized that 2 μm thick n-doped buffer layer starts from here where the etching should be stopped.

5.3 Selective Lateral Oxidation

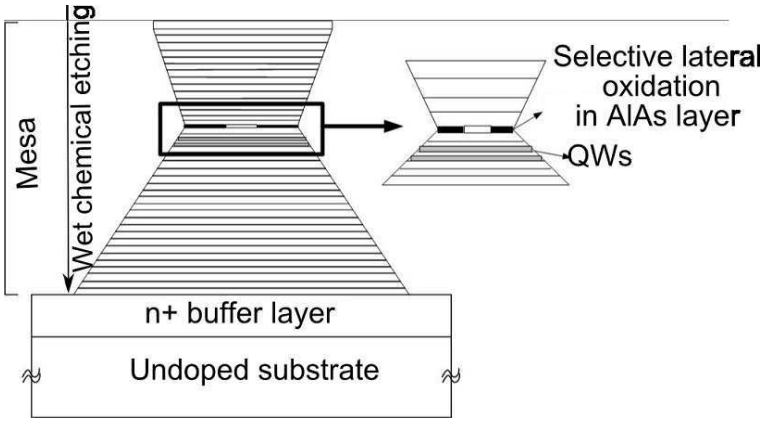


Figure 5.4: *Schematic cross-section view of a selectively oxidized VCSEL after deep mesa etching.*

Then comes to the oxidation. But there are two meaningful words before the oxidation, selective and lateral. What do these mean? Selective means the sample should be oxidized selectively. In details, while oxidizing, the sample should be inserted into the hot three zone furnace where all the epitaxial layers are exposed to the hot furnace to be oxidized. But only that layer, $Al_xGa_{1-x}As$, where, $x \geq 0.95$ will be oxidized and converted into Al_2O_3. At the same time, the rest of the epi-layers will remain unchanged and unaffected. In the sample used here, x is equal to 1, i.e. AlAs whose thickness is about 30 nm. Here selectivity comes from this point of view. And the word, 'lateral' becomes very clear from Fig. 5.4 where the AlAs layer gets oxidized laterally - has been shown.

The oxidation procedure is very simple. Exposed AlAs layer will react with water vapor transported by inert and carrier N_2 gas into the hot furnace where the temperature will be around 380^0 C and that AlAs layer will get converted into Al_2O_3. Note that, the water vapor mentioned earlier is supplied to the hot furnace by bubbling N_2 through deionized water. Moreover, while going to the hot furnace, the water vapor passes through a heated tube to avoid condensation. Note that the resist should be well-stripped from the sample before the oxidation, otherwise that resist will be very hard and sticky to the sample surface which is very difficult to remove will act as insulating layer.

5.3.1 Oxidation Rate Dependencies

The following factors control the oxidation rate [19] :

- Inert carrier gas, N_2 flow
- Al composition
- The layer thickness
- Bubbler temperature
- Furnace tube temperature

5.3.2 Electrical and Optical Confinement

The oxidized region exhibits excellent current-blocking properties and confines the current to the non-oxidized region. Additionally, the native oxide exhibits a much lower index of refraction than the original upper confining layer (n=3.3). Thus, the index step (3.3 to 1.5), through the the thickness of the AlAs layer, forms an optical waveguide in the lateral direction [19].

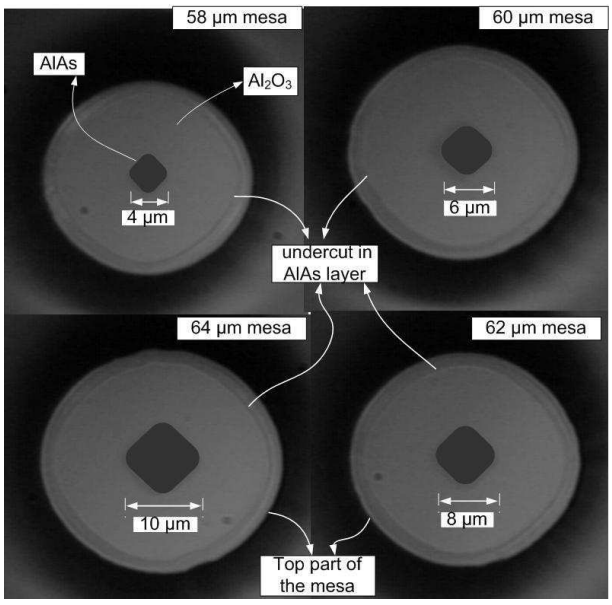


Figure 5.5: *Illustration of the top view of the lateral oxidation in AlAs layer of four different mesas which can be viewed by infrared camera (40x). Here, the dark and bright region indicate the non-oxidized and oxidized area respectively. The undercut in AlAs layer due to the wet chemical etching can be observed as well.*

The parameters used in the oxidation process are as follows:
Temperature of the furnace in three-zones, $T_{furnace} = 382^0C \parallel 382^0C \parallel 382^0C$

Bubbler water temperature, $T_{bubbler} = 96^0C$
Amount of N_2 flow = 0.5 litre/min
Sample temperature, $T_{sample} = 380^0C$
Pressure of water vapor, P = 1012 mbar
After using the above process parameters and checking the oxidation rate by a dummy sample, the oxidation is done. Fig. 5.5 shows the top view of four different sized mesas where we can see the rhombus shaped oxide apertures after oxidation process. Thus approximately the desired active diameters of the devices are found. The operating procedures of the oxidation machine along with the necessary explanations are discussed in details in appendix E.

5.4 Column Isolation

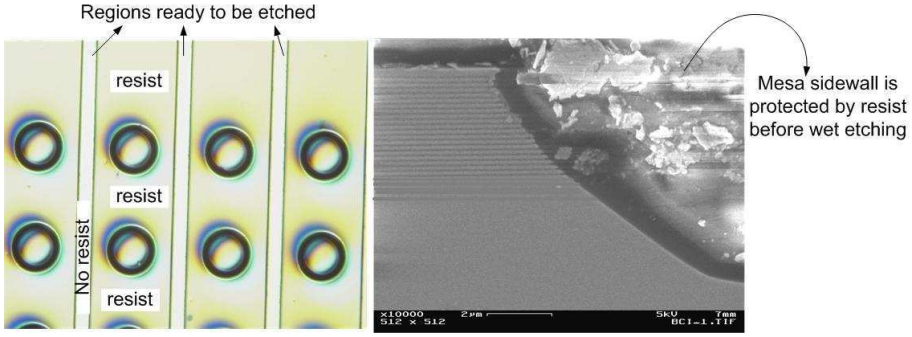


Figure 5.6: *Optical microscope image (10x) of the top view of resist patterning after development prior to etching for column isolation (the left). SEM photograph (10,000x) of the mesa sidewall which is protected by resist so that etching solution does not affect the sidewall at all during the etching (the right).*

After the lateral oxidation process, photoresist was patterned in the wafer for wet chemical etching. Basically in this step, the columns of width 20 μm should be etched 2-3 μm down till undoped substrate by removing the n-doped buffer layer in order to electrically isolate the columns from each other. In addition, the top and bottom regions of few micrometers in width should be etched as well for perfect column isolation. Otherwise, the current flow through the devices can not be controlled properly. Considering this, one can say that this is the most crucial step in matrix addressing array processing.

TI35ES or TI35E photoresist can be used as etch mask which is protective against the harsh condition like wet etching. But due to the problem mentioned in Sect. 5.5, these resists should be avoided. Finally the resist, AZnLOF 2070 resist is used in this etching which is also stable against wet etching. This time, one should make sure that the whole wafer, e.g. the mesa, the mesa sidewall and all the regions except the region of width 20 μm which need to be etched, should be protected by resist so that etching solution can not

affect at these structures as indicated in Fig. 5.6.

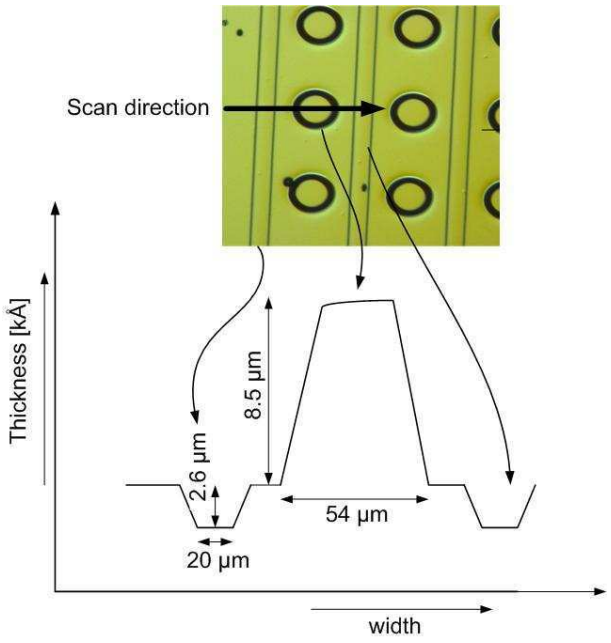


Figure 5.7: *Etch depth measurement by the Alpha-Step surface profilometer after two etching processes.*

Then the same acidic solution like mesa etching is used in etching for column isolation. But the etching rate is much slower at this time compared with mesa etching due to absence of Al-content in the layer, i.e. pure GaAs. Usually the sample is soaked in acidic solution for 3 minutes 30 seconds and the etch depth is found around 2.6-3.0 µm by measuring in alpha step and optical microscope. On the basis of the processing result, it can be said that the etch rate of GaAs is 0.78 µm/min which is accurate and reproducible. Noteworthy that all the etching experiments were performed in this work at room temperature.

Fig. 5.7 shows the measurement result which is obtained by scanning through the sample structure in the profilometer, alpha-step. As an alternative, the etch depth can be measured very easily just by changing the focusing knob of the optical microscope as indicated in Fig. 5.8. It is often convenient that the etching depth should be greater than 2 µm which ensures the arrival in insulating substrate which is very much necessary for matrix addressing operation.

It should finally be noted that before starting the wet etching process, the resist (AZnLOF 2070) patterning after development should be checked very well to make sure there is no residual resist in the etched region which creates a severe problem. May be in this case, O_2 plasma is a solution which can remove this residual resist. Otherwise, after etching it may be found that there are some regions where there is desired 2-3µm etching and there

are some regions without any etching at all. In fact, AZnLOF 2070 resist becomes very stable on the wafer after heat treatment processes. So, well-development and O_2 plasma both are always recommended before the etching process.

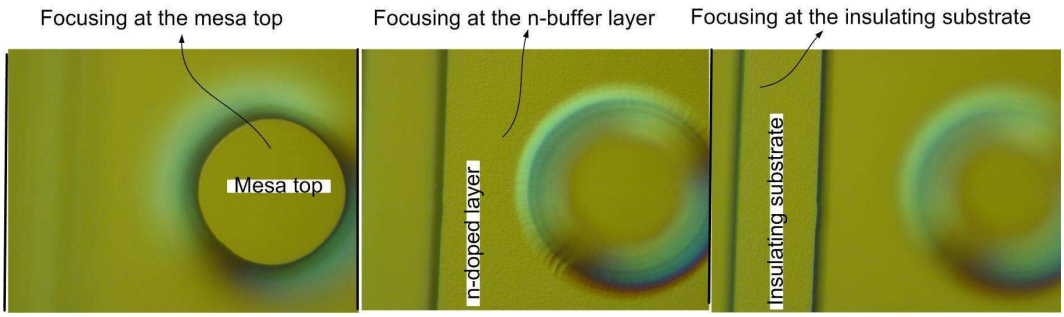


Figure 5.8: *Etch depth measurement by the optical microscope after two etching processes.*

5.4.1 Electrochemical Reaction

GaAs etching rate and shape in a given etching solution can be altered by the presence of a metal substance on the GaAs surface due to the so-called electrochemical effect which is the result of the electric circuit formed between the semiconductor, acting as an anode, and the metal as a cathode [20]. This type of reaction takes place when exposed metals appear in the vicinity of the GaAs area to be etched by the etchant [21]. Due to the different surface potentials, semiconductor and exposed metal behave like anode and cathode in the etchant, respectively, thus forming an electrochemical circuit, thus effecting the etching rate of GaAs by increasing the rate of surface oxidation [22]. It has a pronounced impact on the electrical performance of the device, so one should change the processing steps order so that wet processes are performed before metallization is applied [20].

In this work, it is true that the metal surface can be completely covered by photoresist before the etching process in order to avoid this problem. But it is very possible to finish the two etching processes successively ahead of metallization. Besides, there is also a possibility of exposing the metal surface at the edge of the structures which can cause these problems and at the edge of the wafer, of course, this will take place due to less control in processing over there. Considering all these facts, the n-contact metallization steps should be done later, i.e. after column isolation etching step which will not create any problem in the subsequent processing at all.

In addition to the above-mentioned obvious and serious effect, the metal deterioration problem was also found in the processing if the column isolation etching is carried out after n-contact metallization step which is indicated in Fig. 5.9. But the proper reason of this event can not be figured out due to the lack of time.

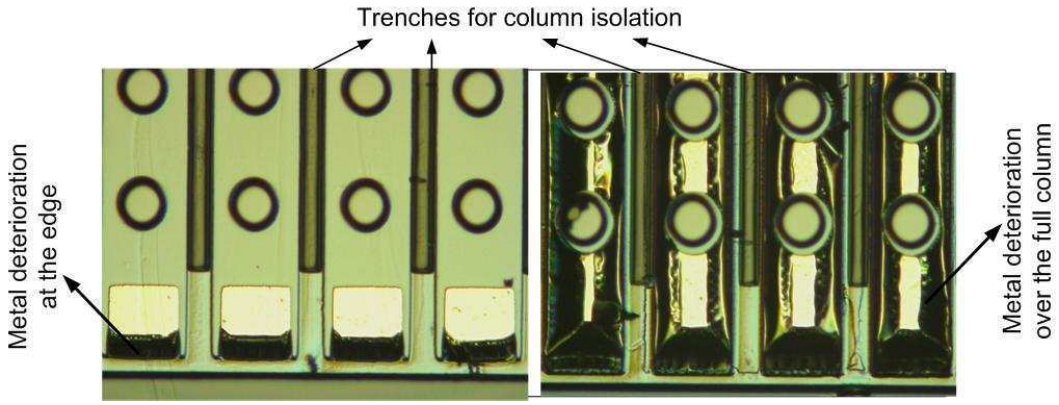


Figure 5.9: *Illustration showing the metal deterioration probably caused by the etchant, the metallization is done earlier than the etching for column isolation here.*

5.5 N-Contact

After column isolation step, the sample has to be ready for n-contact metal evaporation. Since it is selective metallization, one photolithographic step is necessary before loading the sample into the metal evaporation chamber. Fig. 5.10 shows the perfect conditions necessary for selective n-contact metallization. Here we see the resist patterning after n-contact photolithographic step, in specifically, after development, otherwise the desired metallization can never be possible.

At first, TI35ES, image reversal photoresist, very thin or low viscous but has the ability of giving very good resolution, was tested for this purpose. Can TI35ES resist fulfill this condition? After metal evaporation and then lift-off process, the sample is checked in optical microscope to make sure about the desired metallization. Unfortunately the lift-off process does not work well in this way. The main problem is observed at the top of the mesa from where the metal can not be lifted-off. In fact, there should not be any metal since it is supposed to be covered by resist. After investigating the reason it is found that TI35ES photoresist is so thin (low viscosity) that it does not have the ability to cover the deep mesa after development even if very low spinning speed is used in the spin coating machine. Or in other words, after spin coating and then development if the resist patterning is checked very carefully in the microscope then it will be clear that there is no resist at the top of the mesa or some resist at the middle of the mesa but no resist is at the edge of the top mesa which is sufficient for unsuccessful lift-off process. It is very known that resist should be exposed to MP (1-Methyl-2- Pyrrolidon) for lift-off process. If metal covers the top mesa fully then MP can not attack the resist which prevents to lift-off the metal.

In order to solve the problem the thicker negative resist which has the ability of covering the deep mesa after development was used. AZnLOF 2070 is such type of resist which

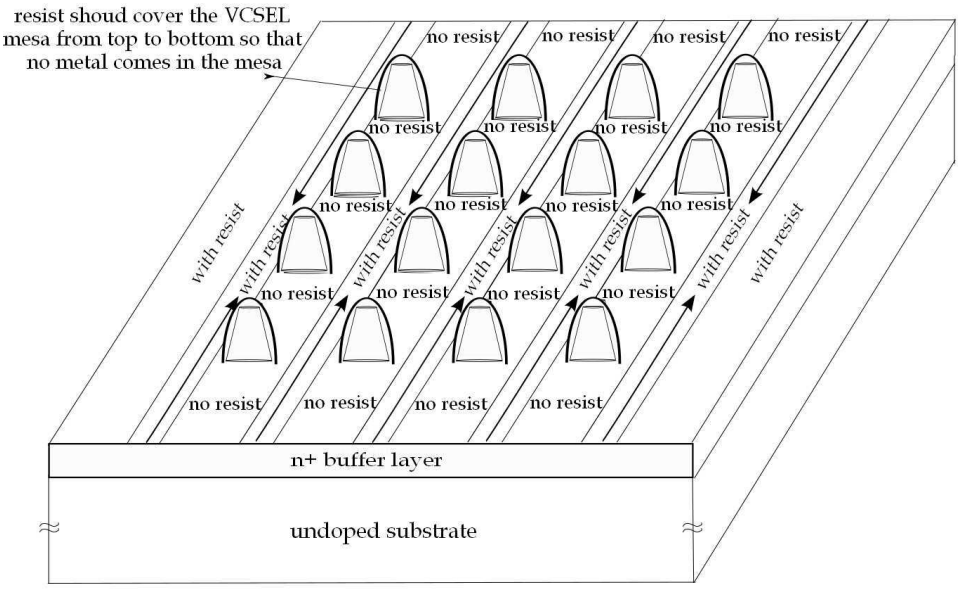


Figure 5.10: *Schematic view of 4x4MAarrays after n-contact photolithographic step, in particular, after development. Two different regions, named 'with resist' and 'no resist' indicate 'no metal' and 'with metal' respectively after lift-off process. In addition, mesas of height 8.5-9 μm are completely protected by the resist so that no metal can remain here.*

has a high viscosity and can give the thickness of 10-12 μm after development depending on the spin speed, but at the expense of the resolution.

Thus by using this resist, metal is evaporated and then lift-off is performed without any problem, or in other words, the desired regions gets metallized. Note that, AZnLOF 2070 has also the ability of withstanding higher temperature in metal evaporation chamber. In most practical cases, before loading the wafer into the evaporation chamber, the sample is soaked in HCl solution (HCl : H_2O = 1:1) for 30 seconds in order to remove the native oxides formed on the sample.

Concerning the n-contact metal evaporation, the materials used Ge(17nm)Au(50nm)-Ni(10nm)-Au(50nm) which are very important for good ohmic contact on the surface of GaAs surface. This contact is also known as alloyed contact which implies that heat treatment process so-called annealing is needed to ensure a good ohmic contact. Actually, GeAu-Ni-Au to n-type GaAs is very complicated ohmic contact process which gets alloyed into the GaAs at temperatures in excess of 400^0C to provide the necessary low contact resistance.

However, the selection of a metallization system that creates a surface region with a high carrier concentration promoting a tunneling mechanism. It is known that by providing a

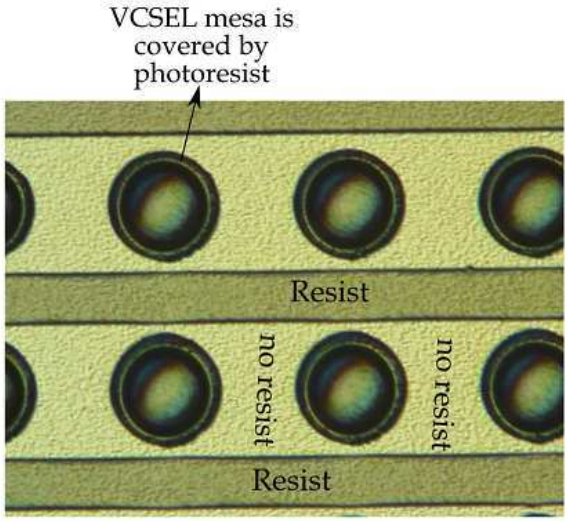


Figure 5.11: *Optical microscope imgae (20x) of the top view of the resist patterning after development in n-contact metallization photolithographic step.*

barrier layer and making it very narrow width by high doping concentration it is possible to achieve an ohmic type contact based on the tunneling mechanism. In such metallization system, Ge, the first material, acts as a dopant element, Au acts as a base metal, Ni acts as a diffusion barrier [23]. Since Ge is a donor, this forms a heavily doped n-type region that promotes tunneling mechanism which leads to an ohmic behavior.

5.6 P-Contact Ring

This is an optional step in matrix addressable array processing. Undoubtedly, p-contact ring enhances the device performance, especially good contact point of view, this step is very important. But skipping this step, one can also test the arrays which saves a lot of time and increases the yield of the chip. Since each photolithographic step reduces the probability of getting the number of good devices. Once all the mandatory processing steps are optimized and the array works well with reproducibility then this optional step can be applied for more improvement.

For a good ohmic p-contact on the surface of GaAs surface, Ti(20nm)-Pt(50nm)-Au(150nm) these three metal layers are used. In fact, this is non-alloyed contact for which annealing is not needed. Evidently these metal layers just sit on the GaAs surface and make the ohmic contact.

A question will arise, why do we need to use these three metals to get an ohmic contact instead of using a good conductive metal (e.g. Au)? Well, among these three metals, Au of course, the base metals for good electrical conduction since it has much higher

conductance and its place in the table of conductance is the third. But the other metals are also needed for good ohmic contact. At first a thin Ti layer was used because it has good adhesion properties with the GaAs surface. Then the interesting metal layer, Pt was deposited as a barrier layer in order to prevent the diffusion from Au into GaAs semiconductor. What would happen if there would be no Pt at all? The answer is obvious, the resulting contact would be converted into Schottky contact since metal carriers and semiconductors carriers will be allowed to diffuse each other then which ultimately lead a rectifying contact - undesired. It is worthy to mention that Au has a high diffusion factor into GaAs and the rate of Au diffusion into the GaAs is a function of the temperature and the material concentration gradient [24]. So, Pt is very necessary. At the end, thick Au layer, base metal, was deposited on top of Pt layer.

It is found experimentally that the arrays work well without any ring contact at the top of the devices. However, the step of the p-contact ring should come after planarization by polyimide. Because keeping the surface unplanarized if the ring contact process is started then there is high probability of unsuccessful lift-off process as mentioned in Sect. 5.5. It is also true that the thick resist (e.g. AZnLOF 2070) can be a solution of this problem but the problem comes when one thinks about the resolution as the ring contact dimensions are not so big.

5.7 Polyimide Step

Polyimide has mainly two purposes in device processing, one is planarization and the other one is electrical isolation between two parts so-called passivation. Thanks to polyimide, both purposes are fulfilled by the polyimide step at the same time. Experimentally, this is the most difficult step in the processing because one has to make sure the planarization of the surface of 8-9 μm and keeping the desired profile at the top of the device in order to facilitate the p-metallization simultaneously. Moreover, without successful polyimide step one can not think of the good devices because this step highly influences the subsequent steps.

There are three types of polyimide which can be used in the device processing, Durimide 7505, durimide 7510 and durimide 7520 are the three options to be used which are orderly arranged according to the thickness. These polyimides have the ability of planarizing in the range 2-40 μm. Apparently it seems that there should be no problem to planarize the surface of 8-9 μm. Where does the problem come from then? The following discussion will help the readers to know the answer.

To optimize the polyimide step for matrix addressable array, different approaches are adopted from the beginning. In fact, four different approaches (three of them are unsuccessful) were used in the processing which will be discussed now.

1) Three steps of polyimide and usage of "POLYIMIDE SAFETY" mask:
At first, the traget is made like this, the planarization will be done in three steps. The 'polyimide-1' which is designed just for filling the trenches will be used initially and then the 'polyimide safety' mask which has a bigger dimension to make very rough planarization and then the rest planarization will be done as the conventional 'polyimide-2' which has the overlap with the top of the devices as discussed in chapter 4. The processing steps are maintained keeping this target at the front. But the processing are not successful due to various reasons. Fig. 5.12 highlights these reasons. The polyimide planarization will

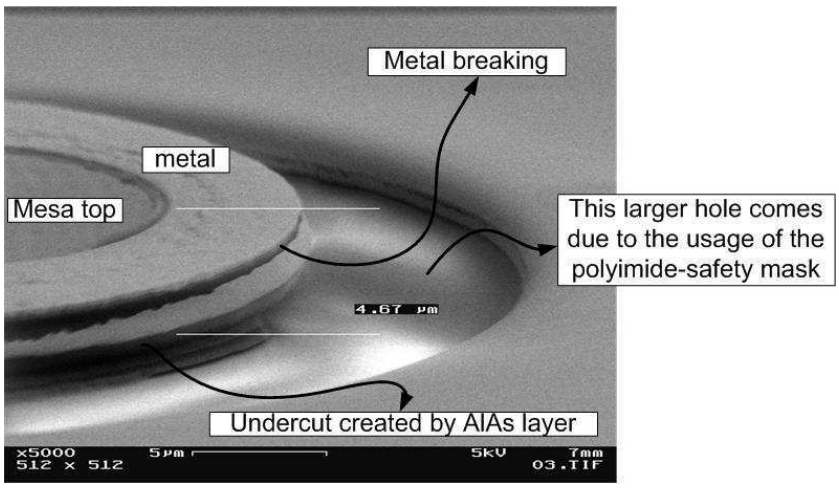


Figure 5.12: *SEM photograph (5000x) of the lateral view of the mesa top and mesa-close regions where after three steps planarization by the polyimide, p-metallization is done over the full row.*

be successful or unsuccessful that can be justified after metal evaporation for p-contact. If the p-contact metallization over the full row maintains its continuity or does not break in any region then we can say that polyimide planarization is flawless and perfect. Fig. 5.12 shows the catastrophic result which is obtained after p-metallization where the metal breaking problem at the top of the device is shown due to very steep sidewall. The obstacle to planarize the surface due to huge undercut created by AlAs layer and the effect of the usage of polyimide-safety mask are demonstrated in this figure. So a question arises what is the reason of metal breaking?

Fig. 5.13 shows the reason schematically from where it is evident that the thin metal layer of approximately 200 nm does not have the ability of tolerating the rough surface like steep sidewall. So there is a high probability of breaking the metals until the surface becomes smooth. From the first processing the information we obtained that is the mask 'polyimide-safety' is not good to use since it creates a huge hole close to mesa top which is a hindrance of planarization and smooth continuous metallization till the mesa top of the device. In addition to this obvious effect, another effect which is noticed here, that is the huge undercut created at the AlAs layer also consumes a lot of polyimide which

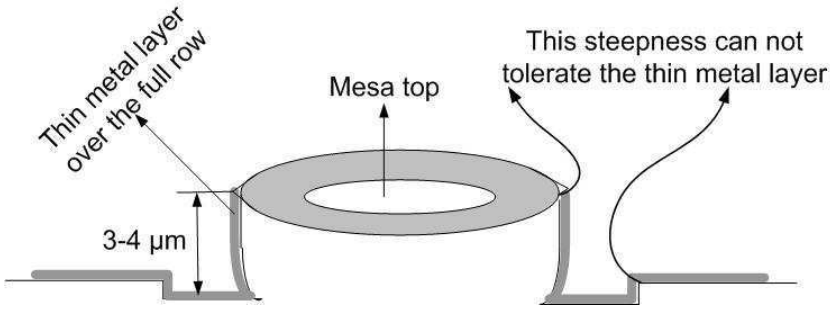


Figure 5.13: *Schematic of the metal breaking problem due to the extreme rough surface.*

also creates some problem in getting the plain surface. In order to solve the problem it is needed to diffuse some polyimide in the undercut which can help in this purpose. Considering further, carrying out the polyimide step three times also very ridiculous because each polyimide step requires a lot of processing time and in each step some devices get damaged due to processing.

2) Two steps of polyimide with lower spinning speed using mesa-top overlapping mask (POLYIMIDE-2) two times and skipping the trench planarizing mask (POLYIMIDE-1): Then the plan is made newly. According to this new plan, the number of polyimide steps

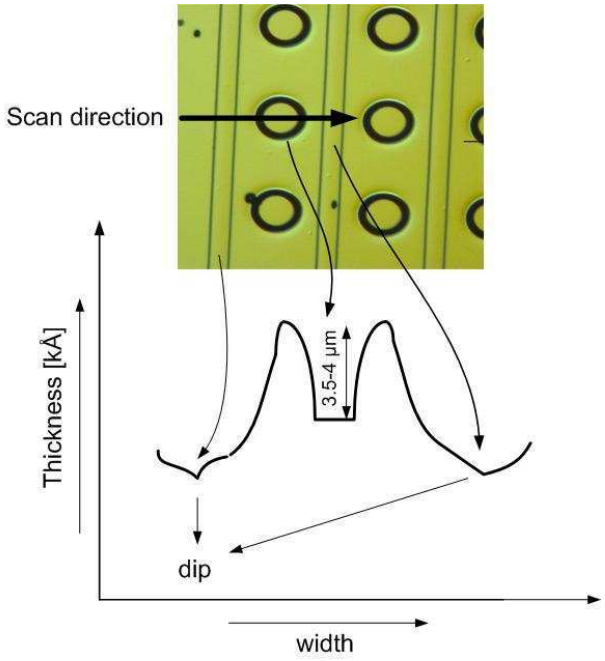


Figure 5.14: *Illustration showing the alpha-step measurement after polyimide planarization by using the mask, "POLYIMIDE-2".*

has to be reduced as much as possible. May be even in single step, polyimide planarization

can be done which certainly reduces time and effort and increases the probability of getting good devices. Finally the plan is concluded like this, the number of polyimide steps will be two and the overlapping mask (polyimide-2) will be used two times successively and no need of using the polyimide-1 which is just to planarize the trenches. Furthermore, it is not so easy to handle the region of huge undercut at the AlAs layer where polyimide needs to be well-diffused for good planarization. Finally, after implementing this plan, the instantaneous problem is found, that is lack of planarization at the trench region where there are some sharp dips are noticed which can be a cause of breaking the metals again. The alpha-step measurement as indicated in Fig. 5.14 can show the evidence of this truth.

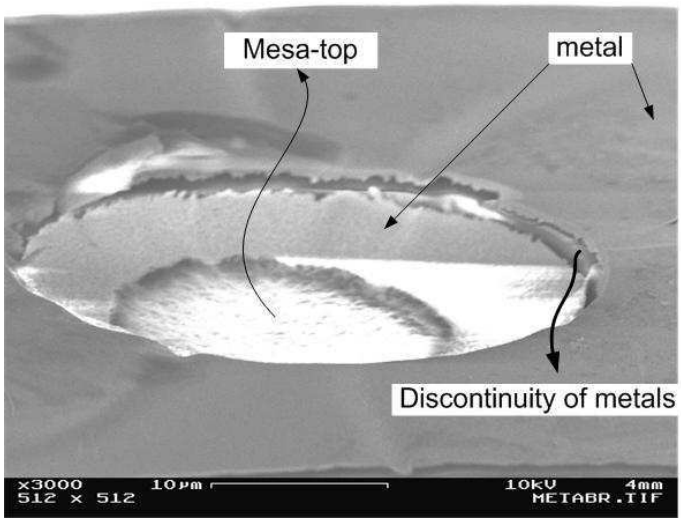


Figure 5.15: *SEM photograph(3000x) of the mesa after planarizing the surface by polyimide in two steps by using the same mask ("POLYIMIDE-2") two times where we can see that metal breaks at the steep sidewall due to the raising profile created by the polyimide at the edge of the mesa.*

The severe problem is found after the p-metallization over the full row. Though it is subject to suspicion that the thin metal layer will be continuous or discontinuous over the trenches specially at the dip (where the column isolation etching is done), finally it is found that the thin metal layer is very smooth and continuous along the dip, there is no problem there at all. The main problem is found at the top of the devices where there is a huge raising profile (3.5-4 µm) created by the polyimide leads to build a steep sidewall as illustrated in Fig. 5.15. This raising profile at the top is enough to break the overlying thin metals. The reason of forming this raising profile at the top is not obscure. It is obvious that when one tries to planarize the surface of 8-9 µm beside the devices, the top of the devices get also affected, i.e. some raising profile is created at the top which is completely undesired.

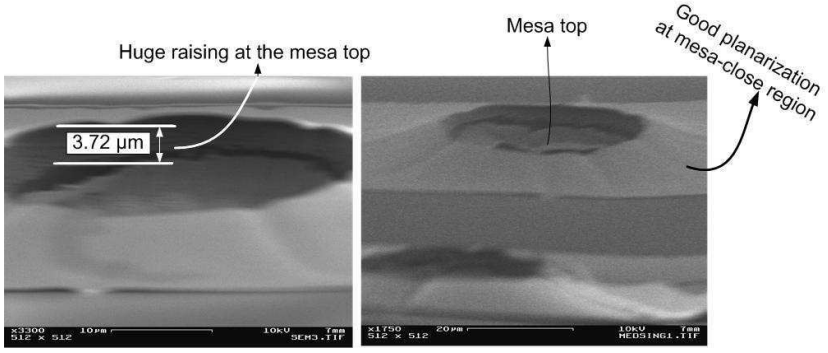


Figure 5.16: *SEM photograph(3300x) of the lateral view of the mesa top after single polyimide step for planarization where huge raising profile created by polyimide is noticed (the left) and SEM photograph(1750x) at the right side shows the mesa-top and mesa-close regions where it is obvious that good planarization comes at the mesa-close regions.*

3) Single step using thicker polyimide with lower spinning speed and mask "POLYIMIDE-2":

It is also tried to planaraize the surface in single step where very thicker polyimide (e.g. Durimide 7510) is used with low spinning speed so that the height of 8-9 µm can be obtained at a time which certainly saves time and effort. But the same problematic result is found again, may be this time the result is more severe because almost all of the devices suffer this metal-discontinuity problem. While flowing the current through the devices by placing the needles in two bondpads it is realized. Fig. 5.16 represents the unplanarized profile close to mesa top which causes to break the metal.

Finally, the huge raising profile at the edge of the devices can be drawn schematically as Fig. 5.17 where we can see the typical result after two step planarization with thinner polyimide or single step planarization with thicker polyimide which creates a major problem in electrical conduction point of view. This problem needs to be overcome as early as possible so that the processing step can be optimized and reproduced with high yield.

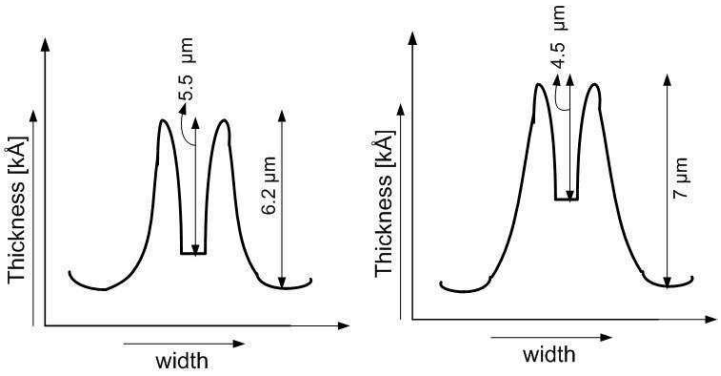


Figure 5.18: *The profile at the top of the device after planarization by thicker polyimide, measured by alpha-step profilometer. Without O_2 plasma after heat treatment(the left), with O_2 plasma for 40 minutes after heat treatment(the right)*

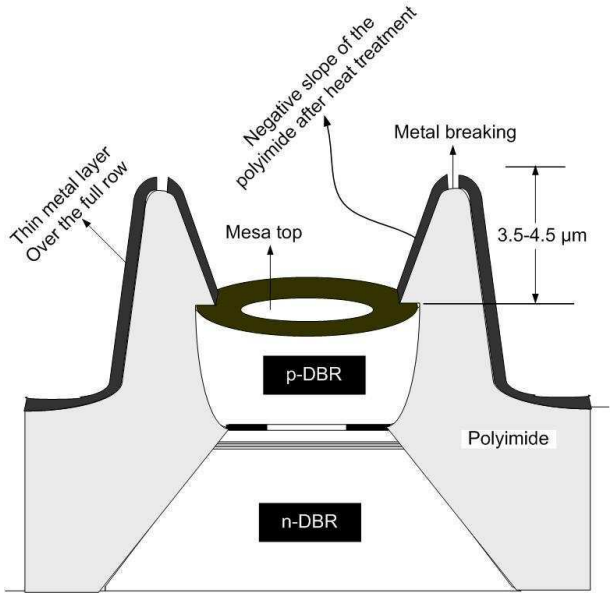


Figure 5.17: *Schematic of the device profile after polyimide planarization and bondpad metallization over the full-row.*

If the raising profile at the top is removed somehow then this problem appears to be solved. O_2 plasma can be a hope here. So, the thicker polyimide with lower speed (e.g. 2000rpm) is spun onto the sample and then the profile is checked in alpha-step profilometer after long heat treatment process in the annealing machine. That unexpected profile is observed again as usual as shown in Fig. 5.18 (at the left). Then the sample is kept in O_2 plasma for 40 minutes to remove this raising profile and then checked again in profilometer, shown in Fig. 5.18 (at the right) from where it can be concluded that etching rate of polyimide after heat treatment is very slow, almost negligible and the top and bottom surface are getting affected at the same rate. Though there is some enhancement at the top but the bottom surface lowering gives the same problem again.

4) Three step of polyimide with higher spinning speed and using mask POLYIMIDE-1 and POLYIMIDE-2:

In order to avoid this unpredictable problem, the polyimide is spun onto the sample with a higher speed (e.g. 4000rpm) this time instead of using lower speed (e.g. 1500 rpm) which was used last time. It is worthy to mention that "Polyimide-1" is used for planarizing the trenches at first and then the same mask "Polyimide-2" is used two times for overall planarization. This time the result obtained is very promising and satisfactory. By optical microscope and alpha-step profilometer measurement, the profile obtained as shown in Fig. 5.19 which can be proceeded with for the next step. There is no huge raising profile at the top of the device, though there is 0.5-1 µm raising but the thin metal layer can tolerate this roughness. It should be noted that in all polyimide planarization steps mentioned in this strategy, Durimide 7505, the thinner one, is used. Moreover, after the last metallization

step the sample was examined in SEM, alpha-step profilometer and optical microscope to check the continuity of the metals, starting from the each edge of the unit cell till the top of the devices. This time no metal breaking problem was found.

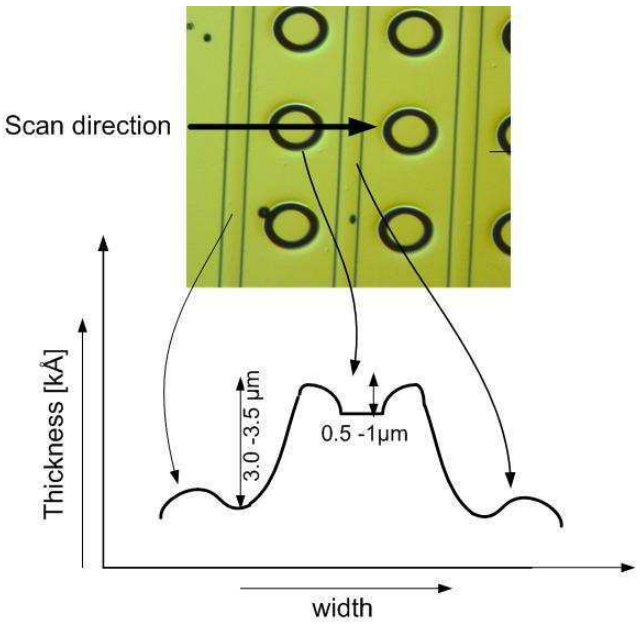


Figure 5.19: *Measurement in the alpha-step profilometer after all polyimide planarization steps. The scanned profile looks very conventional.*

5.8 P-Row Contact

This is one of the most important steps in MA array processing. In fact, this is not the bondpad for individual device, instead, this is the p-contact over the full row which cover all of the devices in a single row keeping some opening at the top from where light can come out. It was mentioned that the metallization of p-contact ring can be skipped in this array processing because this bondpad metallization will cover some top region of the devices which is enough for flowing the electrical current through the devices. Obviously, the p-ring contact ensures a good contact of the devices which is very necessary to enhance the device performance. But it is also true that the devices with matrix addressing can be found only by this metallization step. Fig. 5.20 shows the p-metallization over the full row keeping some opening at the top of the devices in each row.

Concerning the materials used for p-metallization, Ni-Au metal layers are deposited in bondpad metallization on polyimide surface conventionally. The reason behind it Ni has a good adhesion properties and reactivity with polyimide which is used as first metal layer and then Au is used as base metal layer. But if the p-ring contact metallization step is skipped where the different metal layers Ti-Pt-Au were used then which material

for metallization should be chosen now? Should it be p-ring contact material (Ti-Pt-Au) or bondpad material (Ni-Au)? Obviously, there is one dilemma here, if Ti-Pt-Au metal layers are used where Ti, the first material, has a good adhesion properties with GaAs semiconductor which is very good for the top region of the device but not so good for polyimide surface. On the other hand, if we would use Ni-Au metal layers then this would not be so good for GaAs semiconductor surface. Clearly, this bondpad metallization will cover the devices of full row where the metal layers will face the polyimide and GaAs surface. Anyway, considering the merits and demerits, Ti-Pt-Au metal layers are deposited in this step and those metal layers were also robust on top of polyimide as well. No problem was found from electrical conductivity point of view afterwards.

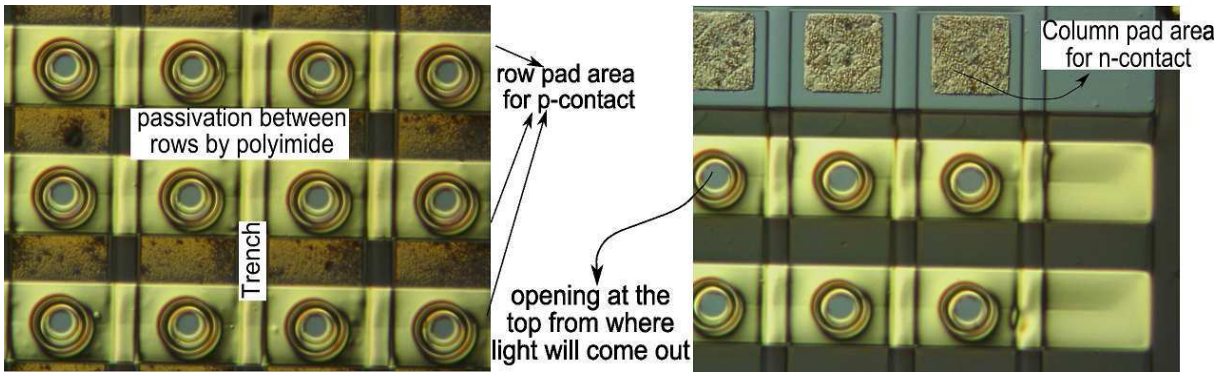


Figure 5.20: *Optical microscope image (10x) after the p-metallization over the full row.*

5.9 Summary

All the processing steps and their results in fabricating MA array are presented with necessary explanations and figures in this chapter. The problems encountered during the processing and the implemented solutions for those problems are also illustrated here. At the end, it can be declared that the processing steps (mentioned in Appendix F) in fabricating the MA array is well-optimized at the end by which one can reproduce this array without any problem.

Chapter 6

Matrix Addressable Array Characterization

6.1 Introduction

The characterization after the fabrication of the 4 x 4 arrays plays an important role in realizing the performance of the devices. In addition, the success rate of the processing, the yield in the chip and so on can be measured only after the characterization. These characterizations include the determination light-current-voltage (LIV) curves of each device from which some other important parameters can be extracted such as the sheet resistance of the array, power conversion efficiency, dissipated power etc. Besides, on the basis of the characterization result one can also tell the quality of the sample epitaxial growth, the uniformity of the wafer, the location of good quality device and so on which are extremely significant information for them who are involved in epi-growing of the sample.

In this chapter, the electro-optical characterization of the array will be outlined at first. The experimental setup used for this characterization will be explained along with the schematic figure. Furthermore, the homogeneity of the array, some device performance-related parameters like the dissipated power, wall-plug efficiency and differential quantum efficiency are also calculated here depending on the above-mentioned electro-optical characterization. In addition, the sheet resistance faced by the devices in the array is also calculated theoretically and then it is compared with the experimental values. Finally, the optical spectra of the devices measured by the spectrum analyzer are also shown in this chapter.

6.2 Electro-optical Characterization

As mentioned, four different sized circular mesa were designed in the mask layout to get four different sized active diameters of the devices. In this work, the 4 x 4 array called as one unit cell consists of 16 devices with same mesa dimension and the pitch

size is 125 µm is in all cases. The LIV characterization was done for four different unit cells distinguished by the type of the unit cell (discussed in subsection 6.2.2) and mesa dimension. Before showing the LIV curves of these devices, the experimental setup used for the electro-optical characterization is described in the next section.

6.2.1 Experimental Setup

For standard LIV characterization the experimental setup used in this work as schematically illustrated in Fig. 6.1. In this setup, at first the sample has to be mounted on the sample stage made by insulating material where vacuum can be applied through a small hole. In fact, this sample stage is motorized which can be controlled by joystick. To put the needle on two different bondpads of the device which needs to be measured, an optical microscope (0.5x, 1x, 1.5x, 2.5x, 5x) was used. The current source supplies current via a probe needle to the VCSEL. It is worthy to mention that two needles must be necessary to characterize the arrays as shown in Fig. 6.2 where spontaneous and stimulated emissions are controlled by the laser driving current. The current source is connected to the PC via parallel port. In this setup, the large movable photodetector was used to measure the optical output power instead of power meter which has to be kept at the centre of that device from where light output will come out. The photodetector is reverse biased by the rechargeable battery mounted on 'biasing unit' which is finally connected to the current source. Thus, PC senses the value of current, voltage and optical output power and plots the real time data.

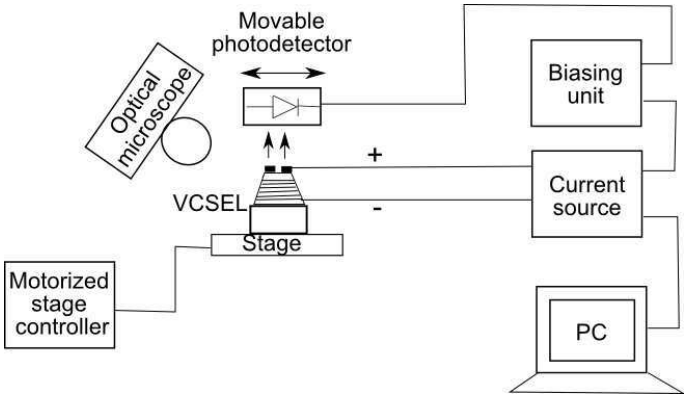


Figure 6.1: *Setup used for the characterization (e.g. LIV curves) of VCSELs.*

6.2.2 Classification of Unit Cell

As mentioned earlier, there are two different types of column pad area for n-contact available in the fabricated wafer which will be called as "TYPE-1" and "TYPE-2" from now as indicated in Fig. 6.3. It is very interesting to characterize both types of unit cells

Figure 6.2: *VCSEL in operation with matrix addressing, placing two needles in n- and p-bondpads. Below threshold current (the left one) so-called spontaneous emission and above threshold (the right one) so-called stimulated emission.*

from where some important comparisons and the deviation of series resistance from one another can be figured out very easily.

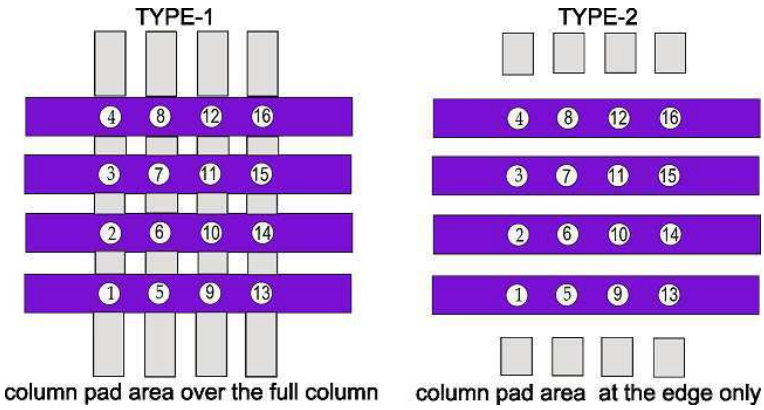


Figure 6.3: *Illustration showing two types of unit cells in the processed wafer. This classification has been made on the basis of the column pad area design for n-contact. The numbering of the VCSELs starting from 1 to 16 will be used later.*

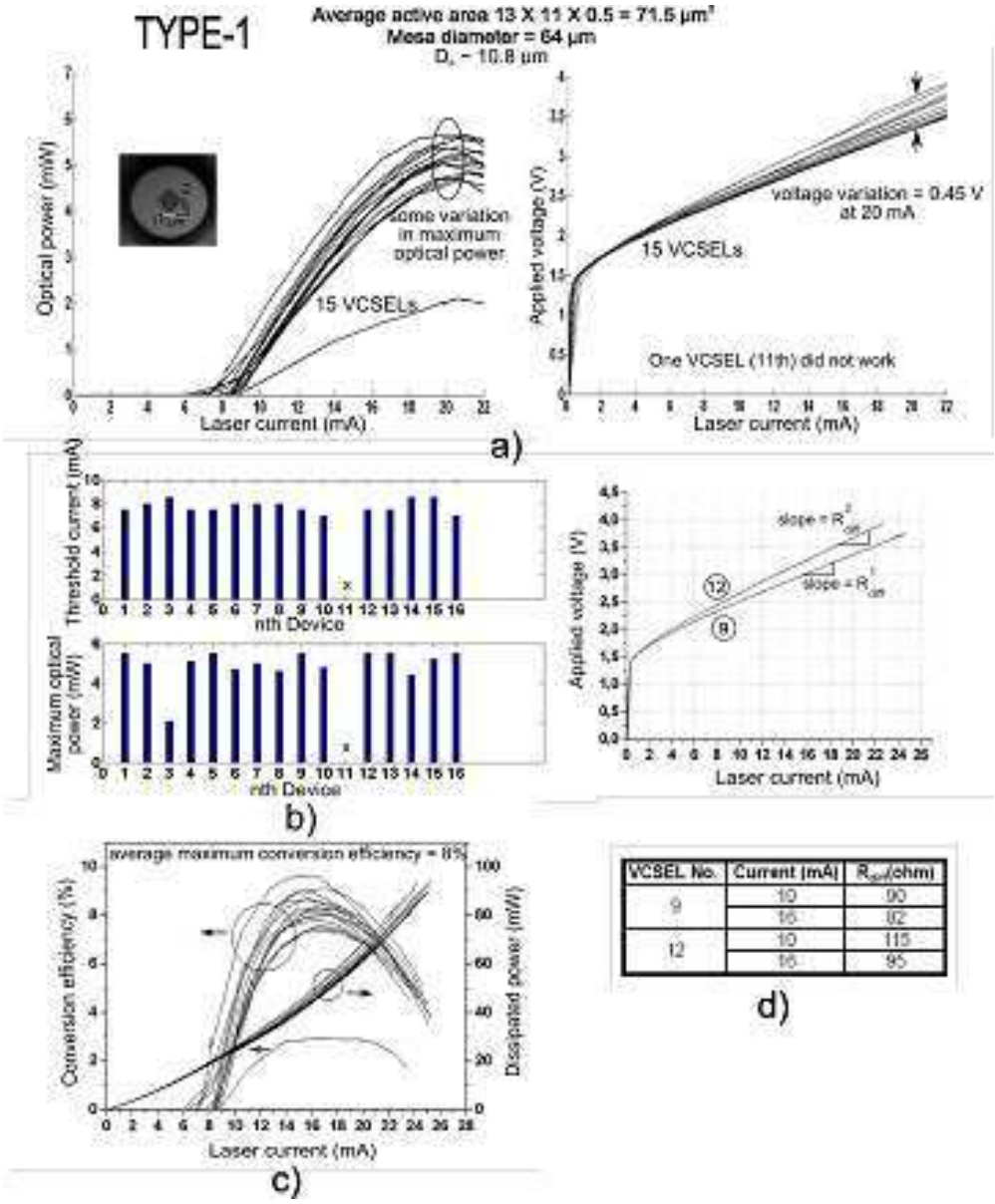


Figure 6.4: *a) Typical light output against laser driving current (LI curves) and operating voltage against current (IV curves) of "TYPE-1" unit cell of mesa diameter 64 μm. b) Bar chart showing maximum optical power and threshold current against laser current. c) Conversion efficiency and dissipated power Vs laser current. d) Measurement of differential series resistance.*

6.3 Important Results Depending on the LIV Characterization

Now four different types of unit cells will be characterized by LIV curves, statistical representation of the array uniformity, differential series resistance, power conversion efficiency

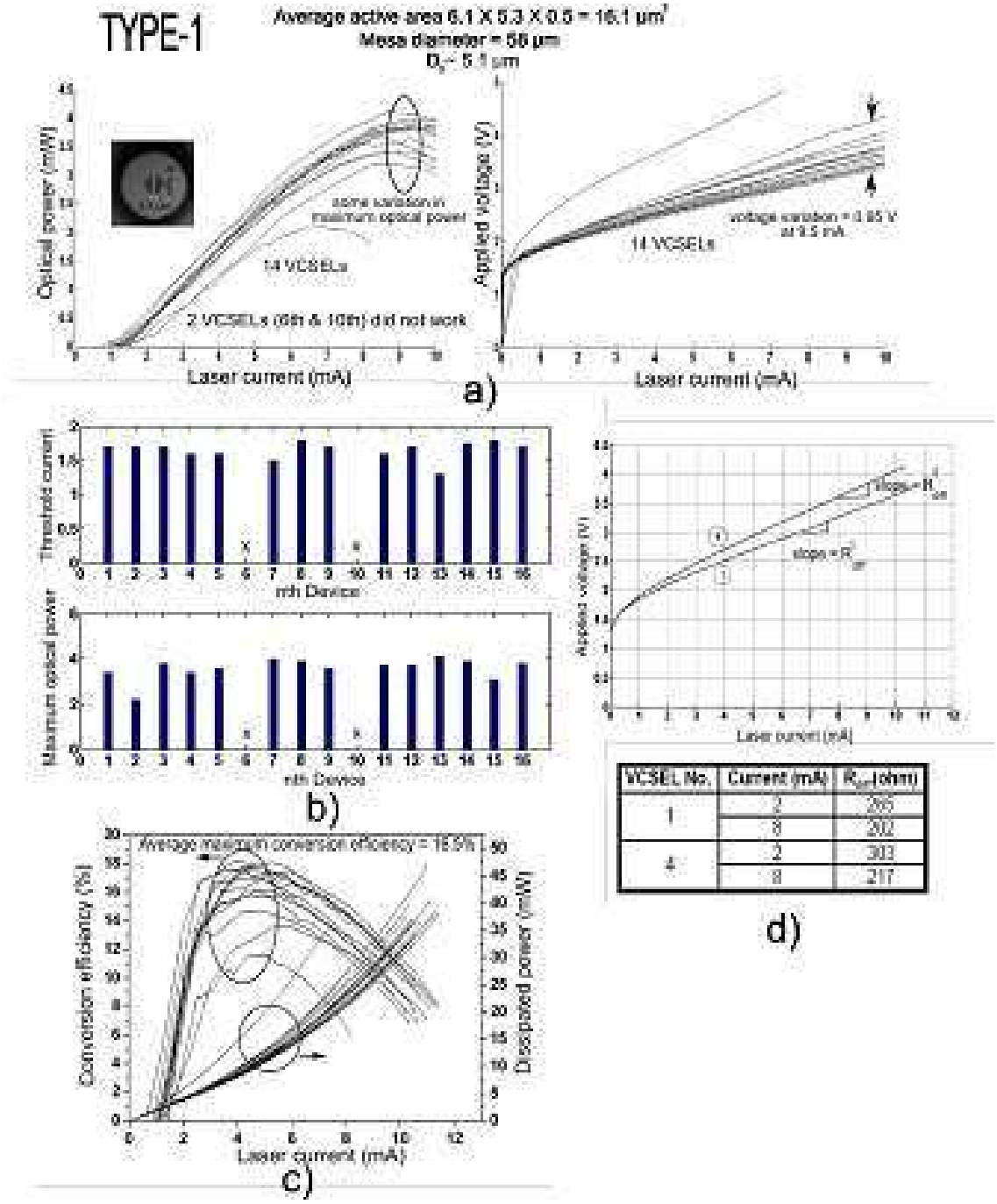
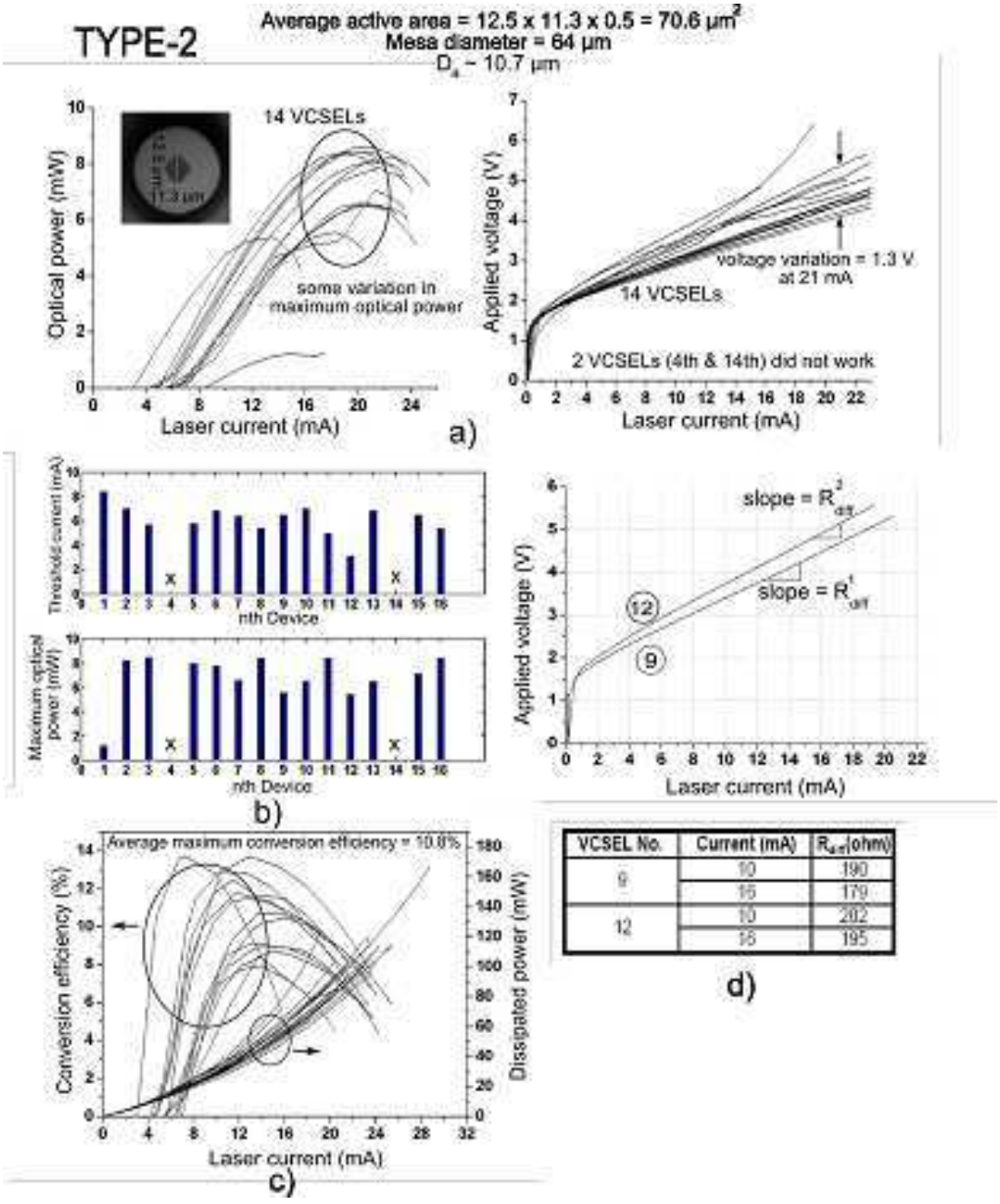


Figure 6.5: *a) Typical light output against laser driving current (LI curves) and operating voltage against current (IV curves) of "TYPE-1" unit cell of mesa diameter 58 μm. b) Bar chart showing maximum optical power and threshold current against laser current. c) Conversion efficiency and dissipated power Vs laser current. d) Measurement of differential series resistance.*

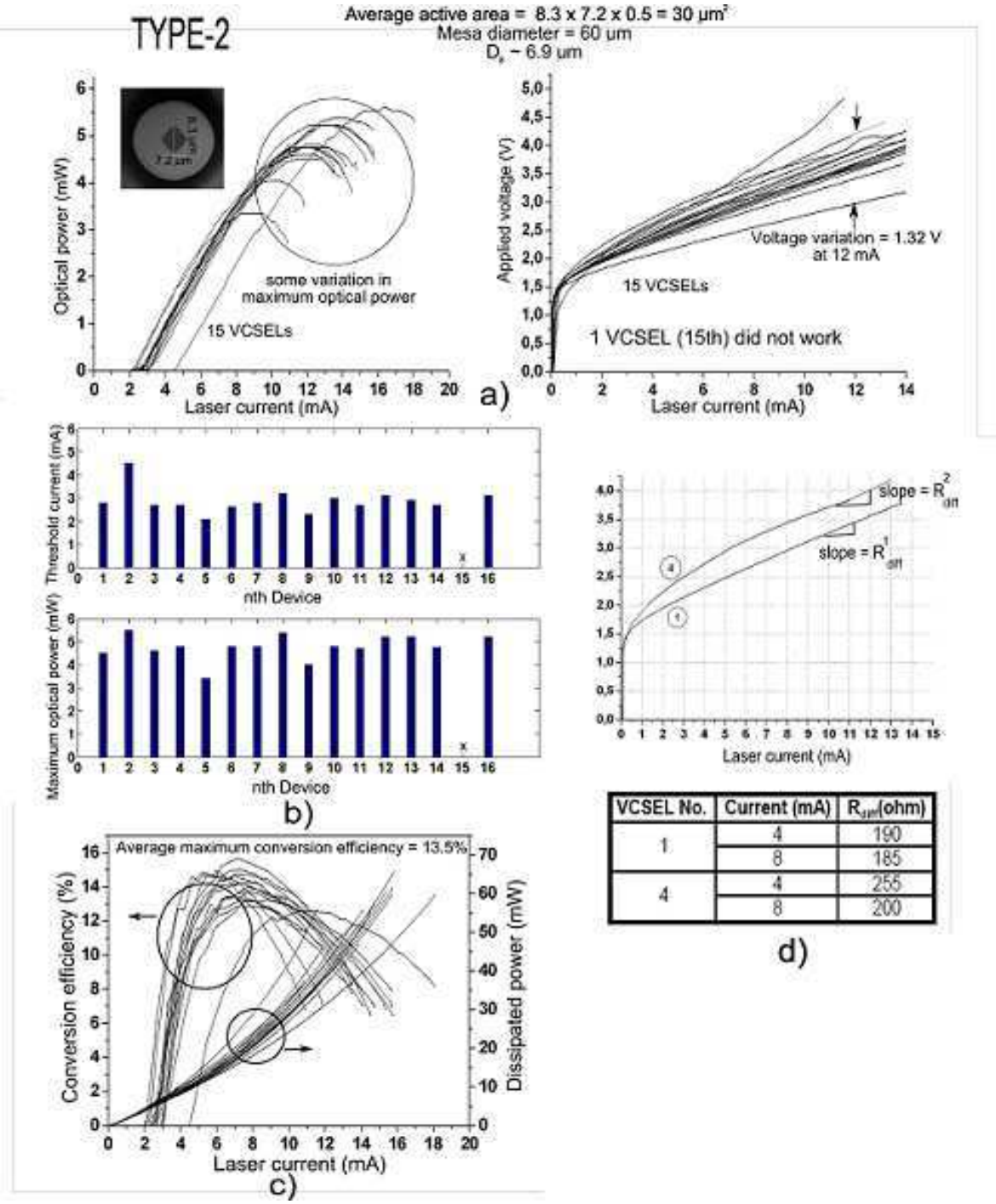
and dissipated power. 1/2 VCSELs in all unit cells did not give the lasing, may be due to metal breaking problem in p-row contact or may be some processing problems. Some of



VCSEL No.	Current (mA)	R_{diff} (ohm)
9	10	190
	15	179
12	10	202
	15	195

Figure 6.6: *a) Typical light output against laser driving current (LI curves) and operating voltage against current (IV curves) of "TYPE-2" unit cell of mesa diameter 64 μm. b) Bar chart showing maximum optical power and threshold current against laser current. c) Conversion efficiency and dissipated power Vs laser current. d) Measurement of differential series resistance.*

the devices show little bit smaller optical power due to some unclear reasons.
Anyway, the important results found depending on the LIV characterization, the com-



VCSEL No.	Current (mA)	R_{dif}(ohm)
1	4	190
	8	185
4	4	255
	8	200

Figure 6.7: *a) Typical light output against laser driving current (LI curves) and operating voltage against current (IV curves) of "TYPE-2" unit cell of mesa diameter 60 μm. b) Bar chart showing maximum optical power and threshold current against laser current. c) Conversion efficiency and dissipated power Vs laser current. d) Measurement of differential series resistance.*

parison between two types of unit cells classified earlier will be shortly described now in terms of the following issues:

1. **Comparison of optical output power among the characterized unit cells:** The optical output power from the VCSELs with larger mesa is higher than the smaller mesa which is quite logical as the optical output power increases with the active area of the device as shown in Fig. 6.4 (a), Fig. 6.5 (a), Fig. 6.6 (a) and Fig. 6.7 (a). Though the optical output power should be independent of the type of unit cell, we see some difference of maximum optical output power between two types of unit cells (Fig. 6.4 and Fig. 6.6) having the same mesa dimension. As an explanation, the positioning of the unit cell can be mentioned since epitaxial growth is not uniform over the full wafer. In fact, those two unit cells are not closely located in the processed wafer, instead they have some distances in between as displayed in Fig. 6.10.

2. **Variation of optical output power and threshold current:** VCSELs with same mesa dimensions should have the same optical power if the oxide apertures or the active areas of the devices remain same. But in reality, there is strong inhomogeneity found in the oxide aperture of the devices due to the inhomogeneity of epitaxial growth even in one unit cell having the same mesa dimension which leads to vary the optical power obtained from the devices. The change of the threshold current is noticed among the devices of a unit cell due to the same reason as illustrated in Fig. 6.4 (a), Fig. 6.5 (a), Fig. 6.6 (a) and Fig. 6.7 (a).

3. **Threshold current in terms of device dimension:** The threshold current of a device depends on the active area of the device. The larger the active area, the higher the threshold current and vice versa which is reflected in the LI curves. Fig. 6.4 (a) - Fig. 6.5 (a) and Fig. 6.6 (a) - Fig. 6.7 (a) show this evidence where the largest and smallest mesa have been characterized side by side.

4. **Combined voltage variation among 16 devices in terms of the type of unit cell:** The voltage variation from one device to another device resulting from the series resistance is also an important parameter in MA array. If the IV characteristics of TYPE-1 (Fig. 6.4 (a)) and TYPE-2 (Fig. 6.6 (a)) is compared where the devices of both type has the same mesa dimension, then much higher voltage variation among the devices is noticed in TYPE-2 which is also logical since TYPE-2 has higher sheet resistance. TYPE-1 shows better performance than TYPE-2 in this case as well.

5. **Uniformity of the array in terms of the threshold current and maximum optical output power:** The uniformity of the array in terms of the threshold current and maximum optical power is not so satisfactory due to the non-uniformity of oxdie

aperture of the device, already mentioned, as indicated by the bar chart of Fig. 6.4 (b), Fig. 6.5 (b), Fig. 6.6 (b) and Fig. 6.7 (b).

6. **Conversion efficiency in terms of the device dimension:** The device with smaller dimension should have the smaller conversion efficiency than the device with bigger dimension because heat gets dissipated from the larger device easily. But in the experimental result the opposite behaviour was found which is illustrated in Fig. 6.4 (c) and Fig. 6.5 (c) due to the wavelength dependence of the gain which varies with the position of the unit cells in the processed wafer. Note that all of the measurements mentioned here are done at room temperature without any heat sink.

7. **Differential series resistance of the devices:** Above threshold current and with small intrinsic losses, the slope of the IV curve gives a resistance value for the device so-called differential series resistance, denoted as R_{diff}. Basically this value tells the rate of increasing voltage drop with increasing current, formulated as $R_{diff} = dV/dI$.

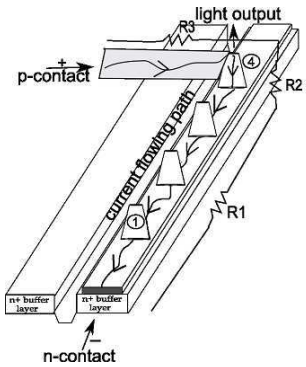


Figure 6.8: *Schematic showing of the factors influencing the differential series resistance of the device.*

For matrix addressable array, there are some additional factors influence this differential resistance. In fact, the voltage drop along the long VCSEL n-contact column or p-contact row can not be ignored at all. Specially when the device 4, 8, 12, 13, 14 15 and 16 needs to be turned on because in these devices either long n-contact or long p-contact line is used in flowing the current through the devices. For example, if one wants to turn on the VCSEL-4 (as shown in Fig.6.8), the differential resistance will not be same like the VCSEL-1, obviously VCSEL-4 will show higher resistance since current needs to travel a longer path in this case. In fact, this resistance depends on the following factors:
R_1 = Sheet resistance due to the metal or semiconductor layer through which current

flows. This is the resistance faced by the electrical current. It is known that sheet resistance will depend on the resistivity of the material and the thickness of the sheet,
R_2 = Intrinsic resistance of the device due to non-perfect grading of heterointerfaces and
R_3 = Metallization resistance and tip resistance of the needle.
The difference of differential resistance between these two VCSELs (1 & 4) was examined by IV curves. It is obvious that the slope of IV curve for VCSEL-4 is higher than VCSEL-1, quite logical. However, the calculated differential resistance of these two far-positioned VCSELs for every type of unit cells are given in a tabulated way in Fig. 6.4 (d), Fig. 6.5 (d), Fig. 6.6 (d) and Fig. 6.7 (d).

8. **Differential series resistance in terms of device active area:** Device active area also plays an important role in influencing the differential series resistance of the device which is presented in Fig. 6.4 (d) and Fig. 6.5 (d). The differential series resistance of the device decreases with increasing the active area of the device which abides by the law of resistivity.

9. **Differential series resistance in terms of the type of unit cell:** R_{diff} is also influenced by the mask design. If the calculated values of R_{diff} in Fig. 6.4 (d) and Fig. 6.6 (d) are compared where two different unit cell can only be distinguished by the n-contact pad formed depending on the mask design, then it will be found that 'TYPE-1' gives less R_{diff} compared with 'TYPE-2', since 'TYPE-1' is continuous Au layer over the full column. From this point of view, one can undoubtedly say that, 'TYPE-1' is better than 'TYPE-2'.

10. **Differential quantum efficiency** : The slope of the output characteristics curve (light output vs current) above I_{th} is the differential quantum efficiency or DQE, indicating the fraction of injected electrons which, converted into photons above laser threshold current.

Unit cell	Differential quantum efficiency, η_d (%)
Mesa = 64 μm, D_a ~ 10.8 μm	46.1
Mesa = 58 μm, D_a ~ 5.1 μm	56.5
Mesa = 64 μm, D_a ~ 10.7 μm	64
Mesa = 60 μm, D_a ~ 6.9 μm	56

Table 6.1: Differential quantum efficiency, η_d above I_{th} of four different unit cells where the numerical result given here is the average of 16 VCSELs

6.3.1 Oxide Aperture Shape

The inset pictures of Fig. 6.4 (a), Fig. 6.5 (a), Fig. 6.6 (a) and Fig. 6.7 (a) shows the real shape of oxide apertures in the processed wafer, which is rhombic shaped.[5] The numerical values of the oxide apertures shown in these figures are averaged over 16 devices.

6.3.2 Calculation of D_a

The value of equivalent effective oxide aperture shown in Fig. 6.4 (a), Fig. 6.5 (a), Fig. 6.6 (a) and Fig. 6.7 (a) which is denoted as D_a can be calculated by using the following equation:

$$D_a = \frac{\frac{a+b}{2} + c}{2} \tag{6.1}$$

where, a, b = The length of the two diagonals of rhombic shaped oxide aperture
and $c = \sqrt{\frac{2ab}{\pi}}$ [assuming, $\frac{ab}{2} = \frac{\pi c^2}{4}$]
For example in Fig. 6.4, a = 13 μm, b = 11 μm (measured)
and c = 9.54 μm (calculated)
After entering these values in Eqn.(6.1), the value calculated for D_a is 10.8 μm.

6.4 Calculation of Sheet Resistance

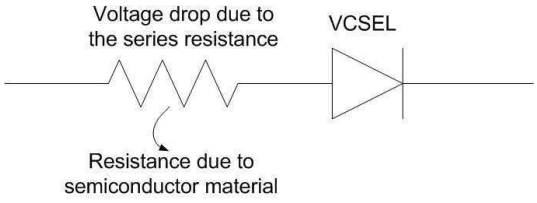


Figure 6.9: *Illustration showing the sheet resistance by a simple equivalent circuit in the array.*

Sheet resistance is that resistance which will be taken into account when the current flowing path will be through the semiconductor layer, specifically, n-doped buffer layer which is applicable for TYPE-2 design. In this design, the current needs to flow a longer path made by semiconductor layer to turn on the VCSEL-4 compared with VCSEL-1.
The conductivity (σ) of the n^+ doped layer is given by,

$$\sigma = qn\mu_n \tag{6.2}$$

where, q = The charge of the electron (A-s),
n = Electron doping concentration (cm^{-3}),

[5]Oxidation rate is larger in ¡001¿ than in ¡011¿ direction, Basic Characterization of the New Oxidation System, Seminar of the Institute of Optoelectronics, 11.07.2007,Andrea Kroner.

μ_n = The electron mobility (cm^2/V-s)

For a Si doping concentration of $1.7x10^{18}$(collected form the sample recipe file) in GaAs and the electron mobility depending on this doping concentration 8000 (cm^2/V-s) and the elementary charge $1.6x10^{-19}$C, the conductivity found of n^+ doped layer is 2176 Ʊ/cm, whereas, the conductivity of Au is $4.52x10^7$ Ʊ/cm which is five order of magnitude higher.

The maximum sheet resistance of the semiconductor material faced by the array in the second type of design is givn by-

$$R_{sh} = \frac{\rho l}{A} = \frac{l}{\sigma t w} \tag{6.3}$$

Here, l (573 μm), t (1.5 μm) and w (80 μm) are the length, thickness and width of the material respectively. After entering all the values in Eqn.(6.3), the theoretical maximum sheet resistance (neglecting Au resistance) calculated is about 22 Ω. Though, a factor 2 can be inserted in Eqn. 6.3 from the fact that the bondpad has been incorporated in both sides of the array as redundancy to reduce the sheet resistance by half, but during measurement the redundancy bondpad was not used due to the smaller array.

6.5 Processed Wafer Characterization

One-third (the best quality part which is close to the center of full wafer) of quarter of 2" wafer was fabricated and fully characterized as shown in Fig. 6.10 which can give some information regarding the homogeneity of the epi-growth, the location of good quality part in the wafer, etc. This characterization was done in terms of average threshold current and maximum optical output power of the corresponding unit cell. The dimensions of the active diameters are not written in the unit cells of Fig. 6.10 since there is strong inhomogeneity of the oxide apertures of the devices but roughly it can siad that the oxide apertures vary from approximately 5 to 13 μm over the full wafer. Moreover, in the right part of the wafer, 'x' mark in some unit cells is indicating that those VCSELs do not give any lasing due to have the less quality of epitaxial growth since this region is away from the center even though current flows through the devices very well. Four unit cells with shaded marks are characterized by LIV curves which are already shown. Optical spectra are measured in the unit cells marked by alphabetical letters (A, B,...I).

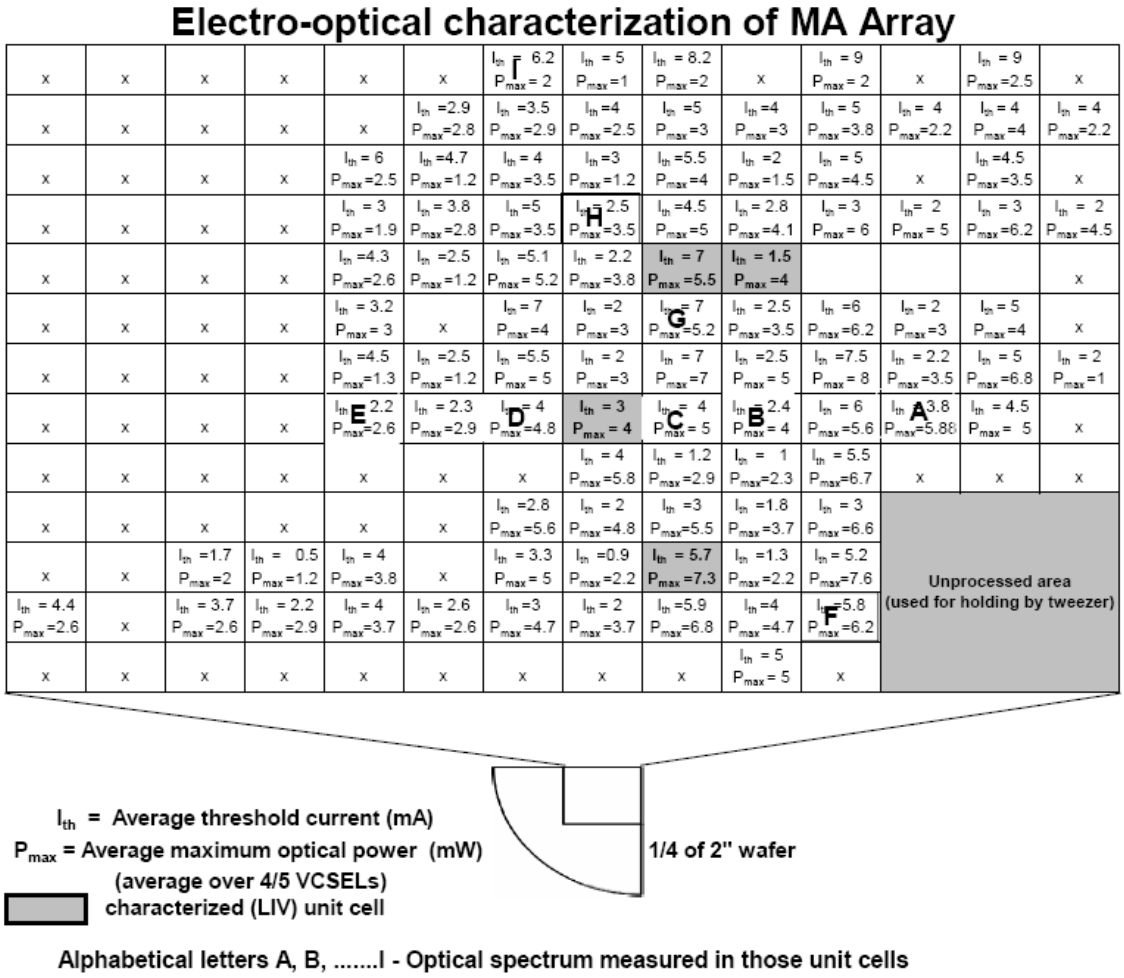


Figure 6.10: *One-third of quarter of 2″ wafer was fabricated and fully characterized in terms of the threshold current and maximum optical power emitted from the devices making average of 4/5 VCSELs in one unit cell.*

6.6 Optical Spectra

Fig. 6.11 shows the optical spectra of different positions of the wafer which was measured at the room temperature. The Optical Spectrum Analyzer was used in this measurement connected to the multimode fiber through which emitted light from the VCSELs is coupled. It is seen that the emission wavelength is shifted with respect to the position. Moving horizontally and diagonally along from one part of the wafer to another part give significant change of wavelength as indicated in Fig. 6.11. After calculating, approximately 3.2 nm/mm shift of wavelength due to horizontal movement and 5.2 nm/mm shift of wavelength due to diagonal movement are found.

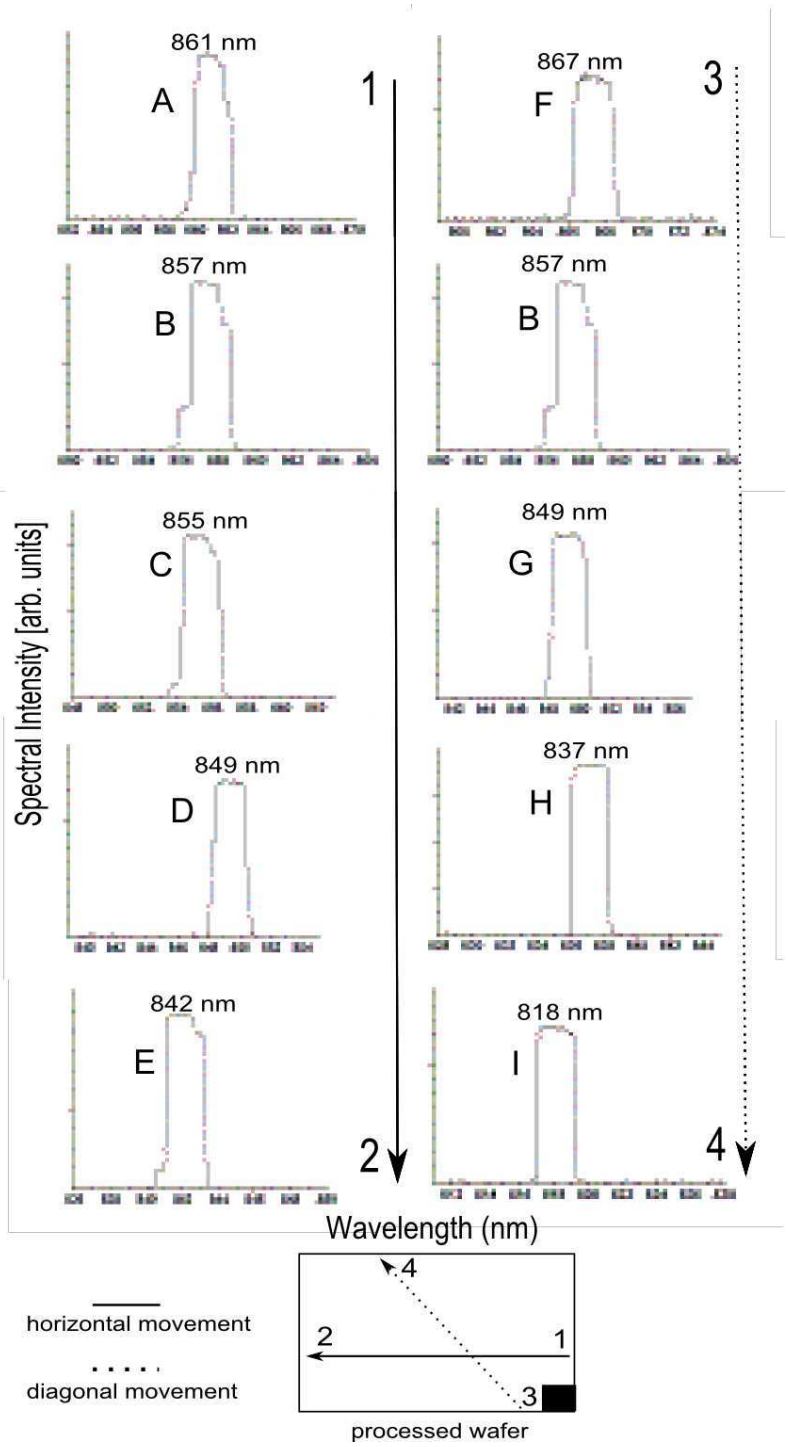


Figure 6.11: *Optical spectra at different positions of processed wafer are shown. The numerical value at the top of each spectrum indicates the emission wavelength of that corresponding position. The wavelength shift with respect to position is categorized as horizontal and diagonal movement. The alphabetical letters in each spectrum indicates the position of the unit cell in the wafer which have been marked in Fig. 6.10*

6.7 Summary

In this chapter, the basic characterization, LIV curves, extraction of some other important parameters from LIV curves, calculation of series resistance and comparison of two different types of unit cells and at the end the average threshold current and average maximum optical power of all unit cells over the full wafer have been described. The optical spectra of VCSELs are also measured.

Appendix A

Simulation Script

For obtaining the band diagram, band diagram with biasing and refractive index profile of the full VCSEL structure as shown in Chapter 2, the simulation script used in SimWindows is as follows:

```
#----------------------n+ BUFFER REGION STARTS HERE ----------------
structure material=gaas alloy=al length=2 conc=0.00
doping length=2 Nd=1.7e18  Nd_deg=2  Nd_level=0.006
grid length=2 points=250

structure material=gaas    alloy=al     length=0.0491    conc=0.2
doping length=0.0491 Nd=1.4e18+(2.5e18-1.4e18)/0.0491*d  Nd_deg=2 Nd_level=0.006
grid length=0.0491 points=49
#----------------------n+ BUFFER REGION ENDS HERE ----------------
#----------------------n-DBR REGION STARTS HERE ----------------
repeat start
structure material=gaas alloy=al length=.0124 conc=.27+(0.47-0.27)*d/.0124
doping length=.0124 Nd=2.3e18+(2.7e18-2.3e18)/0.0124*d  Nd_deg=2 Nd_level=.03
grid length=.0124 points=12

structure material=gaas alloy=al length=.0192 conc=.47+(.9000-.47000)*d/.0192
doping length=.01920 Nd=2.7e18+(3.1e18-2.7e18)/0.0192*d  Nd_deg=2 Nd_level=.036
grid length=.0192 points=19

structure material=gaas alloy=al length=.0297 conc=.90
doping length=.0297 Nd=3e18+(1.7e18-3.1e18)*d/.0297 Nd_deg=2 Nd_level=.036
grid length=.0297 points=29

structure material=gaas alloy=al length=.0192 conc=0.9+(0.47-0.9)/0.0192*d
doping length=.0192 Nd=1.7e18+(1.5e18-1.7e18)*d/0.0192 Nd_deg=2  Nd_level=.036
grid length=.0192 points=19

structure material=gaas alloy=al length=.0124 conc=0.47+(0.27-0.47)*d/.0124
doping length=.0124 Nd=1.5e18+(1.3e18-1.5e18)/.0124*d Nd_deg=2  Nd_level=.036
grid length=.0124 points=12

structure material=gaas alloy=al length=.0368 conc=0.2
doping length=.0368  Nd=1.4e18+(2.5e18-1.4e18)/.0368*d Nd_deg=2 Nd_level=.03
grid length=.0368 points=36
repeat=38
#----------------------38 PAIRS OF n-DBR REGION ENDS HERE ----------------
structure material=gaas  alloy=al  length=.0124  conc=0.27+(0.47-0.27)/.0124*d
doping length=.0124   Nd=2.3e18+(2.7e18-2.3e18)/.0124*d  Nd_deg=2  Nd_level=.006
grid length=.0124 points=13

structure material=gaas alloy=al length=.0192 conc=0.47+(0.9-0.47)/.0192*d
doping length=.0192 Nd=2.7e18+(3.1e18-2.7e18)*d/.0192  Nd_deg=2  Nd_level=.006
grid length=.0192 points=19
```

```
structure material=gaas alloy=al length=.0297 conc=0.90
doping length=.0297  Nd=3.1e18  Nd_deg=2 Nd_level=.006
grid length=.0297 points=29

structure material=gaas alloy=al length=.0192  conc=0.9+(0.47-0.9)/.0192*d
doping length=.0192 Nd=3.1e18+(1.3e18-3.1e18)*d/.0192  Nd_deg=2  Nd_level=.006
grid length=.0192 points=19

structure material=gaas alloy=al  length=.0125  conc=0.47
doping length=.0125  Nd=3.1e18+(1.3e18-3.1e17)*d/.0125  Nd_deg=2  Nd_level=.006
grid length=.0125 points=12

structure material=gaas alloy=al  length=0.0443  conc=0.47
doping length=0.0443  Nd=3.1e18+(3.1e17-1.1e17)*d/0.0443  Nd_deg=2 Nd_level=.006
grid length=0.0443 points=44
#----------------------QUANTUM WELL REGION STARTS HERE ----------------
structure material=gaas alloy=al  length=0.0365  conc=0.47+(0.27-0.47)/0.0365*d
doping length=0.0365
grid length=0.0365 points=36

structure material=gaas alloy=al  length=0.0099  conc=0.27
doping length=0.0099
grid length=0.0099 points=36

repeat start
structure material=gaas alloy=al  length=.008 conc=0
doping length=.008
grid length=.008  points=8

structure material=gaas alloy=al length=.010 conc=0.27
doping length=.010 Nd=0 Nd_deg=0 Nd_level=0
grid length=.010 points=200
repeat=2
structure material=gaas alloy=al  length=0.008  conc=0
doping length=0.008
grid length=0.008 points=8

structure material=gaas alloy=al  length=0.0099  conc=0.27
doping length=0.0099
grid length=0.0099 points=36
#----------------------QUANTUM WELL REGION ENDS HERE ----------------
structure material=gaas alloy=al  length=0.0371  conc=0.27+(0.47-0.27)/0.0371*d
doping length=0.0371
grid length=0.0371 points=36

structure material=gaas alloy=al  length=.0258  conc=0.47
doping length=.0258 Na=3.9e16+(1.2e18-3.9e16)/.0258*d Na_deg=4    Na_level=.0350
grid length=.0258 points=26

structure material=gaas alloy=al length=.0615 conc=0.47
doping length=.0615 Na=1.2e18+(1.8e18-1.2e18)/.0615*d  Na_deg=4 Na_level=.051525
grid length=.0615 points=61

structure material=gaas alloy=al length=.0192 conc=0.47+(0.9-0.47)/.0192*d
doping length=.0192 Na=1.8e18+(1.1e19-1.8e18)/.0192*d  Na_deg=4  Na_level=.075
grid length=.0192 points=19
#----------------------OXIDATION REGION STARTS HERE ----------------
structure material=gaas alloy=al length=.032 conc=1
doping length=.032  Na=1.2e19   Na_deg=4    Na_level=.075122
grid length=.032  points=32
#----------------------OXIDATION REGION ENDS HERE ----------------
structure material=gaas alloy=al length=.0192 conc=.9+(.47-.9)*d/.0192
doping length=.0192 Na=1.1e19+(1.8e18-1.1e19)/.0192*d   Na_deg=4  Na_level=.0515
grid length=.0192 points=19
```

```
structure material=gaas alloy=al   length=0.031   conc=0.47
doping length=0.031 Na=1.8e18   Na_deg=4    Na_level=.035025
grid length=0.031  points=31

structure material=gaas alloy=al length=.0192 conc=0.47+(0.9-0.47)/.0192*d
doping length=.0192 Na=1.8e18-(2e18-1.8e18)*d/.0192 Na_deg=4 Na_level=.025
grid length=.0192 points=19

structure material=gaas alloy=al length=.0297  conc=0.9
doping length=.0297 Na=2e18+(3e18-2e18)/.0297*d   Na_deg=4 Na_level=.025
grid length=.0297 points=29

structure material=gaas alloy=al length=.0192        conc=0.9+(0.47-0.9)/.0192*d
doping length=.0192 Na=3e18+(2.6e18-3e18)/.0192*d  Na_deg=4 Na_level=.025
grid length=.0192 points=19

structure material=gaas alloy=al length=.0124        conc=0.47+(0.27-0.47)/.0124*d
doping length=.0124  Na=1.8e18+(1.5e19-1.8e18)/.0124*d   Na_deg=4 Na_level=.025
grid length=.0124 points=12
#----------------------p-DBR REGION ENDS HERE ----------------
repeat start

structure material=gaas alloy=al length=.0368        conc=0.2
doping length=.0368  Na=1.7e18   Na_deg=4 Na_level=.025
grid length=.0368 points=36

structure material=gaas alloy=al length=.0124  conc=0.27+(0.47-0.27)/.0124*d
doping length=.0124  Na=1.5e18+(1.8e18-1.5e18)/.0124*d   Na_deg=4 Na_level=.025
grid length=.0124 points=12

structure material=gaas alloy=al length=.0192    conc=0.47+(0.9-0.47)/.0192*d
doping length=.0192  Na=1.8e18+(2.2e18-1.8e18)/.0192*d   Na_deg=4 Na_level=.025
grid length=.0192 points=19

structure material=gaas alloy=al length=0.0297    conc=0.9
doping length=0.0297  Na=2.2e18+(3e18-2.2e18)/0.0297*d   Na_deg=4 Na_level=.025
grid length=0.0297 points=29

structure material=gaas alloy=al   length=0.0192 conc=0.9+(0.47-0.9)/0.0192*d
doping length=0.0192  Na=3e18+(4e18-3e18)/0.0192*d   Na_deg=4 Na_level=.025
grid length=0.0192  points=19

structure material=gaas alloy=al   length=0.0124  conc=0.47+(0.27-0.47)/0.0124*d
doping length=0.0124  Na=4e18+(1.5e18-4e18)/0.0124*d   Na_deg=4 Na_level=.025
grid length=0.0124  points=12

repeat=23
#----------------------23 PAIRS OF p-DBR REGION ENDS HERE ----------------
#----------------------p+ REGION STARTS HERE ----------------
structure material=gaas alloy=al   length=0.009        conc=0.20
doping length=0.009  Na=1.7e18+(3.9e18-1.7e18)/0.009*d   Na_deg=4 Na_level=.0257
grid length=0.009  points=9

structure material=gaas alloy=al   length=0.0084        conc=0.0
doping length=0.0084  Na=4.9e18  Na_deg=4     Na_level=.025
grid length=0.0084   points=9

structure material=gaas alloy=al   length=0.29        conc=0.0
doping length=0.29  Na=8.4e18+(1.6e20-8.4e18)/0.29*d  Na_deg=4     Na_level=.025
grid length=0.29   points=290
#----------------------p+ REGION ENDS HERE ----------------
```

Appendix B

Standing Wave Pattern of E-Field Amplitude Calculation

[6]The complex propagation coefficient,

$$\gamma_m = \frac{2\pi\bar{n}_m}{\lambda} - i\frac{\alpha_m}{2} \tag{B.1}$$

where, m = index for each epitaxial layer
α_m = Absorption coefficient of all layers except the QWs.
The two symbols,

$$\gamma_m^+ = \frac{\gamma_m + \gamma_{m+1}}{2\gamma_m} \tag{B.2}$$

$$\gamma_m^- = \frac{\gamma_m - \gamma_{m+1}}{2\gamma_m} \tag{B.3}$$

$$E_m^+ = (\gamma_m^+ E_{m+1}^+ + \gamma_m^- E_{m+1}^-) \exp\{i\gamma_m(z_{m+1} - z_m)\} \tag{B.4}$$

$$E_m^- = (\gamma_m^- E_{m+1}^+ + \gamma_m^+ E_{m+1}^-) \exp\{-i\gamma_m(z_{m+1} - z_m)\} \tag{B.5}$$

where, E_m+ and E_m- denote the complex field amplitudes of the waves at the interface $z = z_m$ and $(z_{m+1} - z_m)$ is the layer thickness.

In each layer, the electric field is the superposition

$$E_m(z) = E_m^+ \exp\{-i\gamma_m(z - z_m)\} + E_m^- \exp\{+i\gamma_m(z - z_m)\} \tag{B.6}$$

of two monochromatic plane waves in z-direction.

[6] Reference : **Basic Properties of VCSEL, by Dr. Rainer Michalzik , pp. 65, Manuscript of the course, Advanced Optoelectronic Communications Systems.**

Appendix C

Reflectivity Spectrum Calculation

[7]The characteristics matrix of each epitaxial layer has to be calculated at first. The equation used to calculate the characteristics matrix of one layer, M_1

$$M_1 = \begin{vmatrix} A_1 & B_1 \\ C_1 & D_1 \end{vmatrix} \tag{C.1}$$

where,

$$A_1 = cos(k_0 * h_1 * \overline{n}_1) = C_1 \tag{C.2}$$

$$B_1 = -\frac{i}{\overline{n}_1} sin(k_0 * h_1 * \overline{n}_1) \tag{C.3}$$

$$D_1 = -i\overline{n}_1 * sin(k_0 * h_1 * \overline{n}_1) \tag{C.4}$$

here,
$k_0 = \frac{2\pi}{\lambda}$ = wavenumber; $\overline{n}_1$ = refractive index of a layer; h_1 = Layer thickness;
Calculation of combined characteristics matrix:
The combined characteristic matrix, M can be calculated considering all the epitaxial layers.

$$M = \begin{vmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{vmatrix} \tag{C.5}$$

where, M_{11}, M_{12}, M_{21}, M_{22} are the matrix elements of the combined matrix, M.
Important to mention that the calculation of M is just the multiplication of the matrices of all individual epitaxial layers. But for repeating layers (e.g. 38 pairs of n-DBR and 23 pairs of p-DBR), the formula used,

$$MM_1 = (M_1 * M_2 * M_3 * M_4 * M_5)^{38}$$
$$MM_2 = (M_6 * M_7 * M_8 * M_9 * M_{10})^{23}$$
$$M = MM_1 * MM_2$$

[7] The equations mentioned in this appendix are collected from: **Principles of Optics, by Max Born and Emil Wolf, pp. 58-69, Cambridge University Press, Published 1999.**

where,
M_1....M_5 are the epitaxial layers to form one n-mirror pair;
M_6....M_{10} are the epitaxial layers to form one p-mirror pair

$$r_1 = (M_{11} + M_{12} * \overline{n}_{\text{last}})\overline{n}_{\text{first}} \tag{C.6}$$

$$r_2 = (M_{21} + M_{22} * \overline{n}_{\text{last}}) \tag{C.7}$$

Calculation of Reflection and Transmission Co-efficient: If the reflection coefficient and transmission coefficient can be denoted as r and t respectively, then

$$r = \frac{r_1 - r_2}{r_1 + r_2} \tag{C.8}$$

$$t = \frac{2n_1}{r_1 + r_2} \tag{C.9}$$

$$\text{Reflectivity} = |r|^2 \tag{C.10}$$

$$\text{Transmittivity} = \frac{\overline{n}_{\text{last}}}{\overline{n}_{\text{first}}}|t|^2 \tag{C.11}$$

here, $\overline{n}_{\text{last}}$ = Refractive index of the last layer, i.e. air,

$\overline{n}_{\text{first}}$ = Refractive index of the first layer

Appendix D

Mask Layout Using AutoCAD

D.1 Introduction

For drawing the mask layout in this work, the CAD software, AutoCAD is used. It is very important to be familiar with this software in advance so that the mask layout can be drawn without any error and in an efficient way. For this reason, one needs to know the proper use of the tools or entities available in this CAD software. In this appendix, the usage of some handy entities of AutoCAD will be discussed which are extremely helpful to draw the layout. The basic entities (e.g. lines, circles, arcs and so on) are very easy to deal with, that's why, those will be left for the readers to learn by themselves.

D.2 Drawing Complicated Structures

Complicated structures like contact ring or the structure shown in Fig.D.1 can be drawn in two ways:

Pline	**Boolean**
Draw help structures on separate layer.	Draw the structure as needed.
Pline connect on desired points by using snap.	Boolean: XOR (Exclusive OR).
Close Pline and check with hatch.	NA

Table D.1: *Two ways of drawing the mask layout.*

D.3 Contact Ring

The procedures of drawing the contact ring are as follows:

- Draw two concentric circles by **SNAP or CENTER** option.
- Form the semicircles by **TRIM** (cutting the one half of those two circles).

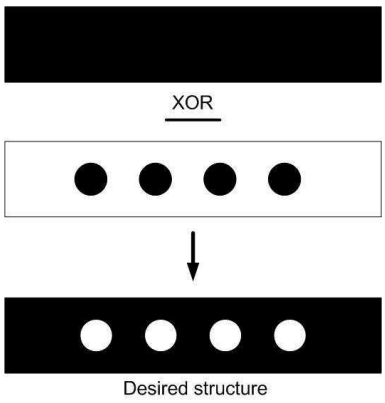


Figure D.1: *Illustration showing that how XOR operation works for the complicated structures. In the above figure (bottommost) the shaded region is made by 1 XOR 0 = 1 and in the unshaded region(circle) 1 XOR 1 = 0. This way can also be called as subtractive method.*

- Delete that straight line which was used in trimming.
- Draw a new straight line which connects the two end points of those two circles.
- Edit polyline, command: **PEDIT.**
- Select the polyline and give the answer by typing **'Y'** once the prompt comes.
- Join these three parts.
- Mirror and type **'N'**once the prompt comes 'Do you want to delete the old one?'
- Edit the polyline by joining these two parts, i.e. make it one unit.
- Test the unit by **HATCH** command and undo the hatching afterwards.

D.4 Deletion of Layer:

Procedures of deleting one used layer are as follows:

- Necessary command: **PURGE.**
- Prompt LAYER: name_x.
- Type : **"Y"**.

Make sure that the layer which needs to be deleted that should be CURRENT LAYER and close the file and reopen it.

D.5 Move the Structure

The procedures of moving the drawing of one layer to another layer are as follows:

- Necessary command: **CHANGE.**
- Select objects: selection.
- Properties/change point: Properties.
- Change what properties: Color/Layer/Ltype: Layer.
- New layer: layer_x.
- Change what properties: color (sometimes).
- Press **ENTER.**

Make sure that the layer name which is typed (mentioned above) that must be created earlier and the object selected that must be copied (for backup) in some place.

D.6 Few Important Commands

These following commands also need to be known-

- List
- Change
- Wblock
- Insert
- Explode

By the command, **WBLOCK** the drawing in one file can be moved in another file. But the file where it will be transferred that will remain there as block, i.e. composite unit. To make it unblock or for splitting that block into many units the command, **EXPLODE** will be used. For deleting the layer where the drawing was transferred from another file, we have to delete the block name which was used while transferring. Use **PURGE** to delete this block: Press no, no and so on then we will get that block. Then delete the layer by using **PURGE.**
N.B. The layer where the drawing was transferred can not be deleted even though this layer is completely empty unless and until the block is removed.

D.6.1 Procedure

- Open the file from where it is needed to transfer the drawing.
- Command: **wblock.**
- One pop-up will come as ”create drawing file”.
- Give the name of the drawing file.
- And then **ENTER.**
- Insertion base point: selection.
- Select objects: Selection.
- The objects will disappear.
- Open another file where want to transfer.
- Command: **INSERT.**
- Block name: Give the name which was used earlier.
- That block will come→Insertion point: scale X: 1→ Y scale: like X →Angle: 0 →And then ENTER.

D.7 Few Tips

- All the structures should be closed, it is necessary to check all the structures very well.
- All the drawn structures should be checked by hatching at the end to make sure that the desired region of those structures will be covered by chrome.
- The mask should be designed in such a way so that the consumption of chrome in the mask can be reduced. Because less chrome in the mask always gives some advantage in aligning the profile by the mask aligner.

D.8 Summary

In this appendix, some important instructions in drawing the mask layout and some entities for AutoCAD software are briefly discussed which may be helpful for the beginners to draw the layout in a right way.

Appendix E

Instructions for Cleanroom

E.1 Introduction

The name of this appendix is little bit startling, Instructions for Cleanroom. In fact, these instructions are not for adapting the cleanroom environment, these are to be familiar with the cleanroom machineries and equipments instead. How to operate the quite sophisticated machines in the cleanroom, what are the cautionary steps while operating these machines, which process should be done after which step, some handy tips along with the basic principles of those machines are outlined in this appendix from which one can understand clearly the operating procedures of the machines. These machines do not have any official manual or any written documents in the cleanroom. In particular, before operating these machines one has to take the introduction officially (from the responsible person of each machine) ahead of time so that he or she can be allowed to use the machine independently. Actually those introductions are really effective for understanding the way of handling the machines properly, but at the same time if one can go through this document that will be a really fruitful work for more comprehensive understanding. However, in this appendix, the operating procedures of only those machines are described of which I was allowed to use independently after taking the official introduction. If this appendix would be treated as guideline or manual of the machines to everyone, then I will think my efforts have become successful.

E.2 Optical Lithography

E.2.1 Mask Aligner (Karl Suss MJB3)

While turning on

- Turn on the **N_2 (stickstoff) and compressed air** at the mask aligner.
- Press the **POWER** button of the UV lamp. Wait till **RDY** is displayed then press **START** and wait till the display shows the power **274 W.**

- Turn on the power of the mask aligner by pressing the button **NETZ.** Do three empty exposures of 10 sec to finally warm up the lamp. Before exposure one must make sure the **CONTACT** (blue light) is turned on by rotating the vertical knob (coarse one) fully.
- Write down the switch on time and the user name in the mask designer booklet.[8]

Few buttons

- **Soft contact** To get stuck the wafer chuck and the sample. After putting the sample on top of the wafer chuck, this button should be pressed. Note that this push button must be turned on during flood exposure.
- **Bleichten** Optical Exposure
- **HP/ST** The air pressure will come through the hole (edge of the wafer chuck) against the mask and help to get stuck the mask and sample (wafer chuck). This push button has to be pressed once the alignment between the mask and the sample is perfectly done. Press HP/ST, just before pressing BLEICHTEN.
- **Contact/Separation** SEPARATION allows a user to set the separation between the wafer and the photomask during the alignment procedure. For movement in X-Y direction, SEPARATION must be active, indicating that some distance between the wafer and the mask. When alignment is complete and just before the exposure, this has to be deactivated by moving the knob manually, i.e. green light gets turned off, lead to turn on the CONTACT button.
- **Vacuum Kammer** Just before the exposure, HP/ST and then this button should be pressed.

Mask holder

Before using the mask in the mask holder, there is a screw in the holder for the vacuum which should be checked that whether it is tight or loose. Tighten it if it is loose and then put the mask on it and then press **VACUUM** . It will help the mask to get stuck with the holder. While putting the mask on the holder, the holder should not be kept fully on the surface which will force to get stuck the mask holder with the surface (after pressing VACUUM) creating some problems in raising the mask holder. So the mask holder should be kept in such a way so that some part of it becomes exposed in the air.

While keeping the mask on it

Mask has two surfaces, top (GLASS side) and bottom (CHROMIUM side). Mask should be placed on the mask holder in such a way so that Chromium side remains on downside

[8] These four statements are official instructions

and glass side gets top side, i.e. glass side gets the UV light directly after pushing this in the aligner. Or in other words, chromium side should face the sample. Keep in mind, the chromium portion in the mask will block the UV light.

Timer

There is a timer which should be adjusted manually. There is a knob (in a smaller circle) which indicates the Multiplying factor. There is also another knob which points the marking in the bigger circle.

Power display

In the mask aligner there is one display for showing the power supplied to the UV lamp and the power received by the sample during the optical exposure which can be switched from one another. Normally it shows the power supplied to the UV lamp which ranges from 380-400 watt. But pressing the switch closer to this display will show DS (Detector Side) 12 mw/cm^2 which will indicate the optical power (UV light) detected by the detector.

For alignment

In the mask aligner used SOFT CONTACT always remain pressed. Because SOFT CONTACT only becomes active when the sample is ready for the exposure, or in other words, when the sample and wafer chuck inside the aligner will be kept and the vertical knob (coarse one) fully is rotated to bring the wafer up, then vacuum will come through hole of the wafer chuck and sample will get stuck with the wafer chuck. So soft contact already pressed or not pressed - doesn't matter.
For alignment, four movements are necessary after putting the sample on the wafer chuck inside the aligner, X, Y, Z and angle. 'Z' (height) alignment is necessary as soon as the wafer is kept inside the aligner. For height adjustment, the wafer is brought up by vertical knob (coarse one) and then adjust the height by the vertical knob (fine one). Then it is mechanically locked into place by tightening the screw. The wafer is then moved away from the photomask a pre-specified amount for alignment so-called separation mode.

Microscope

The microscope used for alignment has three lenses which are used in aligning the structures. Out of these three GREEN one has the highest magnification (used for final alignment) and the RED one has the lowest magnification (used for rough alignment).

Simple tricks for alignment

Alignment in the centre : Movement of the wafer in X & Y direction
Alignment in the corner : Angle Movement
Or

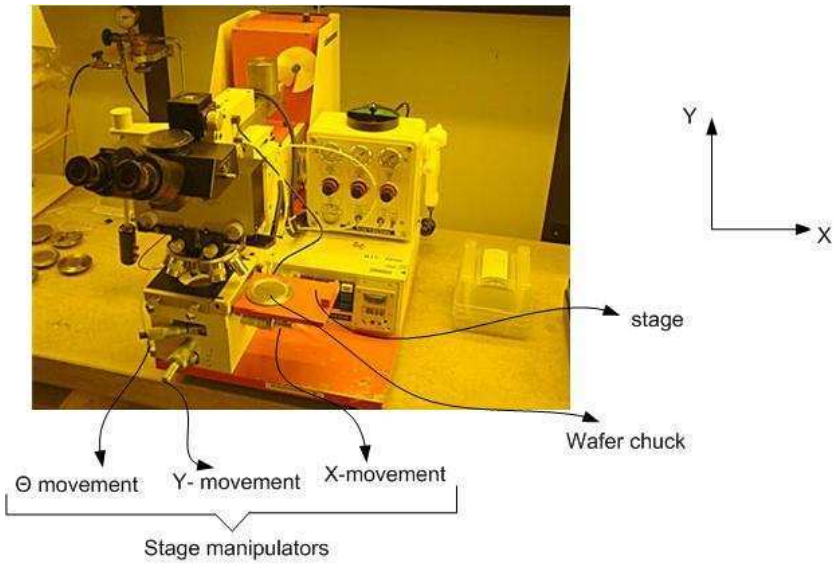


Figure E.1: *Mask Aligner (KARL SUSS MJB3) used for alignment.*

Alignment in one corner : Movement of the wafer in X & Y direction
Alignment in opposite corner : Angle Movement
Or
Alignment in one corner : Half alignment by X & Y and the rest half by angle
Alignment in opposite corner : Half alignment by X & Y and the rest half by angle
At first rough alignment is necessary. For that, the feature orientation of the mask and wafer should coincide. If not, take the sample out and rotate the sample (90^0 or 180^0) as required and then see under the microscope. After rough alignment then the above mentioned tricks should be applied. This rough alignment is done by using the lens (RED) with lowest magnification. Afterwards, the lens with the highest magnification should be used for precise alignment and the above tricks again.
The marking in X-Y movement knob of the mask aligner is very helpful during the alignment because it tells how much movement (in μm) in X-Y direction.
N.B. When it seems that the alignment is perfect, then wafer chuck can be moved upwards by deactivating the **separation** mode and then checking under the microscope again.

While taking the sample out from the aligner

After optical exposure, the sample needs to be taken out. Then the following steps has to be done:

- Press Vacuum Kammer
- Press HP/ST
- Bringing back the wafer down by vertical knob (coarse)
  Just maintain these three steps.

While turning off

- Make sure that the mask has been already taken out from the mask holder before pressing the button **NETZ**. Without taking the mask out if we press **NETZ** then the mask will fall onto the microscope since the vacuum will be inactive.
- Turn off the power of the mask aligner by pressing the button **NETZ**. Then turn off the power supply of the UV lamp.
- Wait at least 30 minutes (so the lamp can cool down) and then switch off the N_2 and compressed air.
- Write down the switch off time and your name in the mask designer booklet. [9]

After exposure and the development

Check the sample under the optical microscope (discussed later) after turning the UV filter on. For that there is a software in the desktop, **CAMERA** . Click it and then click on **START** once the software opens.

E.2.2 Optical Microscope

Figure E.2: *Optical Microscope (Reichert Jung Polyvar) used to check the structure on the sample.*

The Reichert-Jung Polyvar is a high resolution optical microscope for wafer inspection. In fact, this microscope is used after development for checking the profiles on our sample which has three important knobs need to be controlled.
1) X-Y movement
2) Focusing the lens of the microscope
3) Light filter
Another knob needs to be controlled, light intensity knob for the camera. There are six

[9] These four statements are official instructions

different lenses with different magnification in this microscope. Starting form the lens with lowest magnification, the profiles on our samples should be checked. For that, focusing knob has to be tuned. Two focusing knobs, coarse and fine tuning. At first coarse tuning, but in changing from one lens (lower magnification) to another lens (higher magnification) fine tuning is sufficient to get the nice picture.

E.2.3 Preparation for Spin Coating

Take a syringe and take the proper photoresist. Take the plastic foil and lie it on the spin coating machine. Make a hole by a knife in the foil paper in order to ensure nothing is inside of the hole where chuck will be kept to rotate the sample. Choose the appropriate chuck depending on the sample size, e.g. if small sample then chuck having small hole is better.

- Press Ein/Aus - to turn on the spin coating machine - display comes
- Press F4
- Program no. 07, depending on the requirements
- Press - Enter
- Press F1 - Return to the main menu

After checking the program and chuck, the sample is covered with resist, then press VACUUM and then press START. But before putting the resist on the sample, blowing by dry N_2 is always suggested. It has two main purposes:
1) After drying the sample at 120^0 for 10 minutes, it needs some cooling.
2) Dry N_2 will help to remove all the undesired particles from the sample surface.

E.2.4 Some Important Steps

- Keeping the sample on the spin coating machine and turning the VACUUM on, the edge of the sample should be cleaned by Edge Bead Remover. Because so-called edge bead prevents in getting the good resolution. For that, take the edge-bead remover liquid by a syringe and clean the edges of the sample.
- Cleaning the chuck by acetone/MP[10] and then drying it.
- May be after spin coating there is some resist at the backside of the sample which can create some problem in getting the desired profile on the sample after optical exposure since the resist has certain thickness. So the backside should be cleaned by acetone.

[10]Methyl-Pyrrolidone

E.2.5 Wafer Cleaning

- Take the substrate holder having some V grooves where quarter wafer (sample) can be kept.
- Take Acetone in a beaker and keep the sample inside for 5 minutes.
- Take Propanol-2 in a beaker and keep the sample inside for 5 minutes.
- Dry it by blowing N_2.

E.2.6 Mask Cleaning

After every optical exposure, we should clean the mask before the re-usage. The main ways of cleaning the mask are as follows:

- Put the mask in the MP solution for a while to remove the photoresist which can remain on the chrome surface during optical exposure, then
- in the acetone for 4-5 minutes then
- in the iso-propanol for 4-5 minutes

Exceptional: TI35ES (Image Reversal resist, has a very high resolution but very dark, difficult for alignment) is soluble in acetone. So, while cleaning after exposure, the mask can be put directly in the acetone instead of using the MP at first.
N.B. Acetone removes all organic materials from the wafer surface and iso-propanol removes acetone. So it is advantageous to use iso-propanol after acetone to remove all organic materials from the wafer surface.

E.2.7 Hot Plate

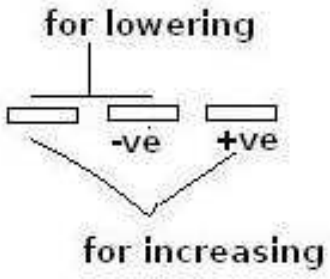


Figure E.3: *Temperature control in hot plate.*

For controlling the temperature in the hot plate, there are three buttons need to be controlled. For example, 120^0C is needed. Then if the initial temperature is less than 120^0C

then the leftmost and rightmost button should be pressed at a time. But this is just the setting, the temperature will not go into this temperature instantaneously. After a while, the temperature will reach at 120^0C.

E.2.8 Removal of Photoresist

- To remove any type of photoresist from the sample, MP(1-Methyl 2- Pyrrolidon) is used.
- Take a beaker and pour some MP into it and then heat it at 120^0 C.
- Then keep the sample on a sample holder and put it on MP beaker and keep it for 12 minutes.
- Clean the sample by water since MP is very sticky liquid.
- Check in the microscope to make sure that all the resist gets removed from the sample.
- If not, then put the sample again in the MP solution.
- Then in acetone (3 minutes) for cleaning
- Iso-propanol (3 minutes)
- Drying by N_2

E.2.9 Polyimide Process

1) Take the appropriate polyimide from the refrigerator 2 hour earlier before the usage.
2) Polyimide has water absorption ability. To avoid this problem, covering the face with the mask is always recommended which prevents the breathing going into the polyimide.

E.2.10 Baking (before photoresist application)

The main objective of this baking is to dry the wafer completely. Any moisture on the wafer surface would interfere with the photolithography process causing it to yield poor results. The hot plate at 120^0 C is used for this type of baking.

E.2.11 Soft-Baking (after photoresist application)

Soft-baking is the step during which almost all of the solvents are removed from the photoresist coating. Soft-baking plays a very critical role in photo-imaging. The photoresist coatings become photosensitive or imageable, only after softbaking. The hot plate at 90^0 C is for soft-baking.

E.2.12 Hard-Baking

Hard-baking is the final step in the photolithographic process. This step is necessary in order to harden the photoresist and improve adhesion of the photoresist to the wafer surface. Any type of hotplate depending on the resist specification can be used for this hard baking.

E.2.13 Reversal Baking

This special type of baking should be done just after exposure in order to make the exposed resist region inert resulting negative patterning which is applicable for Image Reversal Resist.

E.2.14 Resist Patterning

There are four different types of resist patterning can be done depending on the type of resist:

- Positive patterning- using positive resist
- Negative patterning- using negative resist
- Image reversal – using positive resist
  N.B. In Image reversal resist reversal baking temperature and duration of baking will determine the slope of the resist profile which will develop after development.

E.2.15 Keep in Mind

1. After spin coating (putting the photoresist on the sample), it is necessary to clean the wafer chuck (for spin coating) to be usable for the next process. For that, acetone can be used. Take the acetone bottle from the chemical workbench and keep spraying on the chuck for cleaning. Dry it roughly by tissue paper afterwards and then put it on the hot plate (92^0C) for good drying.

2. While developing, the solution used to develop should be well-mixed. For that the solution should be stirred thoroughly for a while by a mixer (available in the workbench).

3. The cleaning liquids, e.g. acetone, isopropanol, MP and methanol should be disposed in the proper place where the names of the liquids are labeled.[11]. It should never be disposed in the sink of the workbench.

[11] **GESPERRT**: German word whose meaning is - **not for using**

E.2.16 Ultrasonic Cleaner

Basic principle

[12]In an ultrasonic cleaner, the object to be cleaned is placed in a chamber containing a suitable ultrasound conducting fluid (an aqueous or organic solvent, depending on the application). An ultrasound generating transducer is built into the chamber or may be lowered into the fluid. It is electronically activated to produce ultrasonic waves in the fluid. Electrical signal converted into a mechanical force by the transducer creates a compression wave (sound waves whose frequency is greater than 20 KHz, outside the range of hearing ability of human being) in the liquid of the tank which helps to form the bubbles in the liquid.
Instead of moving the sample (attached in the holder) in the solution by hand, ultrasonic cleaner can be used to remove the undesired materials e.g. photoresist from the wafer surface. For that-

Figure E.4: *Ultrasonic cleaner.*

- Keep the sample on a sample holder.
- Take the solution in a beaker.
- Put the wafer holder along with the wafer in the solution.
- Open the tray of the ultrasonic cleaner and put this beaker inside the cleaner.
- Press EIN/AUS
- Adjust the time.
- Press SET+ ↑ / ↓ for adjusting the required time.
- Press HANDSTART to start the cleaning process.

[12]http://en.wikipedia.org/wiki/Ultrasonic_cleaning

E.3 Different Issues

E.3.1 HF Dip

(Chemical Formula: HF in Aqueous Solution.) To remove undesired oxide layers from the sample.

E.3.2 HCL Dip

To remove the oxide layers from the sample, e.g. before loading the sample in the evaporation machine.

E.3.3 2" Wafer Cleaving

The procedure of cleaving is shown in Fig. E.5.

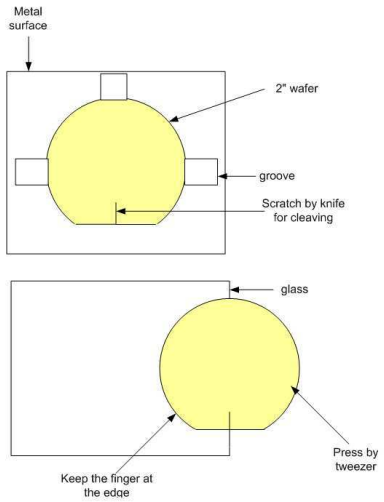


Figure E.5: *The procedure of cleaving.*

E.3.4 Working in HF Workbench

Never dispose used HF acid in the sink. Used HF should be kept in the big jar which is under the table. There are four different types of HF concentrations available in the workbench, e.g. 0.2%, 2%, 4% and 40%. There are three different types of big jars under the workbench for storing the used HF acid depending on its concentration, e.g. 2%, 4%, and 40%. For example, if we use HF acid with 0.2 % concentration then the jar with labellings "2%" can be taken for storing the used HF acid. At the same time, pour one beaker of water into that jar to make it neutralized. Put more water on that jar if the concentration is higher.

Keep in mind, HF acid can be directly poured into the big jar after our usage. But the

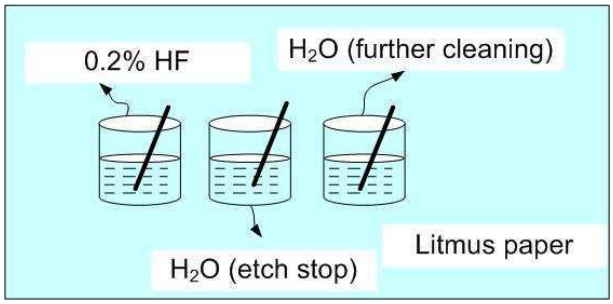


Figure E.6: *The way of keeping the beakers in HF workbench on the litmus paper.*

beaker we used for keeping this HF acid, that can not be cleaned directly. The water from another beaker should be poured into this acid beaker. Then this water mixed with acid should be put into the big jar. Then acid beaker can be cleaned. Cleaning is very important afterwards. While cleaning, keep the beaker under the water for a long time (e.g. 5 minutes) or fill with water and then put away, in this way 10 times (specially for acid). Lie down a litmus paper on a table and put the three beakers on it.
One of them is for HF acid.
One of them is water inside for stopping the etching.
The last one is also water but a larger beaker for further cleaning, if further acid or any undesired chemicals.

E.3.5 Preparing of the acidic solution

While preparing any type of acidic solution, one should always pour acid into water. Never pour water into acid which is explosive. For example, in preparing the acidic solution for wet chemical etching we should take water in a beaker at first and then H_2O_2 and then H_2SO_4 at the end should be poured into that beaker.

E.4 Plasmalab µEtch

This is the machine used to remove the resist residue that can not be removed after development. Just after the DEVELOPMENT of the photoresist (after heat treatment procedure so that the desired portion of the resist remain on the sample and undesired portion gets removed), we have to carry out this step, so-called **Photoresist Stripping** .

E.4.1 O_2 plasma

[13]Plasma ashing is an economical and efficient technique for removing photoresist from a wafer. A mechanical vacuum pump is used to reduce the pressure of the plasma chamber. A throttle valve between the pump and chamber allows for control of chamber pressure.

[13]http://fabweb.ece.uiuc.edu/lab/equipment/asher.aspx

Figure E.7: *The way of looking at the Plasmalab μEtch machine before starting the process to check that the machine is used by someone or not.*

Oxygen is injected at a controlled rate into the chamber. Molecular oxygen (O_2) does not react appreciably with photoresist at room temperature. It must be in a higher energy state in order for it to react. Oxygen radicals, such as O, must be created to initiate a low temperature reaction. A radio frequency (13.56MHz) oscillator connected in a capacitively coupled arrangement provides the energy to create the oxygen radicals (plasma). A small portion of the O_2 will dissociate to form monatomic O in the plasma (along with ionized species). The monatomic O reacts with the organic photoresist to form volatile (gaseous at low pressure) products such as CO, CO_2 and water. The reaction products are then pumped out of the chamber.

E.4.2 Operation

1) Check that if there is any sample inside the chamber or not. To understand, just take a look through a transparent place at the front of the machine which is shown in Fig. E.7. If there is a glowing (blue-white plasma), the device is under operation, i.e. sample is inside the chamber. So one has to wait until the running process finishes.
2) Once the device is ready for the new operation, Press **MANUAL+ VENT** to bring the machine into normal atmospheric pressure so that the chamber can be opened to load my sample. Because the machine should always be kept under vacuum condition.
3) After pressing **MANUAL+ VENT** the machine will come into normal atmospheric pressure after a while but still the door should not be opened until 20 sec elapses.
4) Open the chamber by two mechanical switches.
5) Load the wafer in the chamber.
6) Close the chamber by those two mechanical switches in another direction.
7) Press **MANUAL+ ROUGH** which will make the system to come under rough vacuum condition which is not sufficient for this process. Then system will go into automatically under high vacuum condition. **HI VAC** led will start to blink and wait until this blinking

gets stabilized.
8) Once the system is under high vacuum condition, then press **SET+GAS1** (in our case, O_2).
9) Press 100 (for 10%) and then press ENTER. This numerical percentage for the gas can be realized in this way that is how much valve opening will be activated for flowing the O_2 gas.
10) Press **MANUAL+GAS1** to activate the O_2 flow. The O_2 valve will open, allowing a controlled amount of O_2 (10%) into the system. and wait until the data (10%) given manually displays on the machine **DATA** .
11) Press **SET+RF LEVEL** to allow the RF power.
12) Press 333 (for 33% RF power) and then press enter.
13) Press **MANUAL+RF LEVEL** (to activate the RF power)
14) Ash the wafer for 2 minutes by adjusting the timer manually.
15) Once the specified time elapses, press instantaneously MANUAL+RF to deactivate the RF power.
16) Press **MANUAL+VENT** to take the sample out.
17) After a while, once the machine is in atmospheric pressure and then waiting for 20 secs more, press those two mechanical switches to open the chamber.
18) Unload the wafer.
19) Then the system should be brought back into high vacuum condition. For that Press **MANUAL+ROUGH** which will keep the system into high vacuum after switching from ROUGH to HIGH automatically.

E.5 Rapid Thermal Annealing (RTA):

E.5.1 What is Annealing

Annealing is a heat treatment process that alters the micro structure of a material causing changes in properties.

E.5.2 Why Annealing

In microfabrication procedure annealing plays a very important role for getting the desired properties of the device. To bring the good ohmic contact between metal-alloy and semiconductor, it is necessary to anneal the devices in the annealing machine for specific time at temperatures between 400^0 C and 425^0 C. This elevated temperature annealing accelerates the diffusion between multi-layer metal-alloys and lowers the ohmic contact resistance of the interface.

Figure E.8: *Rapid Thermal Annealing machine used for annealing.*

E.5.3 Basic Principle

[14]This system uses a high intensity visible radiation to heat a single wafer for short periods of between 1 to 300 seconds (for very short time) in a temperature range of 400 to 1150^0C. RTA system for processing semiconductor wafers by thermal annealing processes in an environment from ultra-high vacuum to ambient pressure with different atmospheres like oxygen and nitrogen.
The RTA System is used for rapid thermal annealing of wafers either in ultra-high vacuum (UHV) or other atmospheres like oxygen or nitrogen with a variable pressure range up to atmospheric pressure. The wafer is heated by an array of high-power quartz lamps. The complete system consists of two UHV chambers, the load-lock chamber and the process chamber. Both chambers are pumped by turbomolecular pumps and are equipped with a pressure measurement system that spans the range from 1000 mbar down to 10-9 mbar. With a magnetically coupled transfer system the wafer is transferred into the reaction chamber. Viewports allow the direct observation of the RTA process.
For our sample, we need the annealing only for n-contact. There is no need of the annealing process for p-contact due to higher doping concentration (1-2 order of magnitude).

E.5.4 Operation

The tray of the annealing machine where the sample will be loaded that has to be pulled out very carefully since there is very sensitive thermocouple (temperature sensor) inside.
1) Main menu by pressing **ESC** .
2) Press **2** for batch administration.
3) Press **6** for selecting the recipe group.
4) Type **CJ** and then press **ENTER** .
5) Press **5** to load recipe and then type **4** and then press **ENTER** .
6) Press **7** to start heat process. The temperature will reach at 400^0C in 90 sec and stay at this temperature for 5 sec and come into room temperature.

[14]http://specs.com/products/MBE/MBE-system/rta.htm

7) Press ESC to come into the main menu.
8) Press **1** for process overview.
9) Press **2** to see the temperature behaviour of the system graphically.
Procedure 7,8 and 9 should be done very quickly to check the system behaviour. If some unexpected behaviour is found then the system has to be stopped instantaneously by pressing **EMERGENCY STOP** (red button, at the middle of the machine).
Two temperature curves will be displayed in the graphical interface (monitor). One is RED which indicates the set temperature and the blue one which indicates the actual temperature.
The set curve (RED) will show the sharp fall-off from 400^0C though the system will take some time for cooling which can be realized from the actual curve (blue).
In the display there is a countdown process named **STEPTIME** will continue. Once it reaches **0** , the thermal procedure is over that can be realized.
Press **ESC** two times to come into the main menu then the tray can be pulled out either to put the sample or to take the sample out after heat treatment.
Open the door and load the sample and the same procedures mentioned above have to be maintained orderly.
10) Make the ventilation with N_2 and unload the wafer.

E.6 Oxidation

E.6.1 Basic Principle

This process is so-called, wet oxidation process. The basic chemical reaction takes place in this process:

$$AlAs + 6H_2O = Al_2O_3 + As_2O_3 + 3H_2O$$

[15] The wet oxidation of AlGaAs is a relatively simple procedure. Expose high Al-content layers to water vapor transported in an inert carrier gas within an elevated temperature (400^0 C) environment. However, establishing a stable and reproducible oxidation process is very necessary.
An oxidation system consists of mass flow controller for N_2 gas, a stable water vapor source and a three-zone 4 inch diameter tube furnace. The steam is supplied by bubbling N_2 through water which in turn is immersed within a constant temperature bath maintained at 96^o C. The gas passes through the bubbler and into a three zone furnace temperature enables a stable and reproducible oxidation process.
The oxidation applied in the device is lateral oxidation and the layers will be oxidized are buried, i.e. not at the top. For lateral oxidation process of buried layers, mesas are formed in the device to expose the layers by etching immediately before the oxidation,

[15] Optoelectronics Properties of Semiconductors and Superlattices, edited by Julian Cheng and Niloy K. Dutta,Gordon & Breach Science Publishers, 2000, Chapter-2, The Technology of Selectively Oxidized Vertical Cavity Lasers, Kent D. Choquette.

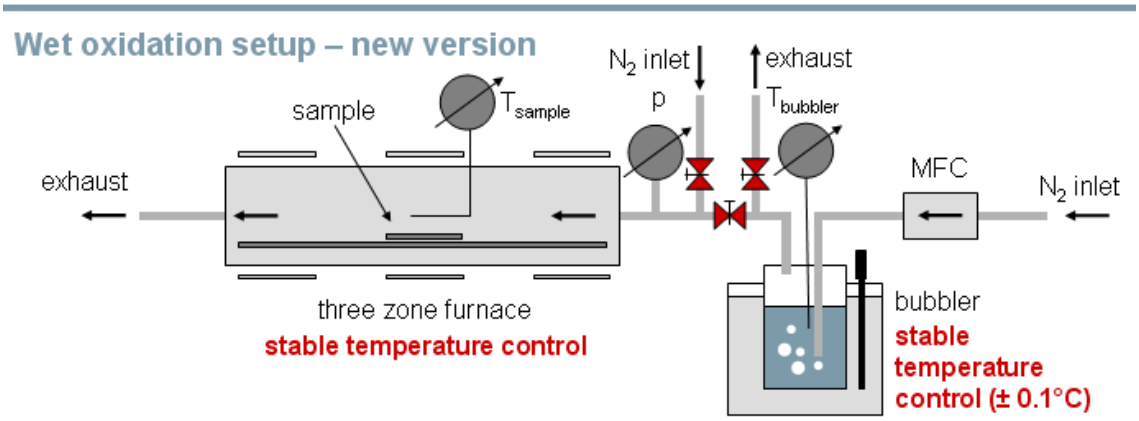


Figure E.9: *Schematics of the oxidation machine*
[p]

[p] Collected from: Basic Characterization of the New Oxidation System, Seminar of the Institute of Optoelectronics, 11.07.2007, Andrea Kroner.

although delays between etching and oxidation of AlGaAs do not significantly influence the oxidation rates.
The composition of the epitaxial layers varies such that one or more buried layers will oxidize laterally within the mesa to a greater extent than the surrounding layers. The oxidation extent is controlled by the time of oxidation.
The measurement of the oxidation extent and rate can be used to identify the oxide aperture within the VCSEL by using the special infra-red camera which makes the buried layers to be visible.

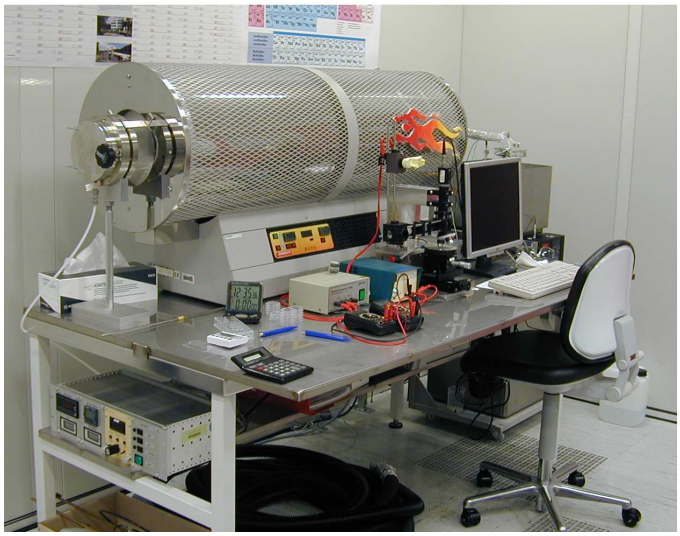


Figure E.10: *Full view of our oxidation machine*

E.6.2 Before the Oxidation

Before the oxidation the sample should be kept in Methanol until the oxidation starts. Note that Methanol evaporates very quickly. So it is highly recommended to cover the methanol solution along with the sample very well. The sample should be soaked in iso-propanol for 2 mins afterwards just before the oxidation process. Moreover, the sample should also be soaked in diluted HF acid (so-called HF dip) for 5 sec to remove the native oxides formed on the sample and which really helps to get the controllable and stable oxidation depth.

E.6.3 Oxidation Machine (Not Automatic, Manually Controlled)

- Before starting the oxidation process check the water level in the water bubbler. If the water level is too small, fill with water manually by using the funnel.

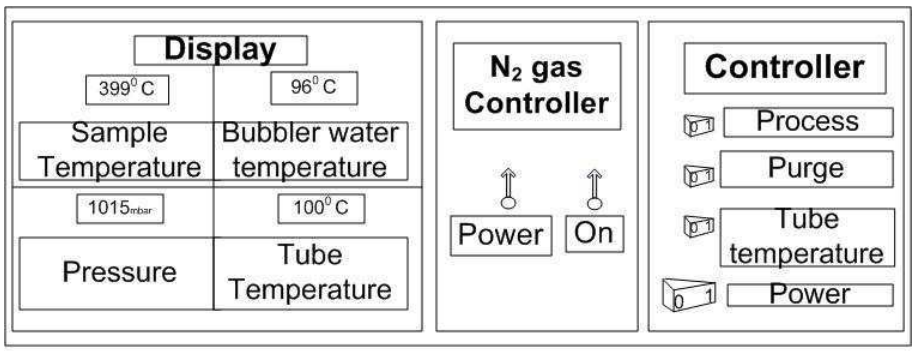


Figure E.11: *Schematics of the oxidation machine controller*

- Press **POWER** button of the controller block (shown in Fig. E.11) and **TUBE HEATER** for the tube (through which water vapor will go into the hot furnace) to be heated and wait till the temperature reaches at 80^0 C. It will take about 30 minutes. Once the tube heater will be turned on from the controller, the heating device located under the working table (shown in Fig. E.12) will get turned on automatically to heat the tube.

- The water bubbler (HUBER UNISTAT - shown in Fig. E.13) has to be turned on once the tube temperature reaches at 80^0 C. Press **POWER SUPPLY** and after a while (2 min) and I_ϑ in the bubbler for heating the water as soon as the tube temperature gets that temperature .This heating will be done by oil (not direct heating) to stabilize the temperature. The bubbler needs to be turned on after the tube heater due to avoid the water condensation in the tube.

- Now the rotating knob of the heating device has to be rotated little bit to be aligned with the two arrow marks in order to get higher heating (shown in Fig. E.12) i.e. when

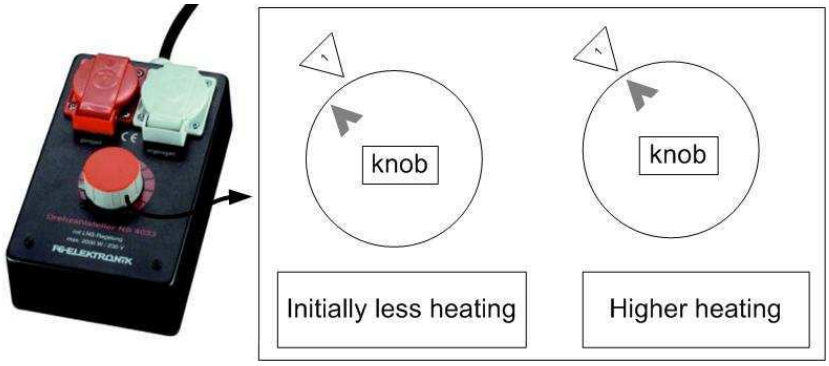


Figure E.12: *Heating device (at the left) and the required settings during the operation(at the right)*

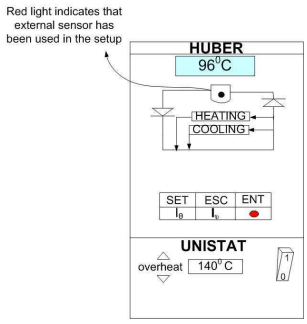
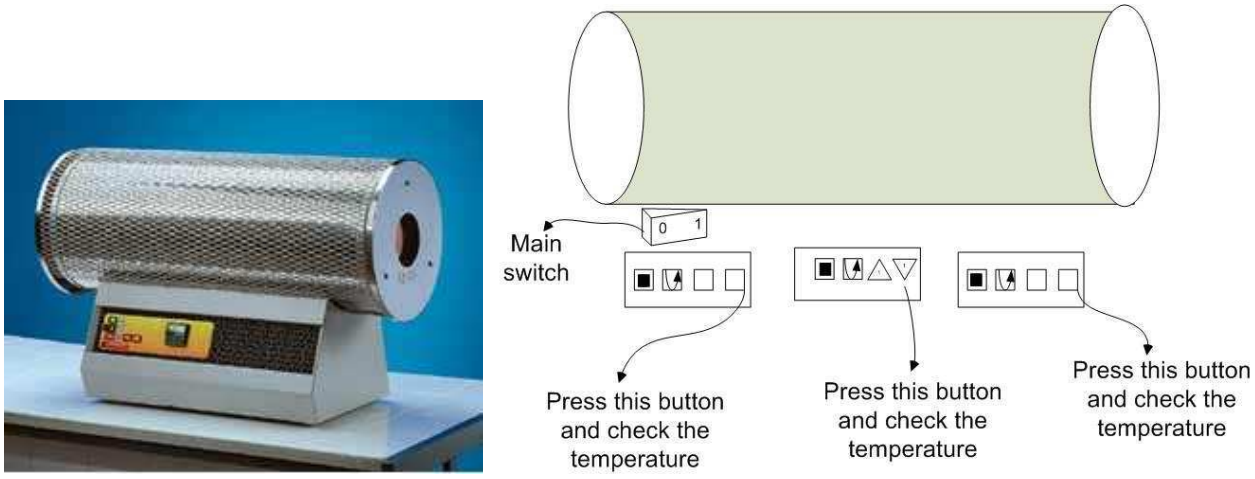


Figure E.13: *Schematics of the water bubbler.*

the bubbler will be turned on. Note that the bubbler water temperature can be viewed from the controller block display which is connected by a sensor.

- At the same time N_2 flow should be allowed to the water bubbler. For that, move the mechanical switch **POWER** and **ON** in the controller block. N_2 acts as carrier gas here, to guide the water flow through the chamber. In fact, N_2 (carrier gas) is bubbled through a hot water in this bubbler system.
- The CARBOLITE (discussed later) tube furnace also needs to be turned on now. Press the **POWER SUPPLY** button(shown in Fig. E.14) and check the existing temperature settings in three zones.
- There is a temperature display (green in color) in the bubbler . When the temperature here reaches at 80^0 C (after 30 minutes) press **PROCESS** (in the controller) to allow the flow N_2 and H_2O inside the furnace to stabilize the process before the temperature finally reaches at 96^o C.After approximately 30 minutes the temperature will reach at 96^o C.
- To get the completely stable system about one and half hour will be needed.
- In the bubbler block just under the temperature display (shown in Fig. E.13) the illumination of red led indicates that External temperature sensor has been used in the setup.



(a) *Three zone tube furnace.* (b) *Different zone of tube furnace.*

Figure E.14: *Three zone tube furnace (at the left) and the illustration showing the required temperature settings for the operation(at the right).*

- After reaching the water temperature into 98^0 C, the temperature will automatically start to go down at the time of stabilization. This rising and falling of temperature can be realized from the display of the bubbler block illustrated in Fig. E.13, i.e. the two paths of the circuit will start to fluctuate, the upper led turn on indicates that heating and vice versa.

- There is a green display in the bubbler block which will show the maximum temperature (96^o C) of water.

- When the temperature of the bubbler block will be at sharp 96^o C, i.e. stabilization, then we can start our work. Then sample can be put inside the hot furnace for oxidation.

- The sample has to be taken out depending on the data of the oxidation rate and the lateral oxidation length obtained from dummy sample.

- To measure the oxidation depth and rate, camera interfaced with the computer (**Software:MB-ruler40,** this number 40 depends on the magnification of the objective lens used in the microscope, another two lens' magnification is 16 and 80) is used. Though the oxidation is taking place under some layers, but the camera is infra-red camera which has the ability of showing the display of some bottom layers.
  N.B. Turn on the CPU of the computer and plug-in the power cord of the camera.**Software : WinTV32** has to be selected. For measurement of the lateral oxdation length three different programs depending on the lens' magnification will be used.

- Under camera,

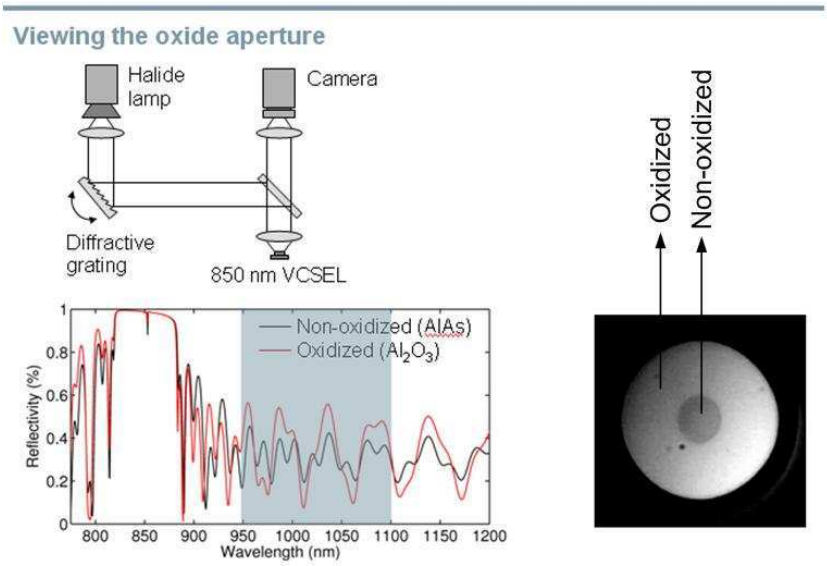


Figure E.15: *Camera setup used in our oxidation machine to view the oxide aperture.* [q]

[q] Collected from: Basic Characterization of the New Oxidation System, Seminar of the Institute of Optoelectronics, 11.07.2007, Andrea Kroner.

Oxidized area → white
Non-oxidized area → dark.

- After oxidation, take the sample out and press PURGE, allows to exhaust all the undesired materials from the chamber. At that time process must be turned off.
- And then, turn off all switches one by one. At last, the power cord of the camera has to be plugged out.

E.6.4 CARBOLITE - Three Zone Tube Furnace

This model utilize three resistance wire heating elements for heating the tube furnace where a tube with one crucible is located.

E.6.5 Some Important Steps

1. At the beginning when the tube will start to be heated to reach into 80^0 C (e.g. when the temperature is 75^0 C), press PURGE for 15 sec to remove any undesired gases from the furnace.
2. The display of the bubbler water temperature in controller block and in bubbler block should be same which is a symptom of stabilization.

Figure E.16: *Different parts of oxidation machine.*

3. The display of the sample temperature in display block and in hot furnace block will not be same until the system becomes stable.

4. When the bubbler water temperature is around $80^0/82^0$ C then press PROCESS allows N_2 and water vapor to go inside the hot furnace in order to stabilize the system. Since the sample has not been kept yet inside the furnace, nothing will take place.

5. The bubbler water temperature will start to increase to reach into 96^0 C after turning on the bubbler block. But while increasing the water temperature might reach into 98^0 C and again it will go down and after a while it will be 96^0 C once the system is stable.

6. While putting the sample inside and taking the sample out we should stop the flow of N_2 and water vapor. So turn off the switch by pressing PROCESS. It is also important that we also have to put the sample inside very fast in order to avoid system instability problem.

7. Finally when the sample is taken out and no need of further oxidation in the device then press PURGE for 15 sec and then turn off all the switches one by one, e.g. TUBE HEATER, POWER button of the controller, two knobs' position, main switch of furnace, main switch of bubbler block, heating button.

E.6.6 Main Problem

In this system, the main problem is that no further oxidation is possible by inserting the sample into the hot furnace once the sample is already taken out from the hot furnace, even though the active diameter does not satisfy our requirements.

E.7 Tencor alpha-step 200:

E.7.1 General Description :

The profilometer measures the vertical depth of a material across a specified horizontal length. The profile is displayed on a printable graphical interface. Uses for this equipment include measuring etch depth, deposited film thickness, and surface roughness.

E.7.2 Equipment Specifications :

1. Vertical ranges of: 1000 Å, 2500 Å, 5000 Å, 10 kÅ, 25 kÅ, 50 kÅ, 100 kÅ, 250 kÅ, 500 kÅ and 1000 kÅ.
2. Leveling (Auto, Manual).
3. Scan Length: 3 mm (Manual mode), 2.5 mm (Automatic).
4. Resolution: 50 Å.

E.7.3 Operating Instructions :

Cautionary notes: Always lower the stage before loading and unloading samples. Do not move the stage when the stylus is in proximity contact with the upper part of the device.
Start-up Procedures:
1. Rotate the BRIGHTNESS and CONTRAST knob until the display looks good.
2. To load the sample, lower the stage and move it out from under the stylus. Do this by pressing the ”TABLE” down arrow and then turning stage knob.
3. Place the sample on the stage.
4. Move the loaded stage under the stylus.
5. To view the sample through the graphical interface, press the ”TABLE” up arrow. Continue raising the stage until the sample is in focus.

6. Orient the stage using the stage knobs until the target feature is under the stylus. (The stylus can be seen as a black pointed object on the top of the screen.)
7. Press the ”TABLE” up arrow button until the stylus makes contact with the sample and then backs off.
8. Press the ”START/STOP” button.

E.7.4 Changing the Horizontal Scan Range:

1. Press ”ENT”.
2. Select from the range choices displayed on the screen by pressing the ”RANGE” up and down arrows.
3. Press ”ENT” again to exit.

Figure E.17: *Tencor Alphastep 200 used to measure the etch depth.*

E.7.5 Changing the Displayed Vertical Depth :

1. Press the ”RANGE” up and down arrows and select from the choices of displayed depths.
2. Press ”PLOT” to make the changes.

E.7.6 Zooming

1. To zoom into a specific section of the plotted profile, move the left and right cursors around the desired section. Do this by pressing the ”CURSOR” left and right arrows.
2. Press ”PLOT”.
3. To zoom back out press the ”PLOT” button again.

E.7.7 Manually Level the Profile

1. Press ”LEVEL”.
2. Move the left and right cursors around a portion of the slanted line you know to be level. Do this by pressing the ”CURSOR” left and right arrows.
3. Press ”PLOT”

E.7.8 Printing the Profile:

1. Press the ”PRINT” button.

E.7.9 Shut-down Procedures

1. Lower the stage and move it out from under the stylus by pressing the "TABLE" down arrow and then turning the stage knobs.
2. Remove the sample.
3. Rotate the BRIGHTNESS and CONTRAST button as it was before.

E.8 Scanning Electron Microscope:

E.8.1 Operating Principles:

- Press Vent (wait 6 minutes to open the chamber).
- Meanwhile turn on the monitor.
- Switch on the four buttons at the right panel (Camera, Signal Mixer, SE, Scan Rotation)
- Turn on the brightness button and keep it high.
- After checking the vacuum condition, open the chamber and take a holder to put the sample on.
- Tighten the holder screw along with the sample.
- Close the chamber.
- The facet we want to investigate should be on our right side while placing the holder inside the chamber.
- There should have some distance (e.g. 3 mm) between the anode and cathode which is visible in the monitor.
- It is always recommended to go down with the holder knob before closing the chamber.
- Press EVAC (for high vacuum) and wait for 6 minutes until the red LED becomes green.
- Two buttons (green led) without labeling at the front panel. Starting the electron beam by switching ON (Red).
- Press TV button (TV gliding average 7 or 8).
- Change to lower magnification to see the structure initially.
- Focus knob.

- Scanning mode (STIGMATOR) to sharpen the picture, i.e. to have a good quality picture.
- Image shift, i.e. view angle.
- TV integration.
- To rotate the sample, Press $\wedge$ or $\vee$ on the right panel.
- To save the picture, press ESC → Memory → ENTER → data → Y → save → enter
- For new picture, press TV.
- Fine tuning ↑↓ - angle display (at the right panels)
- Logout and note all the necessary information.
- Turn off e-beam by switching 'off'(green) button.
- Move the sample down little bit.
- Press VENT and wait for 5 minutes.
- Remove the sample.
- Press EVACUATE again.
- Magnification 10,000 should be brought back.
- Switch off the four buttons at the right panel.
- Brightness should be in lowest position.

E.8.2 Some Important Notes

- The sample examined in SEM should contain conductive material, e.g. metal layer in order to have a good visible picture because the conductive materials will not be charged up very easily with time due to continuous energetic electron bombardment on the sample. On the contrary, the material which is not conductive will be charged up with time resulting lack of contrast in the picture. So it is always a good idea to metallize the sample before examining the sample in the SEM machine.
- There are some buttons red marked should not be touched at all.
- There are two options for choosing the detector, they are, SE (Secondary Electrons) and SEINLES (Back Scattering Electrons). Normally we work in SE mode from we get the whole information about different regions of the sample. By backscattering electron mode we will not get the topographic (surface) information of the sample.

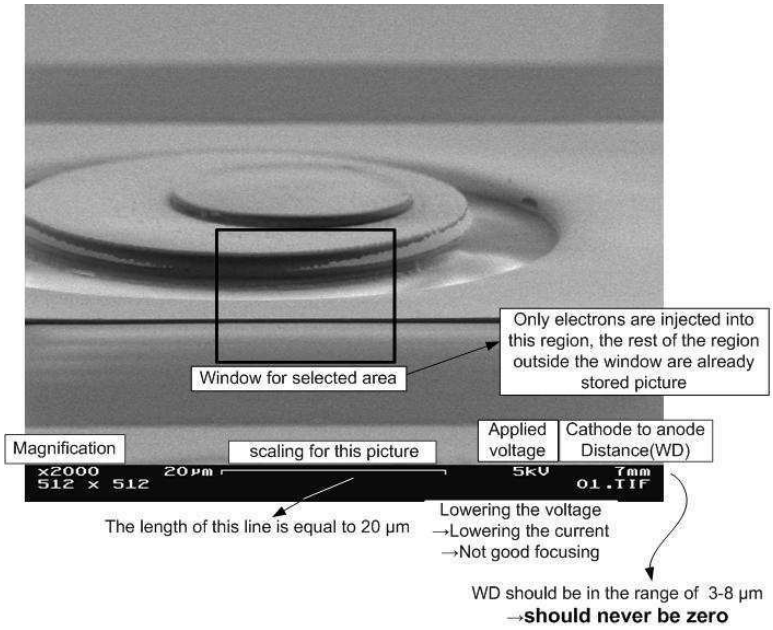


Figure E.18: *Analyzing a sample under SEM*

- Picture at the edges is little bit brighter (does not have good contrast) since electrons hit at the edges and just leave that region without being detected by the detector.
- This machine basically produces images by detecting low energy secondary electrons which are emitted from the sample's surface due to excitation of the primary beam. The e-beam is rastered across the sample, with the detectors building up an image by mapping the detected signal with beam position.

E.9 Opto Annealer

E.9.1 Starting

- Make sure that NOT-AUS (Emergency Stop) has not been pushed and PUMP POWER, EVAC, NO PUSH, Ar, N_2, O_2 are switched off and mode is switched to Automatic.
- Switch on Main Power then the monitor.
- Wait until the process controller has completed booting, then set it to graphic display by pushing its left most key twice.
- Switch on PUMP Power (never switch it on before the process controller is ready).
- Log into computer or Press ESC.
- Start the IPSG software.

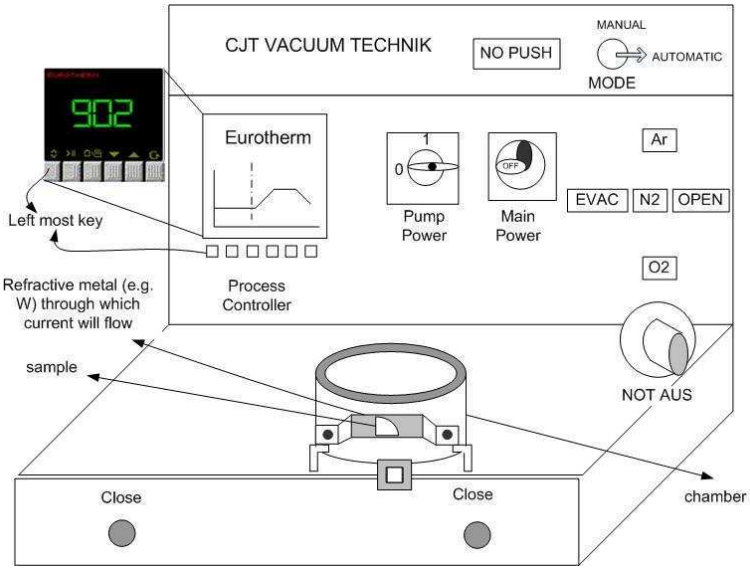


Figure E.19: *Schematics of Opto Annealer.*

- Manually retract any stuck locking clamps and open chamber.

E.9.2 Process

- Place the sample at the center of the heater.
- Close the chamber then press both CLOSE buttons simultaneously.
- Load personal set of programs, SCREENS → Program Edit→ Load from disk.
- Select one of the 20 programs in the set, Program→POLY3 (in my case).
- Check or modify selected program, temperature, gases and evacuate.
- Save the complete case to your personal file, File→Save.
- Load the current program into a program slot of the process controller, Program→ Download this program. Use the same program slot number in the process controller as in your program set to avoid confusion.
- Select to use the program just transferred, program→Load/load to loop.
- Switch to chart, Screens→Trend chart.
- Scale Y-axis according to the maximum temperature in your program, Scale→ Y axis.
- Run the program. For that double click the Prog. Status→Reset→Run.
- Wait until program is finished. Run automatically changes to Reset again.
- Wait until process variable has dropped below 50_0C.

- Press Open to retract locking clamps, help the stuck ones manually and then open the chamber, remove the sample from the heater.

E.9.3 Shutdown

- Close chamber, do not lock it (it would unlock anyway).
- Exit from IPSG software. File→Exit.
- Shut down the computer. Wait until shut down is complete.
- Switch off pump power and then main power.[18]

E.9.4 Some Important Notes

- There are three different heating elements are available, two of them are for heating the sample in N_2 atmosphere and one of them (brighter one) is in O_2 atmosphere.
- The heating process will take place inside the chamber by resistive heating or so-called ohmic heating. The heat produced is proportional to the electrical resistance of the heating element multiplied by the square of the current. The wider heating element will give the lower resistance resulting lower ramp and lower temperature.
- While selecting, Program→ Download this program, always choose : ”1” and then program→Load/load to loop, this time choose: ”Program 1”.

E.10 Summary

In this appendix, the operating instructions of almost all of the machines (except metal evaporation machines) required for fabricating the VCSEL are discussed with some figures which might be quite helpful for the beginners to start their work in the cleanroom.

[18] The statements in Starting, Process and Shut down subsections are official instructions.

Appendix F

Process Overview

F.1 Processing steps

F.1.1 Cleaning

- Rinsing in acetone for 5 minutes to remove any contaminants, particles and organics.
- Rinsing in Isopropanol (propanol-2) for 5 minutes which dissolves acetone residue.
- Blow dry with N_2 to remove water.
- Drying in hotplate at 120^0 C for 10 minutes to remove water residues.

F.1.2 Mesa Positioning

- Spin coating: Resist: AZ1512HS, 6000 rpm, Program 6, 40 seconds.
- Cleaning the edge of the wafer using edge bead remover.
- Softbaking in hotplate at 90^0 C for 10 minutes to make the resist photosensitive.
- Cleaning the backside of the wafer using cotton buds and acetone.
- Optical exposure at 12 mW/cm^2, 16 seconds, mask : "MESA POS".
- Developing: AZ400K : H_2O = 1:4, 18 seconds.
- Hardbaking in hotplate at 120^0 C for 2 minutes to make the resist very stable against etchant.
- O_2 plasma for 2 minutes, 10% O_2, 33.3% RF(100W) to remove the residual resist.

F.1.3 Wet Etching for Mesa

- Wet chemical etching, Etchant:- $H_2SO_4 : H_2O_2 : H_2O = 1 : 6 : 40$ for 6 minutes 45 seconds. N.B. Total thickness till n^+ buffer layer = 8.5 μm. While etching, the sample will be completely dark due to AlAs layer after 2 minutes 42 seconds.
- Checking the etch depth in alpha-step profilometer and optical microscope.
- Resist removal by Methyl-Pyrrolidone (MP) at 90^0 C for 10 minutes.

F.1.4 Oxidation

- Cleaving the sample to prepare a dummy.
- Measuring the diameter of AlAs layer in infra-red camera to observe the undercut.
- Keep the sample in the beaker with methanol at 20^0 C until the oxidation machine ready to prevent the oxidation.
- Rinse in IPA which dissolves methanol residue for 2 minutes.
- HF-Dip (0.1%) for 5 seconds to remove the native oxides from the surface.
- Stopping the etching by immersing the sample quickly in H_2O for 15 seconds.
- Dummy sample in the furnace for oxidation at 382^0 C for 13 minutes.
- Calculation of oxidation rate and depth.
- Hot sample in the furnace for oxidation at 382^0 C for 13 minutes 30 seconds.

N.B. The operating procedures of oxidation machine are given in Appendix E.

F.1.5 Column Isolation Etching

- Cleaning (see §F.1.1)
- Spin coating: AZnLOF 2070, 4000 rpm, 40 seconds, Program 4.
- Cleaning the edge of the wafer by edge bead remover.
- Softbake: Hotplate, 110^0 C, 2 minutes.
- Resist removal from the backside of the sample by acetone.
- Exposure: 12 mW/cm^2, 8 seconds, mask : "COLUMN ISOL".
- Post-exposure Bake: Hotplate, 110^0 C, 90 seconds.
- Development: AZ826MIF, 110-115 seconds.

- O_2-plasma: 2 minutes 30 seconds, 10% O_2, 0.1 Torr, 33.3% RF (100W).
- Hardbake: Hotplate, 110^0 C, 1 minute.
- Wet chemical etching, Etchant :- $H_2SO_4 : H_2O_2 : H_2O = 1 : 6 : 40$ for 3 minutes 40 seconds. N.B. The etching rate of GaAs is slower, experimentally found 0.78-0.80 μm/min.
- Checking the etch depth in alpha-step profilometer and optical microscope.
- Resist removal by Methyl-Pyrrolidone (MP) at 90^0 C for 25 minutes.

F.1.6 N-Contact

- Cleaning (see §F.1.1)
- Spin coating: AZnLOF 2070, 4000 rpm, 40 seconds, Program 4.
- Cleaning the edge of the wafer by edge bead remover.
- Softbake: Hotplate, 110^0 C, 2 minutes.
- Resist removal from the backside of the sample by acetone.
- Exposure: 12 mW/cm^2, 8 seconds, mask : "N CONTACT"
- Post-exposure Bake: Hotplate, 110^0 C, 90 seconds.
- Development: AZ826MIF, 110-115 sec.
  N.B. If DIAGONAL PROBLEM arises during the alignment in this mask, move one block horizontally and if HORIZONTAL PROBLEM, move one block vertically.
- Control in the Microscope.
- O_2-plasma: 2 minutes, 10% O_2, 0.1 Torr, 33.3% RF (100W).
- HCl-Dip: HCl : H_2O = 1:1; 30 seconds to remove oxides.
- Stopping the reaction by immersing the sample in H_2O for 15 seconds.
- Loading the sample inside the metallization chamber for 6 hours.
- Evaporate: Ge(17 nm)-Au(50 nm)- Ni(10 nm)- Au(50 nm).
- Lift-off: MP (warm)→ Acetone → Isopropanol.
- Annealing: 10 seconds, 400^0 C, Program CJ4.

N.B. The operating procedures of annealing machine are given in Appendix E.

F.1.7 Polyimide Passivation-1

- Taking the polyimide out from the refrigerator 2 hour earlier before the usage due to avoid the moisture-picking problem.
- Cleaning (see §F.1.1).
- Spin coating: Durimide 7505, 3000 rpm, 40 seconds, Program 3.
- Softbake: Hotplate, 100^0 C, 3 minutes.
- Exposure: 12 mW/cm^2, 16 sec, mask: "POLYIMIDE-1".
- Immediately after exposure, postbake for 1 minute @ 100^0 C.
- 12-14 minutes delay.
- Developing with Clariant HTRD2 for 90 seconds.
- Stopping the development reaction by immersing the wafer in isopropanol for 1 minute.
- Heating the sample in the annealing machine, OPTO ANNEALER in a heat ramp from 100^0 C to 300^0 C using the program "POLY-3".

N.B. The operating procedures of annealing machine (OPTO ANNEALER) are given in Appendix E.

F.1.8 Polyimide Passivation-2

- Taking the polyimide out from the refrigerator 2 hour earlier before the usage due to avoid the moisture-picking problem.
- Cleaning see §F.1.1
- Spin coating: Durimide 7505, 4000 rpm, 40 seconds, Program 4.
- 3 min delay to let the polyimide diffuse into AlAs layer.
- Softbake: Hotplate, 100^0 C, 3 minutes.
- Exposure: 12 mW/cm^2, 16 seconds, mask : "POLYIMIDE-2".
- Immediately after exposure, postbake for 1 minute @ 100^0 C.
- 12-14 minutes delay.
- Developing with Clariant HTRD2 for 90 seconds.

- Stopping the development reaction by immersing the wafer in isopropanol for 1 minute.
- O_2-plasma: 3 minutes, 10% O_2, 0.1 Torr, 33% RF (100W).
- Heating the sample in the annealing machine, OPTO ANNEALER in a heat ramp from 100^0 C to 300^0 C using the program "POLY-3".

F.1.9 Polyimide Passivation-3

Repeat the entire processing steps mentioned in §F.1.8 and use the same mask: "POLYIMIDE-2".

F.1.10 P-Contact Bondpad

- Cleaning (see §F.1.1).
- Spin coating: AZnLOF 2070, 4000 rpm, 40 seconds, Program 4.
- Softbake: Hotplate, 110^0 C, 2 minutes.
- Exposure: 12 mW/cm^2, 8 seconds, MASK : "P CONT BOND".
- Post exposure bake: Hotplate, 110^0 C , 90 seconds.
- Developing: AZ 826 MIF, 105-115 seconds.
- Control in the Microscope.
- O_2-plasma: 2 minutes, 10% O_2, 0.1 Torr, 33% RF (100W).
- HCl-Dip: HCl : H_2O = 1:1; 30 seconds to remove oxides.
- Stopping the reaction by immersing the sample in H_2O for 15 seconds.
- Loading the sample inside the metallization chamber for 6 hours.
- Evaporate: Ti(20 nm)-Pt(50 nm)-Au(150 nm).
- Lift-off: MP(90^0 C) → Acetone→Isopropanol.
- Hard spraying with MP if metal does not lift-off easily.

Appendix G

Epitaxial Structures

This appendix provides brief layer structures summaries of the sample of which the measurements are presented in the thesis. Layers are specified with the thickness, material composition, absorption and doping concentration along with their functions within the device. In the next page, this is attached in a tabular format:

M06_16
Standard 850 nm top-emitter, 23/38.5 mirror pairs

No. Of pairs	layer thickness (nm)	Material	Al composition	Optical Absorption(cm^{-1})	Doping concentration(cm^{-3})
1x					
	2000	GaAs		9355.13	1.7e18
	49.10	AlGaAs	0.20	4.09 to 5.80	1.4e18 to 2.5e18
38x					
	12.37	AlGaAs	0.27 to 0.47	4.68 to 4.51	2.3e18 to 2.7e18
	19.19	AlGaAs	0.47 to 0.90	4.51 to 4.88	2.7e18 to 3.1e18
	29.67	AlGaAs	0.90	4.88 to 3.58	3.1e18 to 1.7e18
	19.19	AlGaAs	0.90 to 0.47	3.58 to 3.38	1.7e18 to 1.5e18
	12.37	AlGaAs	0.47 to 0.27	3.38 to 3.47	1.5e18 to 1.3e18
	36.82	AlGaAs	0.20	4.09 to 5.80	1.4e18 to 2.5e18
1x					
	12.37	AlGaAs	0.27 to 0.47	4.68 to 4.51	2.3e18 to 2.7e18
	19.19	AlGaAs	0.47 to 0.90	4.51 to 4.88	2.7e18 to 3.1e18
	29.67	AlGaAs	0.90	4.88	3.1e18
	19.19	AlGaAs	0.90 to 0.47	4.88 to 3.24	3.1e18 to 1.3e18
	12.51	AlGaAs	0.47	3.24 to 2.30	1.3e18 to 3.1e17
	44.28	AlGaAs	0.47	2.30 to 2.10	3.1e17 to 1.1e17
	36.45	AlGaAs	0.47 to 0.27	0.00	
	9.95	AlGaAs	0.27	0.00	
2x					
	7.92	GaAs		-1.0 active	
	9.95	AlGaAs	0.27	0.00	
1x					
	7.92	GaAs		-1.0 active	
	9.95	AlGaAs	0.27	0.00	
	37.12	AlGaAs	0.27 to 0.47	0.00	
	25.83	AlGaAs	0.47	2.16 to 6.59	3.9e16 to 1.2e18
	61.50	AlGaAs	0.47	6.59 to 8.94	1.2e18 to 1.8e18
	19.19	AlGaAs	0.47 to 0.90	8.94 to 15.37	1.8e18 to 1.1e19
	31.98	AlAs		12.37	1.2e19
	19.19	AlGaAs	0.90 to 0.47	15.37 to 8.94	1.1e19 to 1.8e18
	30.96	AlGaAs	0.47	8.94	1.8e18
	19.19	AlGaAs	0.47 to 0.90	8.94 to 4.40	1.8e18 to 2e18
	29.67	AlGaAs	0.90	4.40 to 5.59	2e18 to 3e18
	19.19	AlGaAs	0.90 to 0.47	5.59 to 12.37	3e18 to 2.6e18
	12.37	AlGaAs	0.47 to 0.27	8.94 to 10.40	1.8e18 to 1.5e18
23x					
	36.82	AlGaAs	0.20	12.09	1.7e18
	12.37	AlGaAs	0.27 to 0.47	10.40 to 8.94	1.5e18 to 1.8e18
	19.19	AlGaAs	0.47 to 0.90	8.94 to 4.65	1.8e18 to 2.2e18
	29.67	AlGaAs	0.90	4.65 to 5.59	2.2e18 to 3e18
	19.19	AlGaAs	0.90 to 0.47	5.59 to 17.85	3e18 to 4e18
	12.37	AlGaAs	0.47 to 0.27	17.85 to 10.40	4e18 to 1.5e18
1x					
	9.69	AlGaAs	0.20	12.09 to 25.60	1.7e18 to 3.9e18
	8.44	GaAs		9384.06	4.9e18
	29.04	GaAs		9935.89 to 10485.23	8.4e19 to 1.6e20

Bibliography

[1] G.M. Yang, M.H. MacDougal, and P.D. Dapkus: "Ultralow threshold current vertical-cavity surface-emitting lasers obtained with selective oxidation", *Electronics Letters*, Vol. 31, pp. 886-888, 1995.

[2] K.D. Choquette, R.P. Schneider Jr., K.L. Lear, and K.M. Geib: "Low threshold voltage verical-cavity surface-emitting lasers by selective oxidation'", *Electronics Letters*, Vol. 30, pp. 2043-2044, 1995.

[3] Jack L. Jewell, N. A. Olsson, Axel Scherer, Samuel L. McCall, James P. Harbison, Leigh T. Florez, Yong H. Lee: "Surface-emitting microlasers for photonic switching and interchip connections", *Optical Engineering*, Vol. 29, pp. 210-214, 1990.

[4] K.L. Lear, K.D. Choquette, R.P. Schneider, Jr., S.P. Kilocoyne and K.M. Geib: "Selectively oxidized vertical-cavity surface emitting lasers with 50% power conversion efficiency", *Electronics Letters*, Vol. 31, pp. 208-209, 2nd February, 1995.

[5] Christopher L. Chua, David K. Fork, and Thomas Hantschel: "Densely packed optoelectronic interconnect Using micromachined springs", *IEEE Photonics Technology Letters*, Vol. 14, pp. 846-848, 2002.

[6] E. G. Paek, J. R. Wullert, M. Jain, A. Von Lehmen, A. Scherer, J. Harbison, L. T. Florez, H. J. Yoo, R. Martin, J. L. Jewell, and Y. H. Lee: "Compact and ultrafast holographic memory using a surface-emitting microlaser diode array," *Optics Letters*, Vol. 15, pp. 341-343, 1990.

[7] R.H. Webb, and F. Rogomentich : "Microlaser microscope", *Lasers and Electro-Optics Society Annual Meeting, 1994. LEOS '94 Conference Proceedings, IEEE*, Vol. 2, pp. 303-304, 1994.

[8] A. Kroner, F. Rinaldi, I. Kardosh, and R. Michalzik: "Towards ultra-compact optical tweezers without external optics", *Lasers and Electro-Optics Europe*, pp. 633 - 633, 2005.

[9] Yusuke Ogura, Kosuke Watanabe, and Jun Tanida: "Parallel translation of microscopic objects in three-dimensional traps by sequential change of emitting vertical-

cavity surface-emitting lasers", *Japanese Journal of Applied Physics*, Vol. 45, pp. 2603-2605, 2006.

[10] M. Orenstein, A.C. Von Lehmen, C. Chang-Hasnain, N.G. Stoffel, J.P. Harbison, and L.T. Florez: "Matrix addressable vertical cavity surface emitting laser array", *Electronics Letters*, Vol. 27, pp. 437-438, 1991.

[11] R.A. Morgan, G.D. Guth, C. Zimmer , R.E. Leibenguth, M.W. Focht, J.M. Freund, K.G. Glogovky, T. Mullally, F.F. Judd, M.T. Asom: "Two-dimensional matrix addressed vertical cavity top-surface emitting laser array display", *IEEE Photonics Technology Letters*, Vol. 6, pp. 913-917, 1994.

[12] K.M. Geib, K.D. Choquette, D.K. Serkland, A.A. Allerman, T.W. Hargett: "Fabrication and performance of two-dimensional matrix addressable arrays of integrated vertical-cavity lasers and resonant cavity photodetectors", *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 8, pp. 943 - 947, 2002.

[13] A.C. Von Lehmen, C. Chang-Hasnain, N.G. Stoffel, J.P. Harbison, L.T. Florez, L. Carrion and J. Wullert: "Independently addressable InGaAs/GaAs vertical-cavity surface-emitting laser arrays", *Electronics Letters*, Vol. 27, pp. 583-586, 1991.

[14] Giorgio Giaretta, M.Y. Li, Gabriel S. Li, Wupen Yuen and Constance J. Chang-Hasnain: "A Novel 4x8 Single-Mode Independently Addressable Oxide-Isolated VCSEL Array", *IEEE Photonics Technology Letters*, Vol. 9, pp. 1196-1198, 1997.

[15] Hendrik Roscher: "Flip-Chip Integration of 2-D 850 nm Backside Emitting Vertical Cavity Laser Diode Arrays", *Annual Report 2002*, Optoelectronics Department, University of Ulm, Germany.

[16] Carl W. Wilmsen; Henrik Temkin and Larry A. Coldren: "Vertical-Cavity Surface-Emitting Lasers", Cambridge Studies in Modern Optics, Cambridge University Press, Cambridge, Published 1999.

[17] M. J. Howes and D. V. Morgan, Editors: "Gallium Arsenide Materials, Devices, and Circuits", *John Wiley & Sons, Inc.*, pp. 123-132, New York (1985).

[18] S. Kicin, V. Cambel, M. Kuliffayova , D. Gregusova, E. Kovacova, and J. Novak: "Fabrication of GaAs symmetric pyramidal mesas prepared by wet chemical etching using AlAs interlayer", *Journal of Applied Physics*, Vol. 91, pp. 878-880, 2002.

[19] Kent D. Choquette: "The Technology of Selectively Oxidized Vertical Cavity Lasers", Chapter-2, Optoelectronics Properties of Semiconductors and Superlattices, edited by Julian Cheng and Niloy K. Dutta,Gordon & Breach Science Publishers, 2000.

[20] I. Hallakoun, T. Boterashvili, G. Bunin, and Y. Shapira: "Electrochemical etching impact on GaAs process, mask design and device performance", *GaAs Mantech*, pp. 25-27, 2000.

[21] M. Hagio: "Electrode reaction of GaAs metal semiconductor field-effect transistors in deionized water", *J. Electrochem. Soc.*, Vol. 140, pp. 402-2405, 1993.

[22] Y. Zhao, Y. Tkachenko and D. Bartle: "Suppression of electrochemical etching in GaAs pHEMTs", *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, pp. 163 - 166, 1999.

[23] Sammy Kayali: "Reliability of compound semiconductor devices for space applications", *Microelectronics Reliability*, Vol. 39, pp. 1723-1736, 1999.

[24] James Eun, and James A. Cooper Jr.: "High Temperature Ohmic Contact Technology to n-Type GaAs", *a Final Technical Report*, Purdue University, January, 1993.