ECE 154A
Introduction to Computer Architecture
Class Logistics
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**Office Hours:** Tu Th 3:30 pm – 4:30 pm, HFH 5153

**Course load and grading:**
- ~4-6 labs (30%)  Assembly (SPIM), SystemVerilog (Modelsim), and C
- ~6 HWs (20%)  5 - 10 problems each
- 2 Midterms (20%)
- Final (30 %)
- up to 5 % extra for participation and attendance

**TAs:**
- **Mohammad Bavandpour** (Rec: F 9:00 am – 9:50 am, Phelps 3519, Office hours: MW 8:00 am – 9:00 am, TA Trailer)
- **Amirali Ghofrani** (Rec: F 10:00 am – 10:50 am, Phelps 1508, Office hours: TBA)
- **Itir Akgun** (Rec: F 11:00 am – 11:50 am, Phelps 3523, Office hours: MW 9:00 am – 10:00 am, TA Trailer)

**Website:** [http://www.ece.ucsb.edu/~strukov/ecea154aFall2015/home](http://www.ece.ucsb.edu/~strukov/ecea154aFall2015/home)
Prerequisites

• Digital logic (ECE 15A, 152A)
  – Number representation (conversion, 2’s complement)
  – Combinational logic (K-maps, Boolean algebra, logic gates, muxes, decoders, critical path)
  – Sequential logic (clock cycle time, finite state machine, flip-flops and latches)

• Basic programming skills (CMPSC 16, 24, 32)
  – C language basics
  – Procedures, pointers and arrays

• Basic knowledge of hardware description language (ECE 152A)
  – will learn more in parallel in ECE 156A
Assignment

• Reading
  – Due this class:
    • Chapters 1-3 for prerequisite material
    • Sections 5.1-5.2.7
  – Due next class
    • Section 5.3
    • Optional reading: pages 242-258 from P&H

• Homework #1
  – Will be posted this week
  – Tentatively due Oct. 6th

• Lab #1
  – Will be posted next week