ECE202A first problem set. Due October 18, 1999 (in class)

1) Practice with a Smith Chart:
   a) What are  \( Z_l, Y_l, \Gamma \)?

   ![Image](image1.png)

   b) What source impedance will match \( Z_{in} \)?

   ![Image](image2.png)

   c) matching: find the capacitance \( C \) required to make \( Z_{in}=50 \) ohms.

   ![Image](image3.png)

2) Lumped-Element Equivalents:

   A) \[ Z_{o}, \text{length}\times X \]
   B) \[ Z_{in} \]
   C) \[ Z_{o}, \text{length}\times X \]
   D) \[ Z_{in} \]

   Using the smith chart, determine the reactances for the following elements over the frequency range \( f=0 \) to \( f=2f_{0} \), where \( L=Z_{o}\tau, \ C=\tau/Z_{o}, \ \tau=X/V_{p} \), and \( f_{0}=1/\tau \) where \( V_{p} \) is the transmission line (phase) velocity, and \( \tau \) is the line electrical time delay. Plot the trajectories of each on the Smith Chart, and also draw two rectangular plots of reactance-(normalized to \( Z_{o} \)) vs.-frequency (normalized to \( f_{0} \)), one with A) and C), the other with B) and D). Over what range of frequencies does which transmission line reactance approximate which lumped element reactance? This should give a very clear picture
3) Lattice Diagrams and Bus Structures

Sending end termination

Receiving end termination.

The circuit diagrams above represent logic gates interconnected by a 200? balanced transmission line, typical of ECL. The line is one meter long, with a third gate connected at the middle. The line velocity is 2/3 c. The gates have infinite input impedance and zero output impedance. In the sending-end termination case, the sending end is driven from a total source impedance of 150?, while in the receiving end case the receiving end is terminated in 150?. The output voltage of the driving gate is a 300 mV step-function; use lattice diagrams for the 2 cases to find the input voltages to the two receiving gates; which gates function correctly?

4) More on lattice diagrams and pulse responses:

In parts a and b the lines are driven by unit voltage impulses. In case a the line is 50? and the generator impedance 5000?, while in case b the line is 50? and the generator impedance 0.5?. In both cases the lines are 1 ps long.

First) Use Lattice diagrams to find the input voltage to the lines
Second) Using either pi- or T-equivalent lumped-element approximations to the circuits, again find the input voltage
Third) explain clearly what you have found.
You have worked through 2 of 4 possible cases-what would the other 2 cases be?