Problem 1: The MOSFETs have a +0.30 Volt threshold voltage and mobility-limited characteristics, with $\mu C_{ox}/2L_s = 1 \text{ mA}/(\mu \text{m} \cdot \text{V}^2)$ and $\lambda = 0 \text{ V}^{-1}$. For Q1 the gate width $W_{g1}$ is 1 $\mu$m. $V_{dd} = 3.3$ Volts. Pick $R_{ref}$ so that $I_{D1}$ is 100 $\mu$A. (a) What value is needed for $R_{ref}$? Assuming for a moment that $R_L$ is small, pick $W_{g2}$ so that $I_{D2}$ is 300 $\mu$A. (b) What value is needed for $W_{g2}$? (c) over what range of $V_{ds2}$, and over what range of $R_L$ is the output current $I_{D2}$ constant?

Problem 2: Using the circuit of problem 1, now set $1/\lambda = 10 \text{ V}$. In this case, do not ignore $\lambda$ in any calculation. (a) find the value of $R_{ref}$ needed to set $I_{D1}$ to 100 $\mu$A. (b) What width $W_{g2}$ is needed if $I_{D2}$ is to be 300 $\mu$A when $V_{dd} = 3.3$ V? (c) What is $I_{D2}$ when $V_{dd} = 2.3$ V? Hint, brute-force solution involves solving a cubic polynomial. In your math classes, you have learned various numerical methods to solve hard problems.

Problem 3: Q1 and Q2 are mobility-limited FETs with $V_{th} = 0.3$V, $\mu C_{ox}/2L_s = 1 \text{ mA}/\text{V}^2$ and $1/\lambda = 10 \text{ V}$. $V_{DD}$ is 2.5 V. The DC input bias voltage (as is shown) is zero volts. The DC output is at +0.5 Volts, and each FET carries 50 $\mu$A DC drain current. (a) Find $I_{ss}$ and $R_L$. (b) Draw a circuit diagram indicating all DC node voltages and all DC branch currents. (c) Find the transconductance and output conductance of each transistor. (d) Draw a small signal equivalent circuit of each transistor. (e) Draw a small-signal equivalent circuit of the whole amplifier. (f) If $V_{in} = 1 \text{mV} \cdot \cos(2\pi \cdot 1 \text{kHz} \cdot t)$ and
\[ V_{in}^- = 0.5 \text{mV} \cdot \cos(2\pi \cdot 1 \text{kHz} \cdot t) \], find \( V_{out}^+(t) \) and \( V_{out}^-(t) \)

Problem 4: The 4FETs are mobility-limited FETs with 
\( (\mu C_{ox} W / 2L_g) = 1 \text{ mA/V}^2 \) 
and \( 1/\lambda = 10 \text{ V} \). For the NFETs, \( V_{th} = 0.3 \text{V} \), while for the PFETs, the gate must be 0.3V negative of the source in order for the FET to turn on. The DC input bias voltage (as is shown) is zero volts. The drains of Q1 and Q2 are at +0.5 Volts DC, the drains of Q3 and Q4 are at +0.0 Volts and all FETs carries 50 \( \mu \text{A} \) DC drain current. (a) Find the values of the 2 DC current sources and the 4 resistors. (b) Draw a circuit diagram indicating all DC node voltages and all DC branch currents. (c) Find the transconductance and output conductance of each transistor. (d) Draw a small signal equivalent circuit of each transistor. (e) Draw a small-signal equivalent circuit of the whole amplifier. (f) If \( V_{in}^+ = 1 \text{mV} \cdot \cos(2\pi \cdot 1 \text{kHz} \cdot t) \) and \( V_{in}^- = 0.5 \text{mV} \cdot \cos(2\pi \cdot 1 \text{kHz} \cdot t) \), find \( V_{out}^+(t) \) and \( V_{out}^-(t) \)

Problem 5: The FET a mobility-limited with 
\( (\mu C_{ox} W / 2L_g) = 1 \text{ mA/V}^2 \) 
and \( 1/\lambda = 10 \text{ V} \) and \( V_{th} = 0.3 \text{V} \). The DC drain current is 50 \( \mu \text{A} \), the DC current in \( R_{G1} \) is 50 \( \mu \text{A} \), \( V_{DD} \) is 3.3 V, and the DC drain voltage is 2.0 V. \( R_L \) is four times \( R_D \), while \( R_{gen} = 100 \text{ kOhm} \). \( C_{in} = C_{out} = 1 \) microFarad. 
(a) Find the values of all resistors. (b) Draw a circuit diagram indicating all DC node voltages and all DC branch currents. (c) Find the transconductance and output conductance of the transistor. (d) Draw a small signal equivalent circuit of the transistor. (e) Draw a small-signal equivalent circuit of the whole amplifier. (f) Compute the small-signal transfer function \( V_{out}(s)/V_{gen}(s) \). (g) Find the pole and zero frequencies of the transfer function. (h) Make a Bode plot, (horizontal axis being frequency in Hz on semi log paper, vertical axis being dB) of \( V_{out}/V_{gen} \). (i) If \( V_{gen}(t) \) is a 1 mV step-function, find \( V_{out}(t) \) and make an accurate plot of this.