Wireless and Fiber Communication Circuits

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November 19, 2002
High Linearity and High Efficiency of Class B PA in GaN HEMT Technology


Objective

Design RF MMIC power amplifier in GaN HEMT technology to achieve the following simultaneously:

- High output power
- High linearity (low IM3 distortion)
- High efficiency
- Broad bandwidth

Approach

- 12 fingers (1.2mm) dual gate AlGaN/GaN HEMT device (Lg = 0.25um)
- Single-ended common Source Class B configuration
- Lossy input matching and low pass output matching networks.

Accomplishments

- \( I_{\text{dss}} = 1 \text{A/mm} \)
- \( V_{\text{br}} = 55 \text{V} \)
- Bandwidth: 7GHz ~ 10 GHz
- Output power: 36dBm (4W)
- Maxim PAE: 34%
- IM3 distortion: -35dBc

Proved experimentally that Class B is better than Class A because it provides good IM3 performance comparable to that of Class A, while providing PAE ~10% higher than that of Class A.
Title: Fully-Integrated 5.8GHz GaAs Power Amplifier

Authors: F. Bohn, S. I. Long, PI

Sponsors: Nokia Research Center/UC Micro Program

Objective

1. Demonstrate feasibility of fully-integrated GaAs based power amplifier (PA) as alternative to GaAs based power-amplifier modules (PAMs)

2. Design of a 5.8GHz ISM band constant-envelope, highly efficient, watt-level, fully-integrated power amplifier

Approach

1. Two on-chip differential inverse class-F switching power amplifiers

2. Integrated output power combiner/balun

3. Integrated input power splitter/balun

Accomplishments

1. Circuit-level analysis, design and simulation to evaluate tuning/matching requirements and loss mechanisms.

2. Investigation of passive loss mechanism and trade-offs.

3. Extensive E/M simulations of passive input/output power combiners/impedance transformers

Figures

Predicted Performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>5.8 GHz</td>
</tr>
<tr>
<td>Gain</td>
<td>10dB</td>
</tr>
<tr>
<td>PAE</td>
<td>&gt;50%</td>
</tr>
<tr>
<td>Output Power</td>
<td>&gt;3W</td>
</tr>
<tr>
<td>IO Impedance</td>
<td>50Ω</td>
</tr>
</tbody>
</table>
**Title:** High Efficiency High Linearity Power Amplifier  

**Authors:** Jingshi Yao, A. Long, S. I. Long  

**Sponsors:** Nokia Research Center, Samsung, Oplink, UC Micro Program

### Objective

1. Design and implementation of nonlinear Class D switching amplifier with high efficiency  
2. Investigation and demonstration of the technique of Linear Amplification using Nonlinear Components (LINC)

### Approach

1. Current Mode Class-D (CMCD) amplifiers using LDMOS  
2. Lossless combiner  
3. LINC linearization with phase predistortion

### Accomplishments

1. Implementation of a 13 watt CMCD with 60% efficiency at 1GHz  
2. Simulation results have achieved high linearity for LINC system using phase predistortion  
3. Measurement setup for LINC based on our CMCD amplifiers.

### 1 GHz Class D Amplifier
**Title:** High-Speed Mixed Signal Interconnect Design  

**Authors:** T. Collins and S. Long; **PI:** UCSB

**Sponsor:** iTerra Communications/UC MICRO

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**Objective**

1. Investigate various ground planes and transmission line topologies, to establish design rules for circuits operating over 40Gbit/s  
2. Push integration of high-speed InP circuits to Large Scale Integration

**Approach**

1. Simulate and model various transmission line structures: inverted microstrip, microstrip with suspended ground and stripline  
2. Design and test digital circuits of increasing size: Static Divider; Linear Feedback Shift Register and Bit Error Rate Tester

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**Accomplishments**

1. Seven Static Dividers have been fabricated with different interconnect structures, and different area and power requirements.  
2. Current Mode Logic static frequency divider demonstrated above 70GHz.

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**Figure**

- 66 GHz
- time, nsec
### Objective

1. Design a low phase noise frequency synthesizer for fiber optic application.
3. Characterize a divide-by-8 (Prescalar) for phase noise.
4. Assess maximum speed of SiGe BJT process using a static frequency divider.

### Approach

1. Test different configuration of prescalars for best phase noise performance.
2. Phase noise analysis of a PLL using prescalar and VCO phase noise data.
3. Measure static frequency divider to assess the maximum clock frequency.

### Accomplishments

1. Design and layout of static frequency divider for maximum clock speed.
2. Completed layout for test structures to characterize prescalars for phase noise.
3. Completed layout for a low phase noise PLL.

### PLL Layout
## Objective

1. Identify key contributors to VCO phase noise.
2. Analyze the degree to which circuit topologies and component improvements can be used to reduce the phase noise.

## Approach

1. Use the multi-level metal layer inductor to increase the Q-factor.
2. Reduce the noise contribution from the transistor by minimizing the transistor turn-on time.

## Accomplishments

1. VCO using 350um square multi-level inductor was built.
2. VCO using 250um square multi-level inductor was built.
3. Single metal layer and multiple metal layer inductor was built for comparison.