ECE 124a/256c
Power Distribution and Noise

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Chip Power Requirements

- Large Scale Chip Power Phenomenal
  - Pentium 4 @ 0.13um has 85A Peak Package Current
  - @ 1.5V requires .15/85 = 1.8mΩ total power network resistance
  - On-chip peak current risetime is <100pS!
- $I_{DD}$ changes on many time scales (DC to GHz)
Power Distribution Problem

- Maintain stable voltage with low noise
  - Noise reduces reliability and lowers performance
- Average Power
  - Electromigration (grain activation)
- Peak Current
  - IR drop in Vdd and Gnd Bounce
- Provide current return paths for signals
  - Transmission line signalling noise reduction
  - Simultaneous output switching
- Consume minimal routing area and wire resources
  - still need *levels* of metalization
Power Coupled Noise

- Droop due to IR drop, Ldl/dt noise and Supply Inductance
- Modulates behavior of Gates
  - Signalling Failure
  - Reduction of Noise Budget (Can you afford dynamic logic)
  - Reduction of System Performance
  - Increase in Power Dissipation
  - Reduction of device reliability
    - Hot Electrons
    - Oxide Damage
    - Electromigration
- Power noise can move the switching threshold of Gate
- Each repeater adds to the net jitter and skew at destination
Noise to Jitter Conversion: Fundamentals

- Uncertainty of threshold reference (A from power supply noise) determines jitter
  - The buffer can switch (threshold) anywhere in this region (A’)
  - The slower the rise time the more opportunity is presented to PWR noise

- Amount of jitter directly proportional to the magnitude of the noise/ripple/GND bounce
  - \( B \) (jitter) = \( A \) (noise) \* \( \frac{dt}{dV} \)
CMOS Power Loop is not local!

- Current from CMOS transistors comes from supply rails
  - BUT leaves via the output!
  - Load is accepted elsewhere on chip
- Not every output switches each cycle
  - Power loops are a function of state of the circuits!
- Upshot:
  - Cannot statically analyze local power requirements
  - Relatively little correlation between power and ground deviations in area bonded packaging
Power Distribution Mesh

- Connection point
- Connection point contribution
- Current flowing path

VDD (1)
VDD (2)
Module A
Module B
Module C

(3)
(5)
(6)
Gate Behavior with Noise

- Effective propagation time can be longer or shorter due to noise
  - Delay is proportional to noise magnitude
  - Noise induced delay can be either positive or negative
Logic Current Profile

- Assume triangle current profile: \( Q = C_{\text{Load}} V_{dd} \)

- Peak Current
  \[
  i_{\text{peak}} \approx \frac{2Q}{1.8t_r} = \frac{1.1C_{\text{Load}} V_{dd}}{t_r}
  \]

- Average Current
  \[
  i_{\text{avg}} = \frac{kC_{\text{Load}} V_{dd}}{t_{\text{clk}}}
  \]

- K denotes the probability of switching (each direction)
  - K=.5 for a clock
  - K=.2 for a heavily used part of microprocessor
  - K=.1 or less for typical asic
6-> 64 Decoder Current Profile

- Count number of gates switching
- For Power/Ground modeling, count number switching each direction
- Add delays and superpose the current
- Find Peak from $I_{\text{sat}}$ or $\Delta Q$ given the delay:
  - $I_{\text{peak}} = \min(I_{\text{sat}}, 1.1\Delta Q/t_r)$
Current Switching Profile
IR Drop

\[ V_{\text{drop}} = I_{\text{peak}} R_{\text{distribution}} \]

- IR drop is proportional to local peak current
  - Peak current reduced by parasitic bypass capacitance
  - Geometry to estimate \( R_{\text{dist}} \)
  - Inductance usually ignored since small compared to IR
    - Capacitive coupling is very large, inductance is the inverse
    - Not true for low resistance busses (e.g. pad frame wiring)

\[ V_{\text{drop}} = \sum_{\text{path}} I_i R_i + L_i \frac{dI_i}{dt} \]

- Local peak strongly affected by synchronization of clocking
  - Intentional skew (DAC ’98 Vittal)
Power Rail IR Drop

\[ V_{\text{drop} \,(\text{max})} = \frac{I_{\text{total}} R_{\text{total}}}{8} \]

- Distributed model of current loads and resistance
  - Supply from both sides, assume uniform load
  - Supply from one side, uniform: 4x as large = IR/2
Simple Chip Power Model

- $1 \mu m$ Copper = $0.029 \Omega$/sq., via = $1 \Omega$
  - Wide bus: 10mm long/25$\mu$m wide is $400 \times 0.029 = 12 \Omega$
  - Narrow bus: 50$\mu$m long/2$\mu$m wide is $25 \times 0.06 = 1.5 \Omega$

- Typical Power Density (0.18$\mu$m) 20,000 gates/mm$^2$
  - $J_{\text{peak}} = 0.54 A/mm^2$, $J_{\text{avg}} = 100 mA/mm^2$
Simple Chip Power Model II

- Assuming uniform demand, each segment needs to supply a total current for the portion of area it covers (segment pitch times chip width)
  - Assume pitch = 60μm, Source area is 0.06mm*10mm = 0.6mm²
    - Power rail drop is IR/8 = 0.54A*0.6mm²*12Ω/8=0.49V!, Ground Drop is similar… Note that we have used 86% of the copper on the level…
    - To get a barely acceptable drop, we’d need 2 full layers of metal dedicated to power and ground distribution.
    - In practice, the current peak is filtered by parasitic bypass of the non-switching gates (and designed-in bypass) which lowers the peak current
Bypass Calculation I

- Essential idea: Local capacitor supplies power for peak to provide lower frequency requirement to next stage of power network
- \[ Q = CV = It \text{ so: } C = \frac{t*I}{V} \]
- For Impulse of Total charge \( q \), we have: \( C = \frac{q}{\Delta V} \)
  - E.G. for \( I = 3A, t=1nS, \Delta V=0.1V \implies C=30nF \)
  - E.G. for \( q = 120fC, \Delta V=0.1V \implies C=1.2pF \)
Parasitic Bypass

- The majority of gates in a circuit do not switch on a given cycle—
  - Others provide low-resistance (few hundred ohms) path from gates (outputs) to one of the supply rails
  - Roughly 40% of total gate capacitance in given area is connected to each supply rail as bypass
  - (0.18um) 20,000 gates/mm², typical gate has 8-12 fF => 200pF/mm² local bypass or 20nF/1cm² die…
Parasitic Bypass Estimation

- Given the relatively large available bypass—how to estimate?
  - Could Simulate – expensive for large systems
  - Despite dynamic nature of the capacitances, for a subsystem the average capacitance are not strong functions of state

- Good Estimates: (2006 Nassif, Agarwal, Acar) (few percent)
  - For static portions of logic:
  - FET Capacitances basically proportional to width
  - Parasitic Capacitances in stacked FETs divide the voltage swing
  - 0.18um technology, standard cells $\alpha_n$=4fF/$\mu$m $\alpha_p$=1.2fF/$\mu$m
  - For each FET $i$, with width $W_i$ included in a stack of Height $H_i$

$$C = \alpha_n \sum_{i \in N} \frac{W_i}{H_i} + \alpha_p \sum_{i \in P} \frac{W_i}{H_i}$$
Simple Model (Reprise)

- Parasitic Bypass lowers the required peak current
  - For our model $C_{\text{load}}/\text{mm}^2 = 20\text{pF/mm}^2$ (I_p=0.56A/mm$^2$)
  - We have 200pF/mm2 bypass so expect 10% supply deviations = 0.18V on both Vdd and Ground rails + IR drop
  - New IR drop is average current = 100mA/mm2 or 5.6x smaller
  - Total drop = 0.18V+0.49/5.6=0.27V… a bit perilous, but survivable
- Note: Doubling supply metal will only reduce noise to 0.23V
- Doubling Capacitance (adding designed-in local bypass) will lower it to 0.18V

Moral–Bypass whenever possible
Metal Migration

- **Al** (2.9μΩcm M.P. 660 C)
  - 1mA/µm² at 80C is average current limit for 10 year MTTF
  - Current density decreases rapidly with temperature
- **Cu** (1.7μΩcm M.P. 1060 C)
  - 10mA/µm² at 100C or better (depends on fabrication quality)
  - Density decreases with temperature, but much slower over practical Silicon operation temperatures <120C
- Find Average current through wire – check cross section
  - Be wary of Via’s!! Typical cross-section 20-40% of minimal wire.
Off Chip Power Noise

Packaging, Board Distribution and Power Supply Issues
Package Parasitics

- Use many $V_{DD}$, GND in parallel
  - Inductance, $dl/dt$, Impedance Control
Power System Model

- Power comes from regulator on system board
  - Board and package add parasitic R and L
  - Bypass capacitors help stabilize supply voltage
  - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses
Imperfect Bypass Capacitors

- Even with the addition of bypass capacitance there are still sources of inductance in the current loop which can cause power supply noise.
  - Plane inductance
    - Determined by the shape of the plane (pH/sq) and dielectric thickness
    - E.g. 15cm radius to 2cm radius = 70pH
  - Bypass capacitor parasitics
  - Capacitor Mounting
    - Solder land, trace to via, *via itself*
Bypass Capacitors

- Need low supply impedance at all frequencies
- Ideal capacitors have impedance decreasing with $\omega$
- Real capacitors have parasitic $R$ and $L$
  - Leads to resonant frequency of capacitor $\omega_{cap} = 1/\sqrt{LC}$
Chip Bypass Capacitors

- Series Resistance can create alternative breaks:
  - Often need to parallel capacitors to achieve lower inductance

\[ \omega_{RC} = \frac{1}{RC} \quad \omega_{LR} = \frac{R}{L} \quad \omega_{cap} = \frac{1}{\sqrt{LC}} \]
Frequency Response

- Use multiple capacitors in parallel
  - Large capacitors near regulator have low impedance at low frequencies
  - also low resonant frequency (ineffective at high freq)
  - Small capacitors near and on chip have low impedance at high frequencies

- Choose caps to get low impedance at all frequencies
Aggregate Bypass Network

Simulation is needed to view network impedance profile

- Should cover frequencies from 100 kHz to 300MHz (Board/Package)
- Impedance should be low and flat over this range
Board Vias – Parallel Connection

- Mounted Capacitor Parasitics
  - $L_C$ Capacitor self-inductance 0.7nH - 1.2nH
  - $L_{LD, LC}$ Solder land inductance of device and cap 0.1nH - 0.4nH
  - $L_P$ Power plane inductance 0.03nH - 0.4nH
  - $L_{VP}$ Via pair inductance \textbf{0.3nH - 3.2nH}

- Via parasitic can be biggest contributor
- Board thickness is critical factor if caps on the bottom
  - 62mil finished thickness -- typical $L_{VP} = 1.5nH$
  - 127mil finished thickness -- typical $L_{VP} = 3.2nH$
Power Supply Inductance

- Average current through inductor subject to low frequency variations
  - Must control excursions of voltage across the capacitor
  - Inductor does not see high frequency components as long as capacitor can supply bulk of current
  - MUST stay away from resonant frequency of LC circuit
Bypass Reprise: LC step response

- Low Frequency steps in current trigger resonant response

\[ V_c = \frac{Q_L}{C} \quad V_L = L \frac{dI(t)}{dt} \quad V_c = V_L \Rightarrow V_c = LC \frac{d^2V_c}{dt^2} \]

- Solution: \( V_c(t) = \frac{I_{avg}}{\omega_c C} \sin(\omega_c t) + V_{dd} \)

- Solving for C given restriction on V:

\[ C > L \left( \frac{I_{avg}}{V_{droop}} \right)^2 \]
Basic Bypass Rules

- Use small capacitor packages
  - Parasitic L is proportional to pkg. Size and aspect ratio

- Use largest value subject to resonant point
  - L is dominated by pkg, so choose C at limit of frequency

- Connect cap lands directly to planes

- NEVER share cap vias

- Keep trace between land and via short!!
  - Benefit of small package is lost otherwise
Spy-Hole vs. Backside Measurements

- **PCB PDS**
  - PCB vias, planes
  - Backside Via

- **PKG**
  - Bondwire or pkg route
  - Package Ball

- **DIE**
  - IOB
  - IO Output
  - 1
  - 0

- **V^+**

Measure here:
- Noise on PCB PDS (somewhat irrelevant to FPGA operation, but can tell you if someone else (another device) is muddying the water)
- Ground Bounce (how much noise is between PCB PDS and the FPGA die)
Simultaneous Switching Noise

- Issue: Modern packages have hundreds of I/O pins
  - Each pin is driving 50-60Ω timeline on pc-board
  - Rise/fall time of line must be smaller than Bandwidth/3

- Potential for very large $dI/dt$ spike if synchronized:
  \[
  \frac{dI}{dt} = \frac{V_{swing}}{50\Omega \times 1.8t_r} \approx \frac{28mA}{t_r} \quad L < \frac{V_{droop}}{dI/dt} = t_r \frac{V_{droop}}{N_{pins} 28mA}
  \]

- For 333MHz DDR – 80pins at $t_r=0.5\text{nS}$ (50%):
  - 4.5GA/s $\Rightarrow$ at 0.3V drop, need 63pH power supply inductance

- Solution: mixture of on-chip bypass in the pad drivers and lots of connections to power and ground to lower inductance