Flip-Flops and Sequential Circuit Design

ECE 152A – Summer 2009

Reading Assignment

- Brown and Vranesic
  - 7 Flip-Flops, Registers, Counters and a Simple Processor
    - 7.5 T Flip-Flop
      - 7.5.1 Configurable Flip-Flops
    - 7.6 JK Flip-Flop
    - 7.7 Summary of Terminology
    - 7.8 Registers
      - 7.8.1 Shift Register
      - 7.8.2 Parallel-Access Shift Register
Reading Assignment

- **Brown and Vranesic** (cont)
  - 7 Flip-Flops, Registers, Counters and a Simple Processor (cont)
    - 7.9 Counters
      - 7.9.1 Asynchronous Counters
      - 7.9.2 Synchronous Counters
      - 7.9.3 Counters with Parallel Load
    - 7.10 Reset Synchronization

Reading Assignment

- **Brown and Vranesic** (cont)
  - 7 Flip-Flops, Registers, Counters and a Simple Processor (cont)
    - 7.11 Other Types of Counters
      - 7.11.1 BCD Counter
      - 7.11.2 Ring Counter
      - 7.11.3 Johnson Counter
      - 7.11.4 Remarks on Counter Design
Reading Assignment

- **Brown and Vranesic (cont)**
  - 8 Synchronous Sequential Circuits
    - 8.1 Basic Design Steps
      - 8.1.1 State Diagram
      - 8.1.2 State Table
      - 8.1.3 State Assignment
      - 8.1.4 Choice of Flip-Flops and Derivation of Next-State and Output Expressions
      - 8.1.5 Timing Diagram
      - 8.1.6 Summary of Design Steps

---

Reading Assignment

- **Brown and Vranesic (cont)**
  - 8 Synchronous Sequential Circuits (cont)
    - 8.2 State-Assignment Problem
      - One-Hot Encoding
    - 8.7 Design of a Counter Using the Sequential Circuit Approach
      - 8.7.1 State Diagram and State Table for Modulo-8 Counter
      - 8.7.2 State Assignment
      - 8.7.3 Implementation Using D-Type Flip-Flops
      - 8.7.4 Implementation Using JK-Type Flip-Flops
      - 8.7.5 Example – A Different Counter
Reading Assignment

- **Roth**
  - 11 Latches and Flip-Flops
    - 11.5 S-R Flip-Flop
    - 11.6 J-K Flip-Flop
    - 11.7 T Flip-Flop
    - 11.8 Flip-Flops with Additional Inputs
    - 11.9 Summary
  - 12 Registers and Counters
    - 12.5 Counter Design Using S-R and J-K Flip-Flops
    - 12.6 Derivation of Flip-Flop Input Equations – Summary

The JK Flip-Flop

- Allows J = K = 1 condition
  - Implemented with a gated SR latch and feedback of Q and Q*
    - Q toggles (Q+ = Q') on J = K = 1

![Diagram of JK Flip-Flop]
The JK Flip-Flop (cont)

- Characteristic table and equation
  - Karnaugh map of characteristic table
  - Characteristic equation
    - \( Q^+ = JQ' + K'Q \)

- Implementation using a D flip-flop
  - Characteristic Function at D input
The JK Flip-Flop

- State table

<table>
<thead>
<tr>
<th>PS ($Q$)</th>
<th>JK = 00</th>
<th>01</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

- State diagram
The JK Flip-Flop

- With clock circuitry and timing
  - Positive edge triggered JK flip-flop

![JK Flip-Flop Diagram]

The Master Slave JK Flip-Flop

- Master Slave JK Flip-Flop
  - Rising edge triggered
    - note CLK inverted to master

![Master Slave JK Flip-Flop Diagram]
The Master Slave JK Flip-Flop

- Master Slave JK Flip-Flop
  - Falling edge triggered
    - note CLK (CP) inverted to slave

```
<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>X</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
```

- Master active on CLK = 1
- Slave active on CLK = 0
  - Latch data in master on CLK = 1
  - Transfer data to slave (output) on CLK = 0
- Timing Diagram Initial Conditions
  - CLK = 0, J = 1, K = 0, Y = 0, Q = 0
The Master Slave JK Flip-Flop

- Timing Diagram

The JK Flip-Flop (cont)

- What happens if \( J = K = 1 \) for an indefinite period of time (i.e., much greater than clock period)?
  - Output oscillates at \( \frac{1}{2} \) the frequency of the clock
  - Divide by two counter
The T (Toggle or Trigger) Flip-Flop

- Connect J and K inputs together
  - Combined input “T”

Characteristic Table

<table>
<thead>
<tr>
<th>T</th>
<th>0</th>
<th>0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Characteristic Equation

\[ Q' = Q \cdot 0' + 1 \cdot 1 + T \cdot Q \cdot 0' \cdot 1 \cdot 0 \]

Timing Diagram

State Table

<table>
<thead>
<tr>
<th>NS (Q')</th>
<th>PS (Q)</th>
<th>T = 0</th>
<th>T = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
The T Flip-Flop

- State Diagram

\begin{align*}
T = 0 & \quad 1 \\
T = 1 & \quad 0
\end{align*}

\begin{align*}
Q^+ &= JQ' + K'Q \\
Q^+ &= T'Q + TQ' = T \text{ XOR } Q
\end{align*}
Counter Design with T Flip-Flops

- 3 bit binary counter design example
  - “State” refers to Q’s of flip-flops
  - 3 bits, 8 states
    - Decimal 0 through 7
- No inputs
  - Transition on every clock edge
    - i.e., state changes on every clock edge
    - Assume clocked, synchronous flip-flops

Counter Design with T Flip-Flops

- State Diagram

```
000 --- 001 --- 010 --- 011
      |         |         |
      v         v         v
111 --- 110 --- 101 --- 100
```

July 27, 2009 ECE 152A - Digital Design Principles
Counter Design with T Flip-Flops

- State table

<table>
<thead>
<tr>
<th>PS A</th>
<th>B</th>
<th>C</th>
<th>NS A*</th>
<th>B*</th>
<th>C*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- Next State Maps

\[
A^* = AB' + AC' + A'BC = D_A \\
B^* = B'C + BC' = D_B \\
C^* = C' = D_C
\]
Counter Design with T Flip-Flops

- Using D flip-flops, inputs are derived directly from next state maps
  - \( D = Q^+ \)
- Using T flip flops
  - Excitation table (used for design)
    - \( T = Q \oplus Q^+ \)
  - Need to find inputs to T flip-flops
    - Mapping state changes
      - \( Q \rightarrow Q^+ \) requires \( T = ? \)

---

T Flip-Flop Excitation Table

\[
\begin{array}{ccc}
Q & Q^+ & T \\
0 & 0 & 0 \\
0 & 1 & 1 \\
1 & 0 & 1 \\
1 & 1 & 0 \\
\end{array}
\]
Counter Design with T Flip-Flops

- **State Variable A**
  - \( T_A = A' \) (XOR) \( A \)
  
  \[
  \begin{array}{c|c|c|c}
  \hline
  BC & 00 & 01 & 11 & 10 \\
  \hline
  A & & & & \\
  \hline
  A=0 & A^+ = 1 & & & \\
  \hline
  A^+ = AB' + AC' + A'BC = D_A \\
  \end{array}
  \]

  \( T_A = BC \)

- **State Variable B**
  - \( T_B = B' \) (XOR) \( B \)
  
  \[
  \begin{array}{c|c|c|c}
  \hline
  BC & 00 & 01 & 11 & 10 \\
  \hline
  B & & & & \\
  \hline
  B=0 & B^+ = 1 & B^+ = 1 & & \\
  B=1 & B^+ = 1 & B^+ = 1 & & \\
  \hline
  B^+ = B'C + BC' = D_B \\
  \end{array}
  \]

  \( T_B = C \)
Counter Design with T Flip-Flops

- **State Variable C**
  - \( T_C = C^+ \text{ (XOR) } C \)

<table>
<thead>
<tr>
<th>BC</th>
<th>C=0</th>
<th>C=1</th>
<th>C=0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>00</td>
<td>01</td>
<td>11</td>
</tr>
<tr>
<td>0</td>
<td>( C^+ = 1 )</td>
<td>( C^+ = 1 )</td>
<td>( C^+ = 0 )</td>
</tr>
<tr>
<td>1</td>
<td>( C^+ = 1 )</td>
<td>( C^+ = 0 )</td>
<td>( C^+ = 0 )</td>
</tr>
</tbody>
</table>

  \( C^+ = C^+ = D_C \)

- **Implement design using T Flip-Flops with asynchronous preset and clear**
  - Asynchronous preset (PRN) and clear (CLRN) override clock and other inputs
    - Preset : \( Q \rightarrow 1 \), Clear : \( Q \rightarrow 0 \)
    - Used to initialize system (all flip-flops) to known state
      - Bubbles indicate "low true" or "active low"
  - \( TA = BC, TB = C, TC = 1 \)
Counter Design with T Flip-Flops

- Schematic

![Schematic Diagram]

- Timing Diagram
  - QA toggles when B = C = 1
  - QB toggles when C = 1
  - QC toggles on every clock edge

<table>
<thead>
<tr>
<th>Name</th>
<th>500 ns</th>
<th>1000 ns</th>
<th>1500 ns</th>
<th>2000 ns</th>
<th>2500 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>[Q] CLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Q] CLR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Q] QA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Q] QB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Q] QC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Counter Design with JK Flip-Flops

- State Diagram

![State Diagram](Counter_Design_with_JK_Flip-Flops_StateDiagram.png)

- State Table

<table>
<thead>
<tr>
<th>PS</th>
<th>NS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Counter Design with JK Flip-Flops

- **Next State Maps**
  - A\(^*\) = B\(^*\) = D\(_A\)
  - B\(^*\) = A + BC\(^*\) = D\(_B\)
  - C\(^*\) = AB\(^*\) + BC\(^*\) = D\(_C\)

- **JKR FliphFlop RExcitation RTable**
  - Recall JKR state diagram
  - Create excitation table from state diagram
    - Q\(^+\) = JQ\(^-\) + K\(^1\)Q

Counter Design with JK Flip-Flops

- **JK Flip-Flop Excitation Table**
  - Recall JK state diagram
  - Create excitation table from state diagram
    - Q\(^+\) = JQ\(^-\) + K\(^1\)Q
Counter Design with JK Flip-Flops

**State Variable A**
- $A^+ = B'$

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>$J_A$</th>
<th>$K_A$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Counter Design with JK Flip-Flops

**State Variable B**
- $B^+ = A + BC'$

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>$J_B$</th>
<th>$K_B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
</tbody>
</table>

$J_B = A$
$K_B = A'C$
Counter Design with JK Flip-Flops

- **State Variable C**
  - $C^* = AB' + BC'$

<table>
<thead>
<tr>
<th>$A$</th>
<th>$B$</th>
<th>$C$</th>
<th>$D$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

$J_C = A + B$

$K_C = 1$