Silicon-on-Nothing (SON)—an Innovative Process for Advanced CMOS

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Abstract—A novel CMOS device architecture called silicon on nothing (SON) is proposed, which allows extremely thin (in the order of a few nanometers) buried dielectrics and silicon films to be fabricated with high resolution and uniformity guaranteed by epitaxial process. The SON process allows the buried dielectric (which may be an oxide but also an air gap) to be fabricated locally in dedicated parts of the chip, which may present advantages in terms of cost and facility of system-on-chip integration. The SON stack itself is physically confined to the under-gate-plusspacer area of a device, thus enabling extremely shallow and highly doped extensions, while leaving the HDD (highly doped drain) junctions comfortably deep. Therefore, SON embodies the ideal device architecture taking the best elements from both bulk and SOI and getting rid of their drawbacks. According to simulation results, SON enables excellent Ion/Ioff trade-off, suppressed self-heating, low S/D series resistance, close to ideal subthreshold slope, and high immunity to SCE and DIBL down to ultimate device dimensions of 30 to 50 nm.

Index Terms—CMOS, CMOS architecture, epitaxy, microelectronics, MOSFET, short-channel effects, SiGe, silicon devices, SOI.

I. INTRODUCTION

The major bottlenecks of the device downsizing below 100 nm are in the short channel effect (SCE) and in issues related to thin gate oxides (reliability, direct tunnelling, gate depletion and boron penetration). The latter can be potentially circumvented by switching to high-k dielectrics which, however, may require integration with metallic gate [1], [2]. The metallic gate, in turn, implies a buried channel architecture that has bad reputation of leading to relaxed short channel effects. All this means, that for realization of the transistors below 100 nm, new architectures may become necessary.

The first comparative analysis has already been carried out [3]–[5] to search for the best CMOS architecture for decanomeric devices. Double-gated (DG) MOSFET [6]–[9] is considered the most promising candidate for CMOS down-scaling to the ultimate limit of 20 nm channel length but its technological realization remains a difficult task. SOI MOSFETs are also of interests as a more conventional alternative [10], [11]. Previous experimental and simulation work has shown that thinning silicon film thickness and buried oxide layer is an effective way to suppressing SCE [11]–[16]. According to our own simulations (see further-on), a “super SOI” with the silicon film of 5 nm and buried oxide of 20 nm is capable of suppressing SCE even at the ultimate limit of 20-nm channel length, which renders it competitive with DG structure. These requirements on thickness of both the silicon and buried oxide films exceed, however, the present manufacturing capabilities. In the current state of the art, the SOI film thickness ranges from 50 to 150 nm with the uniformity of ±10 nm across the wafer and the buried oxide is in the range of 50 to 400 nm [17], also with the uniformity of ±10 nm. Note that this current level of thickness nonuniformity influences approaches relying on local thinning of the commercially available SOI wafers by for example using the LOCOS process [18], [19], due to the transfer of the nonuniformity to the thinned SOI film.

In this paper, we propose an innovative process called silicon-on-nothing (SON) enabling fabrication of the desired “super SOI” devices which are capable of quasitotal suppression of SCE and DIBL and excellent electrical performances thanks to the extremely thin silicon (5 to 20 nm) and buried dielectric (10 to 30 nm). In Section II, we will present the concept of the SON device and demonstrate experimentally morphological feasibility of SON devices and their integration within conventional silicon CMOS process. Next, we will demonstrate the usefulness of the SON structure for some potential applications by simulation. Therefore, Sections III–VI present briefly the advantages SON can bring in terms of junction depth, integration of metallic gate, suitability for low-voltage operation and heat dissipation, respectively. In these sections the electrical performances of the SON devices...
will be presented and benchmarked against bulk and conventional SOI devices by simulation. Conclusions will be drawn in Section VII.

It should be emphasized that due to the nanometer scale of the Si and SiO2 layer thickness, there may be a small constant shift in absolute values of simulated threshold voltages ($V_{th}$) which are simulated using the drift-diffusion model. Nevertheless, we consider our conclusions should be pretty reliable, mainly because we have limited the simulations to the sub-threshold region. In this region, apart of the shift in $V_{th}$ resulting mainly from the neglect of the carrier centroid distance from the Si/SiO2 interface, the drift-diffusion model is still valid and commonly used as for example in ([5], [14] and [15]).

II. CONCEPT OF SON

In contrast to all other SOI fabrication technologies (SIMOX, BESOI, Smart Cut, ELTRAN, ELO, etc.) in the new SON technology, the silicon film and buried insulator, both of nanometric scale, are defined by epitaxy on a bulk substrate. The cross-section of the SON MOSFET is shown in Fig. 1. The buried oxide is not continuous (contrary to the case of conventional SOI) and is located only under the gate and spacers. The straightforward advantage of such an arrangement is in reduced series resistance and easier silicidation, compared with conventional SOI of an equivalent silicon film thickness.

The fabrication process of SON transistor starts from the conventional STI isolated wafers. Then, the epitaxy of SiGe layer is performed followed by that of a silicon cap layer, which will later serve as the transistor channel [Fig. 2(a)]. The role of SiGe consists in transferring the continuity of the lattice from the bulk to the silicon cap, thus, providing a monocristaline structure of the latter. It is straightforward, that both layers can be much thinner and much better controlled than in any conventional SOI technology, since the epitaxial process is capable of performing the layers of nanometer scale thickness with excellent uniformity and resolution below 1 nm.

After the epitaxy, the conventional CMOS process steps are carried out until the formation of the spacers [Fig. 2(b)]. Next, using anisotropic plasma etching, trenches in source/drain regions are formed in order to open access to SiGe, which is then selectively etched, also within a plasma process. The removal of SiGe from underneath of the Si cap forms an air tunnel, which isolates the silicon film, attached to the gate via gate oxide, from the substrate, Fig. 2(c). This air tunnel gives the SON name to the new architecture. Despite the air tunnel, the gate does not collapse because it bridges the active area and is supported at both ends on the STI, see Fig. 2(f). The SEM photo shown in Fig. 3 supports the feasibility of this step. In the case of empty tunnel, a passivation of its internal walls with a thin RTO oxide is used for preventing the tunnel from being refilled with silicon when rebuilding the S/D regions by epitaxy; see below. The tunnel may also be completely filled with a dielectric to form a super thin SOI-like devices.

The technological results regarding the etching of the tunnel of the SON structure are well seen in the TEM photos in Fig. 4. In our first experiments we obtained 15 nm thick Si film over an empty 20-nm thick tunnel. The thickness of the tunnel remains equal to that of the SiGe layer. High selectivity factor in plasma etching process (more than 100 : 1 for 20% Ge mole fraction) enables formation of very long tunnels, in this case 150 nm per side. This is more than needed for the fabrication of 100 nm CMOS devices (requiring less than 100-nm tunnels per side). The requirements on the tunnel length will be relaxed for the successive CMOS generations due to shorter nominal channel length.

It has to be noted that its thickness and the risk of relaxation limit the Ge mole fraction in the SiGe layer, which determines
We will now pass through some issues of concern of future CMOS down-scaling, such as shallow junction, metallic gate integration, and heat dissipation, and investigate via simulation what kind of potential advantage can be expected if SON device replaces the conventional bulk transistor.

III. SON VERSUS NEEDS FOR SHALLOW JUNCTIONS

As shown in Fig. 7, the junction of S/D extensions can be placed as-implanted within the SiGe layer. After removing of the SiGe, the junction depth reduces to the physical thickness of remaining Si layer, which can be as thin as a few nanometers. Moreover, the dielectric cavities under the extensions prevent the smearing out of the junction profile during thermal steps, which therefore can be doped to high level and comfortably annealed.

As results from Fig. 8, the superiority of SON devices in terms of SCE is in major part due to the very thin junction. This figure shows the threshold voltage roll-off as a function of channel length simulated for bulk and SON MOSFETs with various junction depths and various positions of the peak of the retrograde profile. The results concerning SON formally apply also to SOI, with that restriction, however, that SOI is unable to realize in a reproducible manner such thin films as SON. Considering the retrograde profile (compare the two most right-hand side plots), we can see that passing from \( x_j = 30 \) nm (lightly doped channel) down to \( x_j = 5 \) nm, we reduce \( L_{\text{min}} \) (let \( L_{\text{min}} \) be defined as the channel length corresponding to 100 mV roll-off) by less than one generation (from 0.09 to 0.07 \( \mu m \)). Then, implementing the thin buried oxide below the channel (SON) allows additional gain of roughly one generation (\( L_{\text{min}} \) passes from 0.07 \( \mu m \) down to 0.03 \( \mu m \)).

Accumulation of these three improvements makes a difference between the current state-of-the-art bulk MOSFET \((x_j = 40 \text{ nm}, x_a = 30 \text{ nm})\) and the SON MOSFET \((x_j = 5 \text{ nm}, x_a = 5 \text{ nm}, \text{ plus buried oxide})\). The total amount of improvement dividing these two cases is estimated to roughly four CMOS generations. We believe that whereas this total effect is a thorough assessment, those concerning the singular effects of \( x_a, x_j \) and the buried oxide may depend on the sequence of their consecutive implantation into the process. In any case, the real value of this exercise is of course not in an exact prediction but rather in the indication of trends and possibilities offered by SON.

It is interesting to position the predictions about SON junctions within the state-of-the-art results concerning shallow junctions. As seen in Fig. 9, there is a strong trade-off between the junction depth and its sheet resistance, which makes fabrication of shallow and lowly resistive junctions very difficult. The solid lines (simulation results) superimposed on the literature experimental points [20]–[32] suggest that 20-nm deep junctions are facturable yet, but an extrapolation of available results conducts to an estimation of its mean doping at largely below 1 \( \times 10^{19} \text{ at/cm}^3 \), which would probably compromise its usefulness. Concerning SON, we have demonstrated morphological feasibility of junctions as shallow as 15 to 30 nm (Figs. 4 and 6) and do not see any physical reasons which would impede fabrication of SON films (junction depths) down to 5 nm. Below that thickness, a nonclassical conduction may rapidly alter the film sheet.
resistance [33]. Consequently we will refrain from predictions at beyond 5 nm, but for 5-nm and thicker films, the active doping in SON junctions should not be lower than \(1 - 2 \times 10^{20} \text{ at/cm}^3\). These are the values which correspond to active doping with deep bulk junctions, thus taking into account that with SON equally large doping and activation budgets are allowed, a similar active doping level should be produced. Still, this latter is an estimation, and until having been supported by measurements must be taken with caution. In addition to possible nonclassical conduction, issues such as dopant out-diffusion, segregation etc. will have to be verified.

IV. SON VERSUS INTEGRATION OF METALLIC GATES

The high-k dielectrics often require integration with metallic gate, which is also desirable for preventing gate depletion, boron penetration, GIDL and junction leakage. A single
mid-gap metallic gate is the most straightforward, but then problems arise with the SCE/DIBL control. This is due to a buried-channel, indispensable for threshold voltage adjustment in the case of mid-gap gate [34].

Fig. 10 shows the threshold voltage and roll-off of 50-nm and 70-nm n-channel SON MOSFETs with polysilicon N+ gate and silicon films of 5 nm simulated for wide range of channel doping concentrations. For the SON transistor with the silicon film of 5 nm the roll-off is below 60 mV for the entire domain. These results show an excellent immunity of the SON transistor to the SCE/DIBL. Adjusting the threshold voltage can, however, be a more difficult task. In order to adjust the threshold voltage of a long transistor with polysilicon n+ gate, with the silicon film Ts of 5 nm and with the gate oxide Tox of 1 nm to the value of 0.25 V, the doping concentration in the channel has to exceed $10^{19}$ cm$^{-3}$. The metallic mid-gap gate architecture, gives wider technological window to adjust the threshold voltage. To obtain the required threshold voltage of $\pm 0.3$ V (to end up with $+0.25$ V after substituting polysilicon N+ gate by the metallic one and having corrected for the $+0.55$ V of shift in $\Phi_{ns}$), the channel counter doping in the order of $6 \times 10^{18}$ cm$^{-3}$ is sufficient. This may be advantageous from the point of view of GIDL and junction leakage.

Fig. 11 shows the saturated threshold voltage (extracted at $V_d = 0.9$ V) versus channel length as simulated for the SON, conventional SOI and bulk MOSFETs, all of them supposed with mid-gap gate and buried channel. In all cases the threshold voltage of long channel devices has been adjusted to 0.3 V. When defining the Lmin as that particular channel length which corresponds to 100 mV roll-off, both the state-of-the-art bulk and SOI face a limit of 100-nm of channel length. SON (and any other SOI or SOI-like architecture capable of producing super thin Si films), is capable of pushing the Lmin down to 25 nm if Ts is thinned down to 5 nm. This superiority of SON results from a very thin silicon film and the presence of thin buried oxide under the channel. These allow defining extremely thin counter doping layer of 5 to 10 nm (unreachable within the bulk technology due to diffusion). The buried oxide also eliminates the channel-substrate junction that widens the path of the lateral field penetration in the buried-channel transistor. Within the state-of-the-art of bulk devices, the buried-channel junction depth can hardly reach 30 nm, thus, this is the value we used in our simulations. It is interesting to note the difference (in favor of SON) of more than one generation between the 20 nm S-film SOI and the 20 nm Si-film SON. This is attributed to the effect of thinner buried oxide, 400 nm in the case of SOI and only 20 nm in that of SON. Note that the positive effect of buried oxide thinning has been reported before in, e.g., [10], [14] and [15].

As results from [5] and [15], a still further improvement may be expected in the case of empty tunnel due to reduced dielectric constant, which is potentially possible with SON.

V. SON VERSUS NEEDS FOR LOW-VOLTAGE OPERATION

An improved subthreshold slope is often put forward as an argument in favor of SOI devices as far as low-voltage applications are considered. It has been demonstrated [35] that fully depleted SOI with thick buried oxide exhibits extremely low subthreshold slope, close to the ideal value of $60$ mV/dec which is definitely lower than the best results measured on bulk devices. This is true for long channel transistors, but may no longer be valid in the case of short channel ones. The superiority of SOI in terms of ideal subthreshold slope is lost in short channel devices because of the too thick buried oxide that acts as a field guideline. Fig. 12 shows the potential contours for two thicknesses of buried oxide: 400 nm typical for conventional SOI—Fig. 12(a), and 20 nm typical for SON—Fig. 12(b). In spite of all other geometrical and electrical parameters being strictly identical the device with Tox = 400 nm shows a potential distribution typical for DIBL dominated regime of operation, whereas at Tox = 20 nm the distribution is long-channel-like. The thick buried oxide reinforces the source-to-drain coupling which is out of gate control and thus relaxes the electrostatic integrity of a device [36]. Consequently, the subthreshold slope $S$ increases more rapidly and converges with that of a bulk transistor, see Fig. 13. Only SON (or SOI) transistors with very thin silicon films and thin buried oxide can be scaled down to 20-nm channel length still maintaining the subthreshold slope below...
Fig. 12. Potential distribution at $V_{gs} = V_{th}$ and $V_{ds} = 0.9$ V in 50 nm transistors with (a) buried oxide $Tob = 400$ nm as typical for SOI and (b) $Tob = 20$ nm as typical for SON. The gate oxide is 1-nm thick for both.

Fig. 13. Subthreshold slope versus channel length simulated for different device architectures with $Tox = 1$ nm and $V_{ds} = 0.9$ V. The inset shows body factors calculated for long channel devices.

80 mV/dec. It is interesting to note that the body factor $Kb$ increases when thinning the buried oxide but even in the extreme case of $Tob = 20$ nm, the $Kb$ value relevant to SON devices is much lower than that of bulk devices; see the inset in Fig. 13.

VI. SON VERSUS HEAT DISSIPATION

Depending on operation mode, the self-heating of devices may be a more or less critical problem. In digital CMOS circuits, the self-heating at the level of a singular transistor is not so much a problem due to dynamic operation mode. However, the advantage of SON regarding the overall heat dissipation at the level of chip may be important. It is therefore interesting to note that contrary to the conventional SOI devices, the buried oxide in the SON transistors does not extend under the source and drain regions. This provides better heat dissipation than in SOI. Much thinner buried oxide in SON compared with SOI also contributes to better heat dissipation.

The simulation results confirm these predictions. Fig. 14 shows the maximal temperature in the channel of an SOI transistor and an SON transistor. The SOI device has a silicon film of 20 nm and the buried oxide of 400 nm, and the SON device has the same silicon film thickness but thinner buried oxide of only 20 nm. Owing to much lower thermal conductivity of the oxide, high current flowing in the channel leads to an increase of the channel temperature which for the $V_{ds} = V_{gs} = 1$ V reaches 566 °K. In contrast, in short channel SON transistor the heat produced in the channel can be quickly dissipated through source and drain as well as through the thin oxide. Thus, under the same bias conditions the maximal temperature in the channel increases merely up to 312 °K.

VII. CONCLUSIONS

An innovative fabrication process called silicon-on-nothing (SON) has been presented. This process enables fabrication
of SOI-like structures with well-controlled and extremely thin buried oxide and silicon films directly on bulk substrates. The very thin layers in the SON transistor allow quasitotal suppression of the short channel effects and excellent electrical performances. The SON architecture gives also additional flexibility to the junction design. Ultrashallow extensions and sufficiently deep hard junctions may simplify contact and salicidation processes as compared to the conventional thick film SOI. It was also demonstrated that SON is better suited than bulk or SOI for accepting a metallic gate and for low-voltage operation. It is also free from the self-heating problem.

The feasibility of SON key steps has been demonstrated experimentally at both morphological and material levels. Even if the SON process does require some additional steps, none of them relies on specific equipment or really new materials. The epitaxy of SiGe and Si is a known and already mastered step in HBT BiCMOS technologies. The etching of S/D depressions is readily feasible with ordinary etchers and does not differ much from any gate etching process, being in addition much shallower (20 to 30 nm) than the gate etch (150 to 200 nm). The lateral etching of SiGe may be wet or dry and is not critical due to the very high selectivity with respect to silicon and oxide. Finally, the selective epitaxy of S/D resembles very closely the elevated S/D which are anyway forecasted as a very likely step in the major Semiconductor Roadmaps [38].

In view of the presented analysis, the very thin film SOI devices are capable of approaching the strength of double gate (GAA) devices in terms of performance and resistance to SCE/DIBL, still being much closer to conventional, planar devices than GAA. Therefore, very thin film SOI may become the dominating technology for below 70 nm CMOS, and SON may be the only viable way of realizing such superthin SOI in practice in a manufacturable way.

REFERENCES


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