**FEATURES**

- 90ns Access Time
- Simple Byte and Page Write
  - Single 5V Supply
  - No External High Voltages or $V_{PP}$ Control Circuits
  - Self-Timed
  - No Erase Before Write
  - No Complex Programming Algorithms
  - No Overerase Problem
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - 16 Byte Page Write Operation
  - Byte or Page Write Cycle: 5ms Typical
  - Complete Memory Rewrite: 640ms Typical
  - Effective Byte Write Cycle Time: 300µs Typical
- **DATA Polling**
  - Allows User to Minimize Write Cycle Time
- JEDEC Approved Byte-Wide Pinout
- High Reliability
  - Endurance: 10,000 Cycles
  - Data Retention: 100 Years

**DESCRIPTION**

The Xicor X2816C is a 2K x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor Programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816C supports a 16-byte page write operation, typically providing a 300µs/byte write cycle, enabling the entire memory to be written in less than 640ms. The X2816C also features DATA Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

**PIN CONFIGURATION**

![PIN CONFIGURATION Diagram](image)
PIN DESCRIPTIONS

Addresses (A₀–A₁₀)
The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable (CE)
The Chip Enable input must be LOW to enable all read/write operations. When CE is HIGH, power consumption is reduced.

Output Enable (OE)
The Output Enable input controls the data output buffers and is used to initiate read operations.

PIN NAMES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A₀–A₁₀</td>
<td>Address Inputs</td>
</tr>
<tr>
<td>I/O₀–I/O₇</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>WE</td>
<td>Write Enable</td>
</tr>
<tr>
<td>CE</td>
<td>Chip Enable</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
</tr>
<tr>
<td>VCC</td>
<td>+5V</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
</tr>
<tr>
<td>NC</td>
<td>No Connect</td>
</tr>
</tbody>
</table>

FUNCTIONAL DIAGRAM
DEVELOPMENT

Read
Read operations are initiated by both OE and CE LOW and WE HIGH. The read operation is terminated by either CE or OE returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either OE or CE is HIGH.

Write
Write operations are initiated when both CE and WE are LOW and OE is HIGH. The X2816C supports both a CE and WE controlled write cycle. That is, the address is latched by the falling edge of either CE or WE, whichever occurs last. Similarly, the data is latched internally by the rising edge of either CE or WE, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation
The page write feature of the X2816C allows the entire memory to be typically written in 640ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any other device in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the WE and CE inputs. That is, A4 through A10 must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the WE HIGH to LOW transition, must begin within 20μs of the falling edge of the preceding WE. If a subsequent WE HIGH to LOW transition is not detected within 20μs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20μs.

DATA Polling
The X2816C features DATA Polling as a method to indicate to the host system that the byte write or page write cycle has completed. DATA Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O7 will reflect true data.

WRITE PROTECTION
There are three features that protect the nonvolatile data from inadvertent writes.

• Noise Protection—A WE pulse which is typically less than 10ns will not initiate a write cycle.
• Vcc Sense—All functions are inhibited when Vcc is ≤3V, typically.
• Write Inhibit—Holding either OE LOW, WE HIGH, or CE HIGH during power-up and power-down, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE
Xicor EPROMs are designed and tested for applications requiring extended endurance.
SYSTEM CONSIDERATIONS

Because the X2816C is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that CE be decoded from the address bus and be used as the primary device selection input. Both OE and WE would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling CE will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between VCC and VSS at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between VCC and VSS for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.
ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X2816C: –10°C to +85°C
- X2816CI: –65°C to +135°C

Storage Temperature: –65°C to +150°C

Voltage on any Pin with Respect to VSS: –1V to +7V

D.C. Output Current: 5mA

Lead Temperature (Soldering, 10 seconds): 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C</td>
<td>+70°C</td>
</tr>
<tr>
<td>Industrial</td>
<td>–40°C</td>
<td>+85°C</td>
</tr>
</tbody>
</table>

Supply Voltage Limits

<table>
<thead>
<tr>
<th></th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>X2816C</td>
<td>5V ±10%</td>
</tr>
</tbody>
</table>

D.C. OPERATING CHARACTERISTICS

(Over recommended operating conditions unless otherwise specified.)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Limits</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>ICC</td>
<td>VCC Current (Active)</td>
<td>70</td>
<td></td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISB1</td>
<td>VCC Current (Standby)</td>
<td>35</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILI</td>
<td>Input Leakage Current</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL(2)</td>
<td>Input LOW Voltage</td>
<td>–1</td>
<td></td>
<td>0.8</td>
</tr>
<tr>
<td>VIL(2)</td>
<td>Input HIGH Voltage</td>
<td>2</td>
<td></td>
<td>VCC +1V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output LOW Voltage</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

Notes:
1. Typical values are for TA = 25°C and nominal supply voltage and are not tested.
2. VIL min. and VIL max. are for reference only and are not tested.
X2816C

ENDURANCE AND DATA RETENTION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Endurance</td>
<td>10,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Retention</td>
<td>100</td>
<td></td>
<td>Years</td>
</tr>
</tbody>
</table>

POWER-UP TIMING

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typ.(1)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPUR(3)</td>
<td>Power-Up to Read Operation</td>
<td>1</td>
<td>ms</td>
</tr>
<tr>
<td>tPUW(3)</td>
<td>Power-Up to Write Operation</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

CAPACITANCE  
$T_A = +25^\circ C, f = 1MHz, V_{CC} = 5V$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_I/O(3)</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>pF</td>
<td>$V_{I/O} = 0V$</td>
</tr>
<tr>
<td>C_IN(3)</td>
<td>Input Capacitance</td>
<td>6</td>
<td>pF</td>
<td>$V_{IN} = 0V$</td>
</tr>
</tbody>
</table>

A.C. CONDITIONS OF TEST

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>0V to 3V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise and Fall Times</td>
<td>5ns</td>
</tr>
<tr>
<td>Input and Output Timing Levels</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

MODE SELECTION

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>Mode</th>
<th>I/O</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Read</td>
<td>DOUT</td>
<td>Active</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Write</td>
<td>D IN</td>
<td>Active</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>Standby and Write Inhibit</td>
<td>High Z</td>
<td>Standby</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
<td>X</td>
<td>Write Inhibit</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Write Inhibit</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS

![Equivalent A.C. Load Circuits Diagram](6612 FHD F22.3)
A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Read Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2816C-90</th>
<th>X2816C-12</th>
<th>X2816C-15</th>
<th>X2816C-20</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>90</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>tCE</td>
<td>Chip Enable Access Time</td>
<td>90</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>90</td>
<td>120</td>
<td>150</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable Access Time</td>
<td>60</td>
<td>60</td>
<td>80</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>tLZ(4)</td>
<td>CE LOW to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tOLZ(4)</td>
<td>OE LOW to Active Output</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>tHZ(4)</td>
<td>CE HIGH to High Z Output</td>
<td>50</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>tOHZ(4)</td>
<td>OE HIGH to High Z Output</td>
<td>50</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>ns</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
</tbody>
</table>

Read Cycle

Notes: (4) tLZ min., tHZ, tOLZ, and tOHZ are periodically sampled and not 100% tested. tHZ max. and tOHZ max. are measured from the point when CE or OE return HIGH (whichever occurs first) to the time when the outputs are no longer driven.
### Write Cycle Limits

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>X2816C-90</th>
<th>X2816C-12,-15,-20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>twC(5)</td>
<td>Write Cycle Time</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Setup Time</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>tCS</td>
<td>Write Setup Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tCH</td>
<td>Write Hold Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tCW</td>
<td>CE Pulse Width</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>tOES</td>
<td>OE HIGH Setup Time</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>tOEH</td>
<td>OE HIGH Hold Time</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>tWP</td>
<td>WE Pulse Width</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>tWPH</td>
<td>WE HIGH Recovery</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid</td>
<td>100</td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup</td>
<td>35</td>
<td>50</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>tDW</td>
<td>Delay to Next Write</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>tBLC</td>
<td>Byte Load Cycle</td>
<td>1</td>
<td>100</td>
</tr>
</tbody>
</table>

**WE Controlled Write Cycle**

**Notes:** (5) $t_{WC}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.
 controlled write cycle

**Notes:**

(6) Between successive byte writes within a page write operation, OE can be strobed LOW: e.g. this can be done with CE and WE HIGH to fetch data from another memory device within the system for the next write; or with WE HIGH and CE LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the CE or WE controlled write cycle timing.
Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

**SYMBOL TABLE**

<table>
<thead>
<tr>
<th>WAVEFORM</th>
<th>INPUTS</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>Must be steady</td>
<td>Will be steady</td>
</tr>
<tr>
<td>---</td>
<td>Changing: State Not Known</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>Don't Care: Changes Allowed</td>
<td></td>
</tr>
<tr>
<td>---</td>
<td>N/A</td>
<td>Center Line is High Impedance</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>May change from LOW to HIGH</td>
<td>Will change from LOW to HIGH</td>
</tr>
<tr>
<td></td>
<td>May change from HIGH to LOW</td>
<td>Will change from HIGH to LOW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>N/A</td>
</tr>
</tbody>
</table>
Normalized Active Supply Current vs. Ambient Temperature

Normalized Standby Supply Current vs. Ambient Temperature

Normalized Access Time vs. Ambient Temperature
PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F03
NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY
PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
PACKAGING INFORMATION

24-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
X2816C

ORDERING INFORMATION

Device

X2816C X X -X

Access Time

-90 = 90ns
-12 = 120ns
-15 = 150ns
-20 = 200ns

Temperature Range
Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C

Package

P = 24-Lead Plastic DIP
J = 32-Lead PLCC
E = 32-Pad LCC
S = 24-Lead Plastic SOIC
**U.S. SALES OFFICES**

**Corporate Office**
Xicor Inc.
1511 Buckeye Drive
Milpitas, CA 95035
Phone: 408/432-8888
Fax: 408/432-0640
E-mail: info@smtpgate.xicor.com

**Northeast Region**
Xicor Inc.
1344 Main Street
Waltham, MA 02154
Phone: 617/899-5510
Fax: 617/899-6808
E-mail: xicor-ne@smtpgate.xicor.com

**Southeast Region**
Xicor Inc.
100 E. Sybelia Ave.
Suite 355
Maitland, FL 32751
Phone: 407/740-8282
Fax: 407/740-8602
E-mail: xicor-se@smtpgate.xicor.com

**Mid-Atlantic Region**
Xicor Inc.
50 North Street
Danbury, CT 06810
Phone: 203/743-1701
Fax: 203/794-9501
E-mail: xicor-ma@smtpgate.xicor.com

**North Central Region**
Xicor Inc.
810 South Bartlett Road
Suite 103
Streamwood, IL 60107
Phone: 708/372-3200
Fax: 708/372-3210
E-mail: xicor-nc@smtpgate.xicor.com

**South Central Region**
Xicor Inc.
11884 Greenville Ave.
Suite 102
Dallas, TX 75243
Phone: 214/669-2022
Fax: 214/644-5835
E-mail: xicor-sc@smtpgate.xicor.com

**Southwest Region**
Xicor Inc.
4100 Newport Place Drive
Suite 710
Newport Beach, CA 92660
Phone: 714/752-8700
Fax: 714/752-8634
E-mail: xicor-sw@smtpgate.xicor.com

**Northwest Region**
Xicor Inc.
2700 Augustine Drive
Suite 219
Santa Clara, CA 95054
Phone: 408/292-2011
Fax: 408/980-9478
E-mail: xicor-nw@smtpgate.xicor.com

**INTERNATIONAL SALES OFFICES**

**EUROPE**

**Northern Europe**
Xicor Ltd.
Grant Thornton House
Witan Way
Witney
Oxford OX8 6FE
UK
Phone: (44) 1933.700544
Fax: (44) 1933.700533
E-mail: xicor-uk@smtpgate.xicor.com

**Central Europe**
Xicor GmbH
Technopark Neukeferloh
Bretonischer Ring 15
85630 Grasbrunn bei Muenchen
Germany
Phone: (49) 8946.10080
Fax: (49) 8946.05472
E-mail: xicor-gm@smtpgate.xicor.com

**ASIA/PACIFIC**

**Japan**
Xicor Japan K.K.
Suzuki Building, 4th Floor
1-6-8 Shinjuku, Shinjuku-ku
Tokyo 160, Japan
Phone: (81) 3322.52004
Fax: (81) 3322.52319
E-mail: xicor-jp@smtpgate.xicor.com

**Mainland China**
Taiwan/Hong Kong
Xicor Inc.
4100 Newport Place Drive
Suite 710
Newport Beach, CA 92660
Phone: 714/752-8700
Fax: 714/752-8634
E-mail: xicor-sw@smtpgate.xicor.com

**Singapore/Malaysia/India**
Xicor Inc.
2700 Augustine Drive
Suite 219
Santa Clara, CA 95054
Phone: 408/292-2011
Fax: 408/980-9478
E-mail: xicor-nw@smtpgate.xicor.com

**Korea**
Xicor Korea
27th Fl., Korea World Trade Ctr.
159, Samsung-dong
Kangnam Ku
Seoul 135-729
Korea
Phone: (82) 2551.2750
Fax: (82) 2551.2710
E-mail: xicor-ka@smtpgate.xicor.com

( ) = Country Code

**Xicor product information is available at:**

http://www.xicor.com