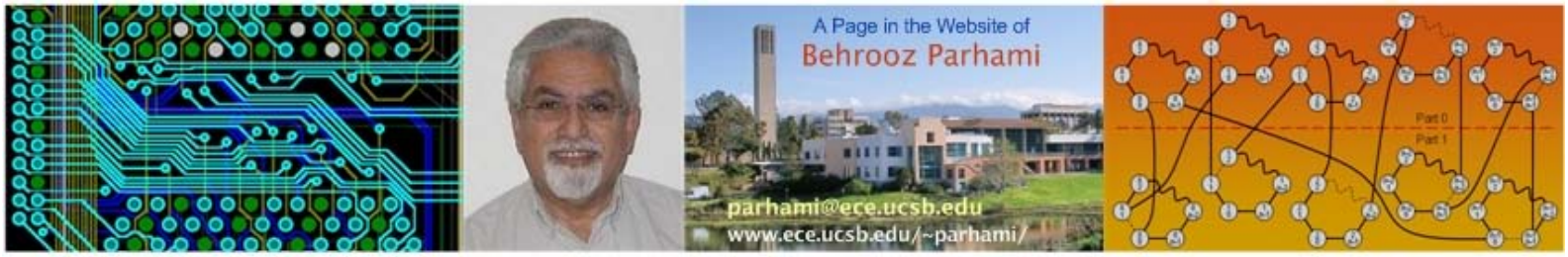
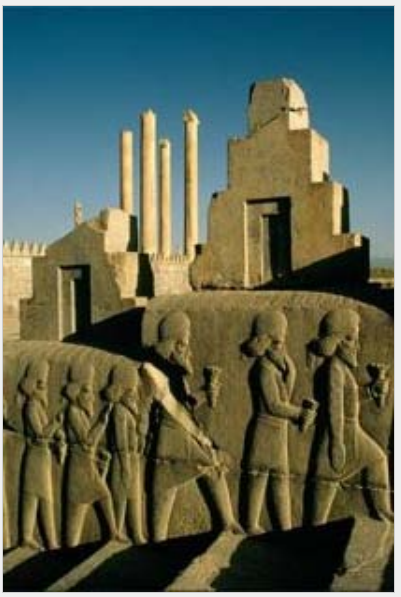


- Home & Contact
- Curriculum Vitae
- Research
  - Computer arithmetic
  - Parallel processing
  - Fault tolerance
  - Broader research
  - Research history
  - List of publications
- Teaching
  - ECE1 Freshman sem
  - ECE154 Comp arch
  - ECE252B Comp arith
  - ECE252C Adv dig des
  - ECE254B Par proc
  - ECE257A Fault toler
  - Student supervision
  - Math + Fun!
- Textbooks
  - Computer arithmetic
  - Parallel processing
  - Dependable comp
  - Comp architecture
  - Other books
- Service
  - Professional activities
  - Academic service
  - Community service
  - Industrial consulting
- Files & Documents
- Useful Links
- Personal

Behrooz Parhami's ECE 154 Course Page for Winter 2009

Introduction to Computer Architecture



Enrollment code: Determined by the discussion session choice
Prerequisite: ECE 152A or equivalent
Class meetings: MW 3:30-4:45, HSSB 1174
Discussion option 1: F 10:00-10:50 (TA1, code 10793), Phelps 3519
Discussion option 2: F 11:00-11:50 (TA2, code 10801), Bldg 387 Rm 103
Discussion option 3: F 12:00-12:50 (TA2, code 10819), Girvetz 1115
Instructor: Professor Behrooz Parhami
Teaching assistant 1: Pradeep Koulgi, pskoulgi at umail.ucsb.edu
Teaching assistant 2: Di-an Li, zstarstu at googlemail.com
Intructor's office hours: MW 12:30-1:50, HFH 5155
TA1's office hours: TR 11:00-1:00, Phelps 1435
TA2's office hours: R 1:30-3:30, Phelps 1435
Course announcements: Listed in reverse chronological order
Course calendar: Schedule of lectures, homework, and exams
Homework assignments: Five assignments, worth a total of 20%
Exams: Two midterms (20% each) and a final (40%), all closed-book
References: Textbook and other info sources (**Textbook's web page**)
Lecture slides: Available on the textbook's web page
Miscellaneous information: Motivation, catalog entry, history

Course Announcements

2009/03/24: Grades for this course have been submitted and the course is officially over. Regarding why our classroom door was locked at the time of the final exam, causing a significant delay in starting the exam, the Registrar's Office is said to be investigating.
2009/03/13: Our final exam will be held on Saturday 3/21, 12:00-2:30 PM, in HSSB 1174. During the finals week (3/16-20), the instructor will keep his regular office hours and will convert the usual class hours (MW 3:30-4:45) into additional office hours. Di-an Li has also agreed to keep all three TA office hours. If you have not received solutions to HW5, please see us during these office hours.
2009/03/10: Welcome to the new web page for ECE 154. The problems mentioned in the next item below have now been resolved. Please help debug this new version of the web page by reporting any errors to the instructor.
2009/03/09: Due to transition to a revamped website, it appears that the ECE 154 web page has been damaged, so that parts of the contents near the end of the page are invisible with Mozilla Firefox, while appearing okay with Internet Explorer. Please e-mail me if you have any problems with other browsers. While the problem is being fixed, please access the course web page with Internet Explorer to see the entire contents.

2009/03/02: HW5 (last one for the course) has been posted below. All lecture slides have now been updated for the current quarter.
2009/02/19: Updated versions of lecture slides for Parts IV and V of the textbooks, as well as grade stats for HW3, have been posted.
2009/02/11: HW4 has been posted below. This homework assignment is very important, because the entire second midterm exam (on M 2/23) will be based on it.
2009/02/03: Due to the overlap with preparations for our first midterm exam, the due date for HW3 has been changed to 10:00 AM on M 2/9 (no further extension is possible; also, be aware that the deadline for HW4 cannot be extended). Updated lecture slides for Part IV of the textbook, as well as samples for MT2 and final

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exam, have been posted.
2009/01/28: HW3 has been posted below.
2009/01/26: Sample midterm problems have been posted below. Updated presentation files for Part III of the textbook are now available from the textbook's website.
2009/01/23: HW2 has been posted below, two days later than originally planned (due to some technical problems). It will still be due on F 1/30. The homework has been made shorter, by removing some problem parts, to compensate for the tighter deadline.
2009/01/16: As stated in class, homework will be due at 10:00 AM (instead of 9:00 AM) on the due date. Besides depositing your homework paper in the box in Room 3120 HFH, you have the option of turning it in to the TA in the first discussion session that begins at 10:00 AM, but you have to do it at the very beginning of the session (no homework will be accepted after 10:00 AM). Remember that you have at least 9 days to work on each homework assignment. So, arriving late at the discussion session is not a valid excuse for missing the deadline.
2009/01/12: HW1 has been posted below. Presentations for Part II of the textbook (chapters 5-8 on instruction set architecture) have been updated and posted to the text's website. Please note that completed course survey forms and pretests are due by Wednesday 1/14 in class. The following students have not turned in their pretests (P) and/or surveys (S) -- Chohan (P); Dasko (PS); Foster (PS); Hildred (PS); Ngo (P); Rhazali (PS); Yeh (PS).
2009/01/06: Updated slides for Part I of the textbook have been posted. Remember to turn in your pretest paper, with the course survey form stapled at the top, to the ECE 154 homework box (in HFH 3120) by 9:00 AM on Friday 1/9.
2008/12/24: Welcome to the ECE 154 website for winter 2009. The following information is now final. Updates will appear at least once a week. Major changes and additions will be outlined in this announcement area.

Course Calendar

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. About half of the lectures have been marked as important or very important. These lectures cover key concepts that constitute the core of ECE 154. The course syllabus follows the calendar below. PowerPoint and pdf files of course lectures can be found on the **Textbook's web page**.

Day & Date (book chapters) Lecture/discussion topic [Homework posted/due] {Special notes}
M 01/05 (ch. 1-3) Course intro, review of logic circuits and computer technology {Pretest & intro survey}
W 01/07 (ch. 4) Computer performance {Very important lecture}
F 01/09 (ch. 1-3) Discussion on logic circuits and computer technology {Pretest and intro survey due}

M 01/12 (ch. 5-6) MiniMIPS instructions and addressing modes
W 01/14 (ch. 6-7) MiniMIPS (cont.) and assembly programs [HW1 posted, ch. 3-4]
F 01/16 (ch. 4) Discussion on computer performance and pretest

M 01/19 *No lecture: Martin Luther King Jr. Holiday*
W 01/21 (ch. 8) ISA variations, RISC, CISC, and URISC [HW2 posted, ch. 5-8]
F 01/23 (ch. 5-8) Discussion on ISA variations and HW1 [HW1 due] {Sample MT1 posted}

M 01/26 (ch. 9-10) Number representation and addition circuits
W 01/28 (ch. 10-11) ALUs, multiplication, and division [HW3 posted, ch. 9-11] {Important lecture}
F 01/30 (ch. 9-11) Discussion on computer arithmetic and HW2 [HW2 due]

M 02/02 (ch. 4-11) First midterm exam, in our regular classroom (closed-book)
W 02/04 (ch. 13) Stages of instruction execution {Important lecture}
F 02/06 (ch. 4-11) Discussion on MT1 and HW3 [HW3 due; extension granted] {Sample MT2 posted}

M 02/09 (ch. 14) Control unit synthesis [HW3 extended deadline] {Important lecture}
W 02/11 (ch. 15) Pipelined data paths [HW4 posted] {Important lecture}
F 02/13 (ch. 13-14) Discussion on data path and control

M 02/16 *No lecture: President's Day Holiday*
W 02/18 (ch. 16) Pipeline performance limits {Important lecture}

F 02/20 (ch. 15-16) Discussion on pipelining and HW4 [HW4 due]

M 02/23 (ch. 13-16) Second midterm exam, in our regular classroom (closed-book)
W 02/25 (ch. 17, 19) Main and mass memory concepts
F 02/27 (ch. 17, 19) Discussion on memory systems

M 03/02 (ch. 18) Cache memory [HW5 posted, ch. 17-20] {Very important lecture}
W 03/04 (ch. 20) Virtual memory and paging
F 03/06 (ch. 18, 20) Discussion on cache and virtual memory

M 03/09 (ch. 21-22) Input/output devices and programming {Sample final exam posted}
W 03/11 (ch. 23-24) Buses, interfacing, and interrupts {Instructor and course evaluation survey}
F 03/13 (ch. 21-24) Discussion on I/O, buses, interrupts, and HW5 [HW5 due]

Sat 03/21 (ch. 4-24) Final exam, 12:00-3:00 PM, HSSB 1174 (closed-book)
T 03/24 {Grades to be submitted by midnight}

Homework Assignments

-Deposit solutions in ECE 154 homework box (3120 HFH) before 10:00 AM on due date.
-Because solutions will be handed out on the due date, no extension can be granted.
-Use a cover page that includes your name, course name, and assignment number.
-Staple the sheets and write your name on top of each sheet in case they are separated.
-Although some cooperation is permitted, direct copying will have severe consequences

Take-Home Pretest: Prerequisites and probability (due F 2009/01/09, 10:00 AM)
This pretest, handed out in class on Monday 1/5/2009, provides you and the instructor with feedback about preparations for ECE 154. You should answer each question on a separate sheet, then staple everything together, using the question sheet as a cover page. The question sheet has a box in which you should make a unique mark or drawing that would allow you to recognize and retrieve your test paper. Papers will be graded anonymously, so please answer each question to the best of your ability, without help from any source, including TAs. To ensure that you are credited with handing in the pretest, staple the completed introductory survey, containing your name and Perm number, to the pretest (to be removed before grading). If you missed the first class, please ask the instructor or one of the TAs for the pretest and introductory course survey. Aggregate scores will be reported below after the pretest has been graded.

Homework 1: Computer technology and performance (ch. 3-4, due F 2009/01/23, 10:00 AM)
Do the following problems from the textbook (20 points each): 3.14, 4.2, 4.11, 4.16, 4.A (defined below)

Problem 4.A Performance and MIPS rating
Consider two different implementations M1 and M2 of the same instruction set. There are three classes of instructions (A, B, and C) in the instruction set. M1 has a clock rate of 1 GHz. M2's clock rate is 1.5 GHz. The average number of clock cycles per instruction for each instruction class of M1 and M2 is as follows:
Class A: CPI for M1 = 2, CPI for M2 = 2
Class B: CPI for M1 = 1, CPI for M2 = 2
Class C: CPI for M1 = 3, CPI for M2 = 4
a. If the number of instructions executed in a certain program is divided equally among the three classes, which machine is faster and by what factor?
b. We can redesign M2 so that the class-C CPI improves from 4 to 2 (class-A and class-B CPIs will still be 2). This change, however, forces a reduction of the clock rate from 1.5 GHz to 1.2 GHz. What minimum percentage of class-C instructions is needed in an instruction mix for this redesign to yield improved performance over the original M2?

Homework 2: Assembly language and ISA variations (ch. 5-8, due F 2009/01/30, 10:00 AM)
Do the following problems from the textbook (20 points each): 5.5, 5.18ab, 6.8a, 7.3abc, 8.10

Homework 3: Computer arithmetic (ch. 9-11, due F 2009/02/06, 10:00 AM) [ext. to M 2/9]
Do the following problems from the textbook (20 points each): 9.4ab, 9.14cd, 10.11, 10.16, 11.6ae

Homework 4: Data path design and control unit (ch. 13-16, due F 2009/02/20, 10:00 AM)
Do the following problems from the textbook (20 points each): 13.2b, 13.6, 14.3ab, 15.7ab, 16.5a

Homework 5: Memory system design (ch. 17-20, due F 2009/03/13, 10:00 AM)
Do the following problems from the textbook (20 points each): 17.4, 18.2, 18.4ad, 19.9ab, 20.6b

Suggested Problems: I/O, buses, and interrupts (ch. 21-24, for practice only, not to be turned in)
Do the following problems from the textbook: 21.8, 21.9 [Correction: Example 21.2 is intended], 22.1, 22.5, 22.9, 23.4, 24.2, 24.11

Sample Exams and Study Guide

The following sample exams are meant to indicate the types and levels of problems, rather than the coverage (which is outlined in the course calendar). Students must study any section or topic that is not specifically excluded in the study guide that follows the sample exams, even if the material was not covered in class lectures. The final exam will also cover the midterm material, but to a lesser degree.

Sample Midterm 1
Problem 1 [15 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [3 points each]: Decoder; PC-relative addressing; Pseudoinstruction; Assembler directive; Biased number representation.
Problem 2 [25 points]: Problem 4.4 in the textbook.
Problem 3 [15 points]: Problem 4.6a in the textbook.
Problem 4 [20 points]: Can you replace the following sequence of MiniMIPS instructions with fewer instructions, without changing the functionality? Explain your answer fully. Assume that the values computed in $t0 and $t1 are temporaries that are not needed elsewhere in the program (Table 6.2 will be provided as reference with problems such as this one):
and $t0,$s0,$s1
or $t1,$s1,$s0
beq $t0,$t1,label
Problem 5 [25 points]: In Fig. 10.19 (provided), explain each of the following:
a. Why the overflow signal is formed by an XOR gate.
b. The role of the *k* XOR gates on the input side of the adder.
c. The total number of control signals supplied to the ALU (show how computed).
d. Why the shifter and logic unit are likely to be faster than the adder.

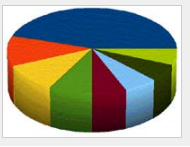
Sample Midterm 2
Problem 1 [20 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [4 points each]: Data forwarding; Loop unrolling; Microprogramming, Optimal pipelining; Pipeline data dependency.
Problem 2 [20 points]: Problem 13.1a in the textbook.
Problem 3 [20 points]: Problem 14.12a in the textbook.
Problem 4 [20 points]: Problem 15.2 in the textbook.
Problem 5 [20 points]: Problem 16.2 in the textbook.

Sample Final Exam
Problem 1 [10 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [2 points each]: Bus arbitration; Conflict miss; Delayed branch; Set-associative cache; TLB
Problem 2 [15 points]: Problem 4.7 in the textbook.
Problem 3 [15 points]: Problem 11.5 in the textbook.
Problem 4 [15 points]: Problem 14.2c in the textbook.
Problem 5 [15 points]: Problem 16.9ab in the textbook.
Problem 6 [15 points]: Problem 18.3c in the textbook.
Problem 7 [15 points]: Problem 20.4a in the textbook.

Midterm and Final Exam Study Guide
The following includes topics that will be emphasized in the course exams, as well as excluded topics.

[Chapters 1-3] No direct problem or question, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.
[Chapter 4] Computer performance: Problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.
[Chapters 5-8] Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, and 8.4.
[Chapters 9-11] Computer arithmetic: Problem likely on 2's-complement numbers, number radix conversion, floating-point number formats, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs, basics of multipliers.
[Chapters 13-14] Data path and control: Problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.
[Chapter 15-16] Pipelining: Problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.
[Chapters 17-20] Memory hierarchy: Problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, and 19.6 are excluded.
[Chapters 21-24] Input/output and interfacing: Problem possible on memory-mapped, polled, or interrupt-driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded.
[Chapters 25-28] Advanced architectures: No problem or question.

Grade Statistics



All grades listed are in percent.
Final exam grades: Range = [30, 90], Mean = 77, SD = 8, Median = 68
MT2 grades: Range = [57, 96], Mean = 63, SD = 15, Median = 77
MT1 grades: Range = [48, 99], Mean = 76, SD = 10, Median = 78
HW5 grades: Range = [32, 98], Mean = 79, SD = 15, Median = 97
HW4 grades: Range = [70, 100], Mean = 93, SD = 9, Median = 97
HW3 grades: Range = [15, 91], Mean = 62, SD = 22, Median = 88
HW2 grades: Range = [56, 100], Mean = 86, SD = 11, Median = 88
HW1 grades: Range = [22, 100], Mean = 65, SD = 22, Median = 62
Pretest grades (min, avg, SD, med, max) -- Problem C (0, 44, 26, 60, 85); Problem D (0, 38, 33, 40, 100); Problem P (0, 14, 17, 10, 70); Problem S (0, 38, 27, 40, 90)

References

Required text: B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. Publisher's list price $89.95, UCSB Bookstore price $89.95/new, $67.45/used. **Textbook's web page** contains an errata and lecture slides.

Useful reference (not required): D.A. Patterson and J.L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 4th ed., 2008.

Miscellaneous Information

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in high-performance uniprocessors (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Catalog entry: **154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour*. The

computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

History: Computer architecture is a required subject in the Computer Engineering Program, and it can be taken as an optional subject by students in certain other majors. ECE 154 (Introduction to Computer Architecture) and its equivalent CMPSC 154 are taught throughout the academic year by a number of faculty from the Department of Electrical and Computer Engineering and the Department of Computer Science. The following record of previous offerings includes only those taught by Professor Parhami.

Offerings of ECE 154 from 2000 to 2008 (PDF file)
