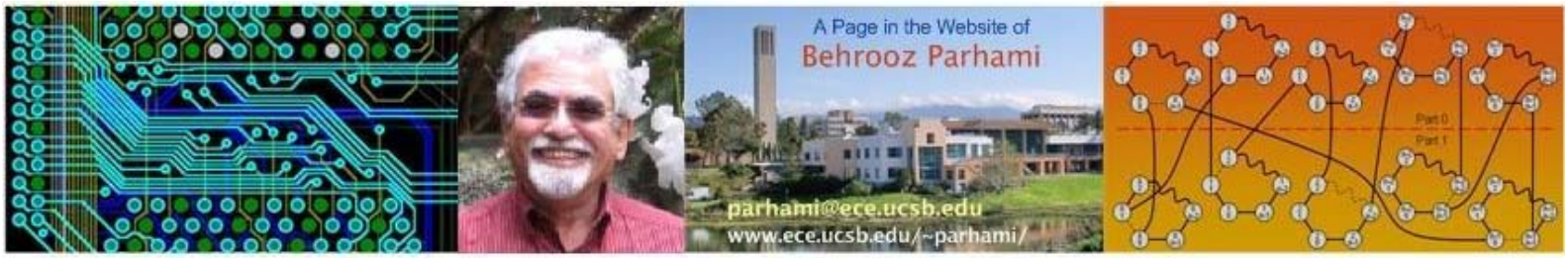
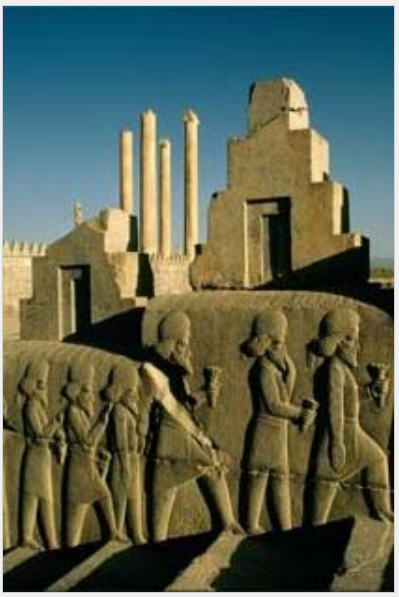


- Home & Contact
- Curriculum Vitae
- Research
  - Computer arithmetic
  - Parallel processing
  - Fault tolerance
  - Broader research
  - Research history
  - List of publications
- Teaching
  - ECE1 Freshman sem
  - ECE154 Comp arch
  - ECE252B Comp arith
  - ECE252C Adv dig des
  - ECE254B Par proc
  - ECE257A Fault toler
  - Student supervision
  - Math + Fun!
- Textbooks
  - Computer arithmetic
  - Parallel processing
  - Dependable comp
  - Comp architecture
  - Other books
- Service
  - Professional activities
  - Academic service
  - Community service
  - Industrial consulting
- Files & Documents
- Useful Links
- Personal

Behrooz Parhami's ECE 154 Course Page for Winter 2011

Introduction to Computer Architecture



Enrollment code: 11452 (11460, 11478, 11486 for discussion sessions)
Prerequisite: ECE 152A or equivalent
Class meetings: TR 9:30-10:45, HSSB 1174
Discussion option 1: F 10:00-10:50 (TA1, code 11460), Phelps 3523
Discussion option 2: F 11:00-11:50 (TA1, code 11478), Phelps 1445
Discussion option 3: F 12:00-12:50 (TA2, code 11486), HSSB 1223
Instructor: Professor Behrooz Parhami
Teaching assistant 1: Jonathan Valamehr, jkv at umail.ucsb.edu
Teaching assistant 2: Amirali Ghofrani, ghofrani at umail.ucsb.edu
Intructor's office hours: M 11:00-12:30, W 12:00-1:30, HFH 5155
TA office hours: TR 18:30-20:30 (TA2), R 14:00-16:00 (TA1), Phelps 1435

Course announcements: Listed in reverse chronological order
Course calendar: Schedule of lectures, homework, and exams
Mandatory pretest and survey: Worth 5% of your grade
Homework assignments: Five assignments, worth a total of 20%
Exams: Two midterms (20% each) and a final (35%), all closed-book
Policy on academic integrity: Please read very carefully
Grade statistics: Range, mean, etc. for homework and exam grades
References: Textbook and other info sources (**Textbook's web page**)
Lecture slides: Available on the textbook's web page
Miscellaneous information: Motivation, catalog entry, history

Course Announcements

2011/03/20: course grades have been submitted to the registrar's office and this offering of ECE 154 is officially over. If you need to take a look at your final exam, or collect previous homework and mideterm papers, please see me during the first two weeks of the spring quarter (M 11:00-12:30, W 12:00-1:30). Have an enjoyable spring break!
2011/03/08: Our closed-book final exam will be held 8:30-11:00 AM on W 3/16 in our regular classroom. During the finals week, the following office hours are in effect: M 3/14, 11:00-12:30 (BP); T 3/15, 9:30-11:30 (BP), 2:30-4:30 (JV), 6:30-8:30 (AG)
2011/02/23: Homework 5 (last one for the course) has been posted below. Lecture slides for Part IV of the textbook have been reposted with very minor "cosmetic" corrections. Midterm 2 grade stats will be posted by F 2/25.
2011/02/07: Homework 4 has been posted below. Midterm 2, covering Chs. 13-16 only, will be held on T 2/22. Homework 3 grade stats will be posted shortly.
2011/02/01: Grades for MT1 will be available by F 2/4. Updated slides for Part IV of the textbook have been posted to the textbook's Web page.
2011/01/27: Please note an added clarification and a correction to Homework 3.
2011/01/25: Homework 3 has been posted below. Midterm 1 will be held on T 2/1.
2011/01/18: Homework 2 has been posted below. Updated slides for Parts II and III of the textbook are available from the textbook's Web page. Please note that the TA office hours have changed (TR 2:00-4:00 PM has shifted to TR 6:30-8:30 PM).
2011/01/11: Homework 1 and stats for pretest grades have been posted below. Updated slides for Part I of the textbook are available from the textbook's Web page. Part II slides will be updated by Friday 1/14.
2010/12/04: Welcome to the ECE 154 Web site for winter 2011. The following information is tentative and is

Blog & books
Favorite quotations
Poetry
Pet peeve
Virtual retirement
CE Program
ECE Department
UCSB Engineering
UC Santa Barbara

provided for planning purposes only. The course lecture schedule and requirements will be finalized in late December 2010, with updates appearing at least weekly thereafter. Major changes and additions to the page content will be outlined in this announcements area.

Course Calendar

Course lectures, homework assignments, and exams have been scheduled as follows. This schedule will be strictly observed. About half of the lectures have been marked as important or very important. These lectures cover key concepts that constitute the core of ECE 154. The course syllabus follows the calendar below. PowerPoint and pdf files of course lectures can be found on the **Textbook's web page**.

Day & Date (book chapters) Lecture/discussion topic [Homework posted/due] {Special notes}
T 01/04 (ch. 1-2) Course introduction, review of logic circuits
R 01/06 (ch. 3) Computer technology {Mandatory pretest and background survey}
F 01/07 (ch. 1-3) Discussion on logic circuits, computer technology, and pretest

T 01/11 (ch. 4) Computer performance {Very important lecture}
R 01/13 (ch. 5-6) MiniMIPS instructions and addressing modes [HW1 posted, ch. 3-4]
F 01/14 (ch. 4) Discussion on computer performance

T 01/18 (ch. 7-8) Assembly programs and ISA variations
R 01/20 (ch. 9) Number representation [HW2 posted, ch. 5-8]
F 01/21 (ch. 5-8) Discussion on instruction-set architecture and HW1 [HW1 due]

T 01/25 (ch. 10) Addition circuits and simple ALUs
R 01/27 (ch. 11) Multiplication and division [HW3 posted, ch. 9-11] {Important lecture}
F 01/28 (ch. 9-11) Discussion on computer arithmetic and HW2 [HW2 due]

T 02/01 (ch. 4-11) First midterm exam, in our regular classroom (closed-book)
R 02/03 (ch. 13) Stages of instruction execution {Important lecture}
F 02/04 (ch. 4-11) Discussion on MT1 and HW3 [HW3 due]

T 02/08 (ch. 14) Control unit synthesis {Important lecture}
R 02/10 (ch. 15) Pipelined data paths [HW4 posted, ch. 13-16] {Important lecture}
F 02/11 (ch. 13-14) Discussion on data path and control

T 02/15 (ch. 16) Pipeline performance limits {Important lecture}
R 02/17 (ch. 17, 19) Main and mass memory concepts
F 02/18 (ch. 15-16) Discussion on pipelining and HW4 [HW4 due]

T 02/22 (ch. 13-16) Second midterm exam, in our regular classroom (closed-book)
R 02/24 (ch. 18) Cache memory [HW5 posted, ch. 17-20] {Very important lecture}
F 02/25 (ch. 17-18) Discussion on main & cache memories and MT2

T 03/01 (ch. 20) Virtual memory and paging
R 03/03 (ch. 21-22) I/O devices and programming
F 03/04 (ch. 19-20) Discussion on mass & virtual memories and HW5 [HW5 due]

T 03/08 (ch. 23-24) Buses, interfacing, and interrupts {Instructor and course evaluation survey?}
R 03/10 (Ch. 25) Road to Higher Performance
F 03/11 (ch. 21-24) Discussion on I/O, buses, interrupts

W 03/16 (ch. 4-24) Final exam, 8:30-11:00 AM, HSSB 1174 (closed-book)
T 03/22 {Grades to be submitted by midnight}

Mandatory Pretest and Survey

A pretest and student background survey, distributed and collected in class, provides the instructor with information about your background and preparations for ECE 154. A small portion of your grade (5%) will be

determined by the pretest and student background survey, to ensure that you try your best to provide complete and accurate answers. The pretest will contain one problem each from the material in Chapters 1 and 2 of the textbook, plus one problem each from probability/statistics and discrete mathematics (combinatorics). The latter two are exemplified by the following problems.

Probability/statistics problem: During World War II, a hypothetical city laid out as a 10-by-10 grid of equal size blocks was hit by 200 randomly dropped bombs. Thus, the probability of any particular bomb hitting a specific city block was 1/100 and each block was hit by an average of 2 bombs. Find the probability of a given city block not being hit at all.

Discrete mathematics problem: There are 20 people in a group, represented as vertices of a graph. An edge exists in the graph between person *i* and person *j* if the two are friends. Therefore, each edge represents a friendship and the number of edges indicates the total number of friendships. What is the maximum possible number of friendships if we know that the graph is bipartite, that is, the group can be divided into disjoint subsets *A* and *B* such that every friendships is between a person in *A* and a person in *B*?

Homework Assignments

-Deposit solutions in ECE 154 homework box (3120 HFH) before 10:00 AM on due date.
-Because solutions will be handed out on the due date, no extension can be granted.
-Use a cover page that includes your name, course name, and assignment number.
-Staple the sheets and write your name on top of each sheet in case they are separated.
-Some cooperation is permitted, but direct copying of work will have severe consequences.

Homework 1: Computer technology and performance (ch. 3-4, due F 1/21, 10:00 AM)
Do these textbook problems: 3.16 [20 pts.], 4.6 [20 pts.], 4.9 [20 pts.], 4.17 [15 pts.], 4.20 [25 pts.]

Homework 2: Machine instructions and ISA variations (ch. 5-8, due F 1/28, 10:00 AM)
Do these textbook problems: 5.11 [15 pts.], 6.9ab [20 pts.], 7.2a-e [25 pts.], 7.4ab [20 pts.], 8.12 [20 pts.]a
Correction to Problem 8.12: On the next to last line, "f_sub_i squared" should be "square root of f_sub_i."

Homework 3: Computer arithmetic (ch. 9-11, due F 2/4, 10:00 AM)
Do these textbook problems: 9.1abc [15 pts.], 9.12ac [15 pts.], 10.8a [15 pts.], 10.12ab [20 pts.], 11.2ab [20 pts.], 11.11 [15 pts.]
Clarification on Problem 9.12: Each of the parts a and c lists 3 numbers, with the third one appearing on two lines, owing to a line break.
Correction to Problem 10.12: Change the beginning of the problem's introduction to: "Consider a 24-bit carry network built by cascading 6 copies ...". Change part b to: "Show that using the block widths 3, 4, 5, 5, 4, 3, rather than 4, 4, 4, 4, 4, 4, leads to a faster carry network."

Homework 4: Data path design and control unit (ch. 13-16, due F 2/18, 10:00 AM)
Do these textbook problems: 13.1b [10 pts.], 13.7 [20 pts.], 14.9 [20 pts.], 15.6e [20 pts.], 15.12 [10 pts.], 16.10ab [20 pts.]
Clarification on Problem 15.6e: Consistent with the coverage of Chapter 15, assume no data forwarding.

Homework 5: Memory system design (ch. 17-20, due F 3/4, 10:00 AM)
Do these textbook problems: 17.2 [15 pts.], 18.4ad [20 pts.], 18.8 [15 pts.], 19.9 [15 pts.], 20.3 [15 pts.], 20.12b [20 pts.]

Suggested Problems: I/O, buses, and interrupts (ch. 21-24, for practice only, not to be turned in)
Do the following problems from the textbook: 21.8, 21.9 [Correction: Example 21.2 is intended], 22.1, 22.5, 22.9, 23.4, 24.2, 24.11

Sample Exams and Study Guide

The following sample exams are meant to indicate the types and levels of problems, rather than the coverage (which is outlined in the course calendar). Students must study any section or topic that is not specifically excluded in the study guide that follows the sample exams, even if the material was not covered in class lectures. The final exam will also cover the midterm material, but to a lesser degree.

Sample Midterm 1

Problem 1 [15 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [3 points each]: Decoder; PC-relative addressing; Pseudoinstruction; Assembler directive; Biased number representation.
Problem 2 [25 points]: Problem 4.4 in the textbook.
Problem 3 [15 points]: Problem 4.6a in the textbook.
Problem 4 [20 points]: Can you replace the following sequence of MiniMIPS instructions with fewer instructions, without changing the functionality? Explain your answer fully. Assume that the values computed in $t0 and $t1 are temporaries that are not needed elsewhere in the program (Table 6.2 will be provided as reference with problems such as this one):
and $t0,$s0,$s1
or $t1,$s1,$s0
beq $t0,$t1,label
Problem 5 [25 points]: In Fig. 10.19 (provided), explain each of the following:
a. Why the overflow signal is formed by an XOR gate.
b. The role of the *k* XOR gates on the input side of the adder.
c. The total number of control signals supplied to the ALU (show how computed).
d. Why the shifter and logic unit are likely to be faster than the adder.

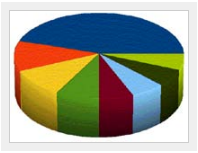
Sample Midterm 2
Problem 1 [20 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [4 points each]: Data forwarding; Loop unrolling; Microprogramming, Optimal pipelining; Pipeline data dependency.
Problem 2 [20 points]: Problem 13.1a in the textbook.
Problem 3 [20 points]: Problem 14.12a in the textbook.
Problem 4 [20 points]: Problem 15.2 in the textbook.
Problem 5 [20 points]: Problem 16.2 in the textbook.

Sample Final Exam
Problem 1 [10 points]. Defining concepts and terms -- Define each of the following concepts/terms precisely and concisely within the space provided (about 1.5 inches per term) [2 points each]: Bus arbitration; Conflict miss; Delayed branch; Set-associative cache; TLB
Problem 2 [15 points]: Problem 4.7 in the textbook.
Problem 3 [15 points]: Problem 11.5 in the textbook.
Problem 4 [15 points]: Problem 14.2c in the textbook.
Problem 5 [15 points]: Problem 16.9ab in the textbook.
Problem 6 [15 points]: Problem 18.3c in the textbook.
Problem 7 [15 points]: Problem 20.4a in the textbook.

Midterm and Final Exam Study Guide
The following includes topics that will be emphasized in the course exams, as well as excluded topics.
[Chapters 1-3] No direct problem or question, but you need to know (and be able to define) concepts such as tristate buffers, multiplexers, register files, and so on, used to explain the topics that follow.
[Chapter 4] Computer performance: Problem likely on CPI calculation, performance enhancement (Amdahl's law), instruction mix, and/or benchmarks.
[Chapters 5-8] Instruction-set architecture: You do not need to memorize instruction codes or formats. Any problem in this area will be accompanied by a reference table providing a list of codes and formats if required. Ignore Sections 7.5, 7.6, and 8.4.
[Chapters 9-11] Computer arithmetic: Problem likely on 2's-complement numbers, number radix conversion, floating-point number formats, shift/logical operations (including distinction between arithmetic and logical shifts), adders and ALUs, basics of multipliers.
[Chapters 13-14] Data path and control: Problem very likely on control unit structure, control signal generation, multicycle instruction execution, and control state machine. Section 14.5 is excluded.
[Chapter 15-16] Pipelining: Problem very likely on pipeline bubbles (how to insert or avoid them), pipeline control, data hazards, data forwarding, control hazards, delayed branch, and/or branch prediction.
[Chapters 17-20] Memory hierarchy: Problem very likely on the need for memory hierarchy, cache memory concepts (levels 1 and 2), miss/hit rate, average memory access time, compulsory/capacity/conflict misses, mapping schemes, virtual memory, page table, and/or TLB. Sections 17.5, 19.5, and 19.6 are excluded.
[Chapters 21-24] Input/output and interfacing: Problem possible on memory-mapped, polled, or interrupt-

driven I/O, buses, and interrupts. Sections 21.5, 21.6, 22.6, 23.5, 23.6, 24.5, and 24.6 are excluded. [Chapters 25-28] Advanced architectures: No problem or question.

Grade Statistics



Grades listed are in percent, unless otherwise noted.
Pretest grades (min, mean, SD, med, max): Problem L (15, 43, 12, 50, 50) out of 50; Problem P (0, 27, 12, 30, 50) out of 50; Total (35, 71, 18, 75, 100)
HW1 grades: Range = [20, 100], Mean = 65, SD = 24, Median = 68
HW2 grades: Range = [43, 100], Mean = 82, SD = 13, Median = 83
HW3 grades: Range = [33, 97], Mean = 71, SD = 19, Median = 74
HW4 grades: Range = [48, 100], Mean = 89, SD = 14, Median = 94
HW5 grades: Range = [20, 89], Mean = 62, SD = 19, Median = 65
Midterm 1 grades: Range = [14, 99], Mean = 66, SD = 22, Median = 70
Midterm 2 grades: Range = [17, 93], Mean = 56, SD = 18, Median = 58
Final exam grades: Range = [22, 83], Mean = 57, SD = 16, Median = 60

References

Required text: B. Parhami, *Computer Architecture: From Microprocessors to Supercomputers*, Oxford University Press, 2005. **Textbook's web page** contains an errata and lecture slides. Many online bookstores offer a better price for this textbook than our campus bookstore.
Useful references (not required): D. A. Patterson and J. L. Hennessy, *Computer Organization & Design: The Hardware/Software Interface*, Morgan Kaufmann, 4th ed., 2008.
W. Stallings, *Computer Organization and Architecture*, Prentice Hall, 8th ed., 2010.

Miscellaneous Information

Motivation: Computer architecture is the study/specification of (digital) computer systems at the interface of hardware and software. Computer architecture is driven from the software side by user needs in terms of functions and speed and from the hardware side by technological innovations and constraints. ECE 154 introduces you to this exciting field and makes you an informed computer user who understands basic architectural features as well as their cost/performance implications. The programmer's view of the instruction set and user interface are considered along with memory organization, addressing methods, input/output, implementation of control, and a multitude of performance issues and computation speedup methods. ECE 154 also prepares you for participation in computer design efforts and for learning the advanced implementation methods and technologies used in high-performance uniprocessors (ECE 254A), parallel processors (ECE 254B), and distributed systems (ECE 254C).

Catalog entry: **154. Introduction to Computer Architecture. (4) PARHAMI.** *Prerequisite: ECE 152A with a minimum grade of C-; open to EE, computer engineering, and computer science majors only. Not open for credit to students who have completed Computer Science 154. Lecture, 3 hours; discussion, 1 hour*. The computer design space. Methods of performance evaluation. Machine instructions and assembly language. Variations in instruction set architecture. Design of arithmetic/logic units. Data path and control unit synthesis. Pipelining and multiple instruction issue. Hierarchical memory systems. Input/output and interfacing. High-performance systems, including multiprocessors and multicomputers.

History: Computer architecture is a required subject in the Computer Engineering Program, and it can be taken as an optional subject by students in certain other majors. ECE 154 (Introduction to Computer Architecture) and its equivalent CMPSC 154 are taught throughout the academic year by a number of faculty from the Department of Electrical and Computer Engineering and the Department of Computer Science. The following record of previous offerings includes only those taught by Professor Parhami.
Offering of ECE 154 in winter 2011 (PDF file)
Offering of ECE 154 in winter 2010 (PDF file)
Offering of ECE 154 in winter 2009 (PDF file)
Offerings of ECE 154 from 2000 to 2008 (PDF file)