Analog I/O

ECE 153B
Sensor & Peripheral Interface Design
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Introduction

- Anytime we need to monitor or control analog signals with a digital system, we require analog-to-digital (ADC) and digital-to-analog (DAC) conversion

- Examples include:
  - Process control
  - Digital audio and video
  - Interfacing to any type of continuous (vs. discrete) voltage or current
Op - Amps (Operational Amplifiers)

- Op – Amps are the basic building blocks in analog input and output devices
  - Current-to-voltage converters, voltage amplifiers, buffers, active filters, sample-and-holds, etc.

- Characteristics: high gain, two analog signal inputs (inverting and non-inverting), and one or two analog signal outputs

- Often, two DC supply voltages of opposite polarity are required
The Ideal Op – Amp

- Infinite input impedance
  - no current flows into input terminals

- Extremely high open loop gain ($A_{OL}$)
  - typically $10^4$ to $10^6$

- $V_o = A_{OL} (V_+ - V_-)$
  - differential amplifier
Common Op - Amp Circuits

- Because the open loop gain of an op-amp is so high, we generally employ “negative feedback” in circuit design.

- The closed loop gain is (to a first approximation) dictated entirely by the external feedback components.
  - Makes the design of linear circuits using op amps relatively straightforward.
  - Analysis of transfer characteristics accomplished using virtual ground analysis.
Virtual Ground Analysis - Requirements

- A first approximation of the operation of an op amp circuit can be done via virtual ground analysis if:
  - The op amp circuit employs negative feedback
    - Output to $V_-$
  - The op amp has a high open loop gain
  - The output of the op amp is operating in the linear range
    - This restricts the closed loop gain and the input signal range
Virtual Ground Analysis - Assumptions

- Virtual ground analysis allows the following assumptions:
  - $V^+ = V^-$
  - Current ($I$) into either input terminal = 0
    - $I^+ = I^- = 0$

- This allows the elementary circuit laws to be used in analyzing these circuits
  - i.e., Ohm’s and Kirchoff’s
Virtual Ground Analysis

Inverting Voltage Amplifier

- We’ll start with the inverting voltage amplifier
  - This is probably the most common application of an op amp
Virtual Ground Analysis
Inverting Voltage Amplifier

Based on the virtual ground analysis assumptions we know that:
- The input terminals, $V_+ = V_- = GND = 0 \, V$

Since we know that $V_I$ is dropped across $R_1$ (to GND), we also know that:
- the current through $R_1$ is $I = \frac{V_I}{R_1}$.
Virtual Ground Analysis
Inverting Voltage Amplifier

- Now we look at the second virtual ground analysis assumption:
  - $I_-$ (the current into the inverting terminal of the op amp) = 0

- Since the current produced by the voltage drop across $R_1$ has to go somewhere (Kirchoff’s current law), it goes to $V_o$ through $R_F$
  - The output voltage would then be the current through $R_F$ (determined above to be $V_I / R_1$) times its resistance:

  $$V_o = - \left( \frac{V_I}{R_1} \right) R_F = - \left( \frac{R_F}{R_1} \right) V_I$$
Virtual Ground Analysis
Inverting Voltage Amplifier

- The sign inversion is a result of
  - \( V^+ = V^- = \text{GND} = 0 \text{ V} \)

- If \( V_I \) is positive, current flows into the node at \( V^- \) (but not into the \( V^- \) terminal itself), then into \( R_F \) and finally to \( V_o \)
  - Since \( V^- \) is at \( \text{GND} \), \( V_o \) must be a negative voltage assuming conventional current flow ( + to -)

- Conversely, if \( V_I \) is negative
  - Current flows out of the node at \( V^- \) and hence \( V_o \) must be a positive voltage
Virtual Ground Analysis
Inverting Voltage Amplifier

\[ V_o = -\left(\frac{V_I}{R_1}\right) R_F = -\left(\frac{R_F}{R_1}\right) V_I \]
Common Op – Amp Circuits

(a) CURRENT TO VOLTAGE CONVERTER

(b) UNITY GAIN BUFFER

(c) INVERTING VOLTAGE AMPLIFIER

(d) INVERTING SUMMING AMPLIFIER

(e) NONINVERTING AMPLIFIER

(f) INTEGRATOR
Digital-to-Analog Converters (DACs)

- DAC accepts an n-bit parallel digital word as its input and provides an analog current or voltage as its output
  - input can be signed or unsigned positional binary number

- Several types of DAC
  - different topologies, different speeds, different accuracies, different output types (voltage vs. current)
Weighted Resistors into a Summing Junction – DAC Type #1
Weighted Resistors into Summing Junction DAC

- Fast, low precision technique
  - Precision of resistors is critical to overall precision
    - Smaller resistors (more significant bits) require proportionally higher precision resistors (tighter tolerance)
    - Only good for a small number of bits as it becomes impractical to attain the required resistor tolerances

- Switches shown on schematic are actually transistors connected to incoming digital word

- B1 is most significant bit
Weighted Resistors Into Summing Junction DAC

- If input bit is 1, the switch is closed and the current is directed to the summing junction of the op amp
  - Conversely if input bit = 0, the current is directed to ground

\[
V_{OUT} = -I_TR
\]

\[
= -\left(\frac{V_{REF}B_1}{2R} + \frac{V_{REF}B_2}{4R} + \frac{V_{REF}B_3}{8R}\right)R
\]

\[
= -V_{REF}\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8}\right)
\]

\[
= -V_{REF}(B_12^{-1} + B_22^{-2} + B_32^{-3})
\]
Weighted Resistors into Summing Junction DAC

- If \( V_{\text{ref}} \) is 10 volts, the maximum output will be
  - \( 10V \times \frac{7}{8} = -8.75 \text{ V} \)
  - Could add inverting amplifier or DC offset to get positive results

- Step size is full scale value \( (V_{\text{ref}}) \) divided by \( 2^n \) (where \( n \) is the number of bits)
  - Step size for this example is \( 10 / 8 = 1.25 \text{ V} \)
  - This is referred to as the “resolution” of the DAC
    - Resolution is the size of the output step associated with a change of 1 in the least significant bit at the input
R–2R Ladder – DAC Type #2
R–2R Ladder DAC

- Requires only 2 resistor values
  - Solves problem of absolute resistor precision we saw in weighted resistor summing junction DAC
  - Resistors in R–2R ladder DAC have to be precisely matched, but their absolute resistance is not important

- Current into summing junction is the same as in weighted resistor summing junction DAC
R–2R Ladder DAC

- Scale and step size are also the same as scaled resistor DAC (for 3 - bit, 10 V case)

- However, because resistor precision is relative for this design, the DAC can be scaled to many more bits
  - Additional bits provide greater resolution
  - For example:
    - 8 - bit, 10V R–2R ladder DAC provides a step size (resolution) of $10 \text{ V} / 2^8 = 39.06 \text{ mV}$
Scaled Current Sources - DAC Type #3

- DAC0802, for example
Scaled Current Sources DAC

- Generic View

![Diagram of Scaled Current Sources DAC](image)
Scaled Current Sources DAC

- Similar Approach to R–2R Ladder DAC

- Bipolar Junction Transistors (BJTs) eliminate the number of floating nodes in the circuit
  - Reduces parasitic capacitance
  - Increases performance

- BJT emitters are sized to be proportional to the desired emitter current
  - 1x, 2x, 4x, etc.
DAC Interfacing Methods

- Store outgoing digital bit pattern in an external register (outside the processor) and apply the register contents continuously to the DAC inputs
  - Only necessary when DAC used has no internal latches (many do)

- Always some analog details to deal with ...
  - Reference voltage or current
  - Full-scale setting
  - External passive components

- And (as always), when in doubt: read the data sheet
Multiplying DACs (a.k.a. “MDACs”)

- By using the full scale adjust (reference voltage) as an input on some DACs, you can create a “multiplying DAC” or simply an “MDAC”
  - Output = input (reference) voltage * digital code

- Multiplying DACs are often used to implement digital gain control in microprocessor and embedded computer systems
Range of DAC Output

- Terminology
  - Unipolar: output all positive (or all negative)
    - i.e. there is a single power supply
  - Bipolar: output goes both positive and negative
    - signed
    - requires two power supplies

- External op amp circuits can also be used
  - to move range of output voltages up or down
  - to buffer or amplify output
Analog-to-Digital Converters (ADCs)

- Analog-to-Digital converters perform two basic operations
  - Quantization
    - mapping of a continuous signal into one of several possible ranges
  - Coding
    - assignment of a unique binary code to each discrete range
      - Binary, BCD, sign magnitude, 2’s complement, 1’s complement, offset binary, etc.

- Like DACs, there are several types
The Comparator Component

- Fundamental component of any ADC
  - essentially an open loop op amp
  - functions as a 1-bit ADC
    - $V_i$ is input, $V_T$ is threshold voltage

![Comparator Diagram](image)

- $V_i > V_T : V_o = \text{LOGIC 1}$
- $V_i < V_T : V_o = \text{LOGIC 0}$

(a) 5 V

(b) $V_o$ vs $(V_i - V_T)$
Parallel or “Flash” ADC
Parallel or “Flash” ADC

- Input signal is fed to n comparators in parallel

- Each comparator attached to n equally-spaced reference voltages
  - generated by a resistor ladder

- Priority encoder generates a $\log_2 n$ output code
Parallel or “Flash” ADC

- Flash is fastest ADC (parallel)
  - up to ~300 Msps ... perhaps even faster
  - small number of bits
    - usually < 10 due to cost
    - internal componentry grows as $2^n$

- Because of high speed, a sample and hold (S/H) circuit is not necessary
  - S/H is necessary with slower converters
Sample and Hold Circuits

- Needed when analog signal changes faster than the conversion rate of ADC
  - Conversion must take place before the analog input changes ± ½ lsb or result is inaccurate
Successive Approximation ADC

- Generic view

![Diagram of Successive Approximation ADC](image.png)
Successive Approximation ADC

- MCP3002 (from ECE 153B lab experiment)
  - 10-bit conversion
  - 2 input channels
  - On-chip sample and hold
  - Serial Interface
Successive Approximation ADC

- Use a DAC and binary search to find correct conversion of n bits after n conversion steps
  - Slower than flash ADC due to n steps needed for n bits of resolution

- Inputs
  - Vin: voltage to be converted
    - Sample and hold often needed
    - Usually (as in MCP3002) S/H is integrated within the ADC
  - Start: external command to begin conversion
  - Clock: digital clock oscillator
Successive Approximation ADC

- **Outputs**
  - EOC: End of Conversion
  - Data out
    - Data [n-1:0], if parallel output
    - Dout, if serial

- **Conversion (sample) time**
  - 1 µs to 50 µs

- **Accuracy**
  - 8 to 12 bits
Successive Approximation ADC

- **Cost**
  - $5 - $400
    - Cost is based on speed and accuracy

- **Potential issues**
  - unipolar vs. bipolar
  - range
  - sample and hold requirements
  - input impedance
Dual Slope Integrating ADC

- also known as Delta – Sigma (ΔΣ) ADC

![Diagram of Dual Slope Integrating ADC](image-url)
Dual Slope Integrating ADC

- Strategy is to cancel the input current with a switched current source
  - Input drives an integrator whose output is compared with any fixed voltage (e.g., ground)
  - Depending on the comparator’s output, fixed length pulses of current are switched into the summing junction of the integrator at each clock transition
    - Maintains zero average current into summing junction
Dual Slope Integrating ADC

- A counter keeps track of the number of pulses switched to the summing junction for a given number of clocks (e.g., 4096 for a 12-bit ADC)
  - Count is the output (it’s proportional to input level)

- Hardware integrating ADC are typically low-speed devices

- They are also capable of high accuracy at low cost due to minimal analog circuitry