RECENT DEVELOPMENTS IN THE DESIGN AND IMPLEMENTATION OF DIGITAL DECIMATORS, INTERPOLATORS, AND NARROW BAND FILTERS

R. E. Crochiere and L. R. Rabiner
Bell Laboratories
Murray Hill, New Jersey 07974

ABSTRACT

In this paper we discuss a number of issues concerning the design of optimal decimators, and interpolators and their application to narrow band filtering. We show that a design which is optimized for minimum storage is essentially optimum in terms of its number of required multiplications and additions as well. We then discuss a practical scheme for efficiently implementing decimators and interpolators.

I. INTRODUCTION

In the area of digital signal processing, there often arises the need for efficiently converting between different sampling rates. The process of decimating or lowering the sampling rate of a signal x(n) by an integer ratio M is depicted in Fig. 1. The original sampling rate is denoted as f_r and the final sampling rate is f_r/M. To avoid aliasing at the lower sampling rate, f_r/M, it is necessary

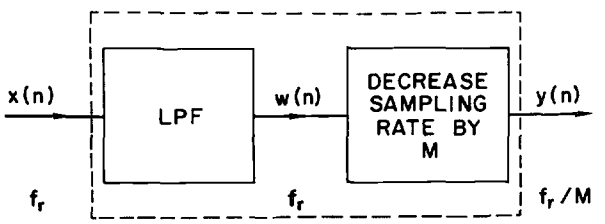

Figure 1: Illustration of the decimation process.

to first filter the original signal x(n) with a lowpass filter whose cutoff frequency is equal to $f_r/(2M)$ giving the signal w(n). The sampling rate reduction is then achieved by forming a new sequence y(n) by extracting every M^{th} sample of w(n).

The process of interpolating a signal x(n) by an integer ratio L is similarly depicted in Fig. 2. In this case the sampling rate of the

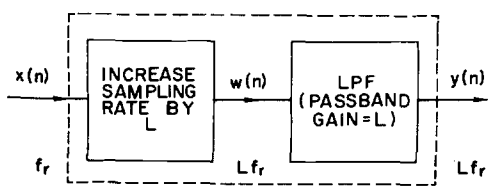

Figure 2: Illustration of the interpolation process.

signal x(n) is increased by the factor L by inserting L-1 zero valued samples between each sample of x(n). This creates a signal w(n) (with sampling rate Lf_r) whose frequency components are periodic in the original sampling frequency f_r. To eliminate these periodic components and retain only the base-band frequencies it is necessary to filter the signal w(n) with a lowpass filter, whose cutoff frequency is $f_r/2$. The resulting signal y(n), with sampling rate Lf_r, is then the desired interpolated signal. It will be assumed in this paper that the above filters are linear phase FIR filters for reasons explained in Refs. 1,2.

II. OPTIMUM DESIGN OF MULTISTAGE DECIMATORS FOR SAMPLING RATE REDUCTION

In Section I a general one-stage technique for changing the sampling rate of a signal was shown. For large changes in sampling rate, however, it is generally more efficient to reduce the sampling rate with a series of decimation stages rather than making the entire rate reduction with one stage. In this way the sampling rate is reduced gradually resulting in much less severe filtering requirements on the lowpass filters at each stage.[3]

The basic multistage process for sampling rate reduction with K stages is illustrated in Fig. 3a and a frequency domain interpretation of this process is given in Fig. 3b.

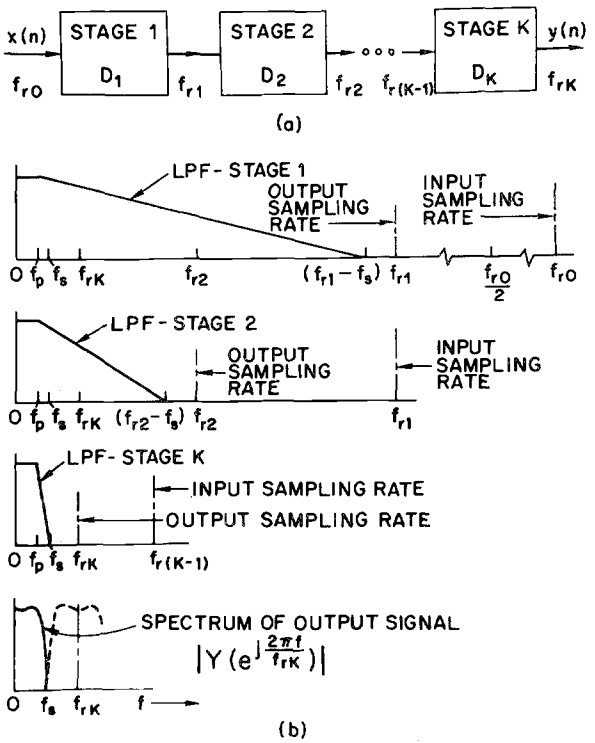

Figure 3: (a) Illustration of a K-stage decimators, and (b) a frequency response interpretation of this process.

The initial sampling rate is f_{r0} and the final sampling rate is f_{rK} with intermediate sampling frequencies designated as $f_{r1}, f_{r2}, \ldots, f_{r(K-1)}$. The sampling rate reduction achieved by each stage is D_i, i=1,2,...,K and the intermediate sampling frequencies are denoted as f_{ri}. The overall sampling rate reduction

achieved by this process is $D = f_{r0}/f_{rK}$. From the sampling theorem, we recognize that the highest frequency in y(n) is $f_s \leq f_{rK}/2$. The passband of the filters in each stage extends from 0 to f_p, where $f_p < f_s$, and the overall passband tolerance is $1 \pm \delta_p$. The stop band tolerance is δ_s.

Thus far, we have established the basic framework for a multistage decimator. Given that the parameters f_{r0}, f_s, f_p, δ_p and δ_s are known, the next consideration is that of optimizing the design for maximum efficiency. The parameters that we have at our disposal are K, and D_i, i = 1,2,...,K. The function to be minimized can be either the total computation, R_T, or the total storage, N_T, of the design. It can be shown that they are of the forms

$$R_T \cong F_0\left(\frac{\delta_p}{K},\delta_s\right)\cdot S(f_p,f_s,K,D_1,D_2,\ldots,D_K)\cdot f_{r0} \quad (1)$$

and

$$N_T \cong F_0\left(\frac{\delta_p}{K},\delta_s\right)\cdot T(f_p,f_s,K,D_1,D_2,\ldots,D_K)\cdot G \quad (2)$$

where F_0 is a fairly weak function of K, and G is a proportionality constant.

To optimize the multistage design (i.e., to minimize R_T or N_T) we can choose a value for the number of stages, K, and then find the decimation ratios (D_i's) which minimize the relevant quantity. By comparing values of R_T or N_T for several choices of K (typically from K = 2 to K = 4) the overall design can be optimized.

By way of example of the results obtained by performing the above optimization on N_T, Fig. 4 shows a plot of the function T of Eq. (2) as a function of D, the overall decimation ratio for the frequency design constraint $\Delta f = (f_s - f_p)/f_s = 0.1$. For comparison, the dotted curves in Fig. 4 correspond

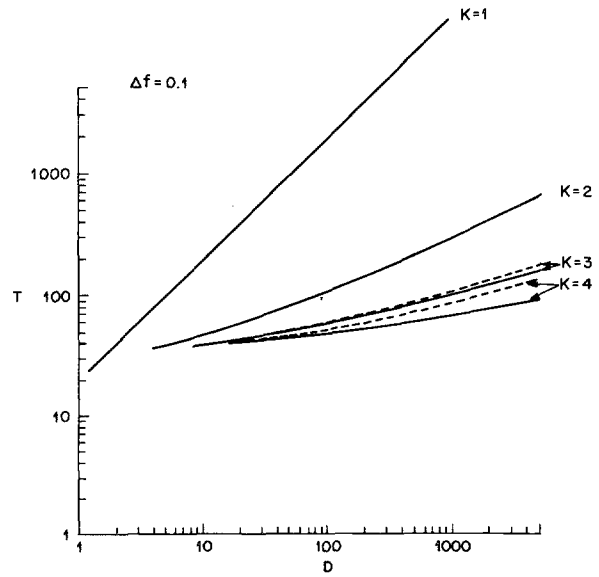

Figure 4: Plot of minimized values of T as a function of K, D, and Δf is 0.1.

to values of T when R_T is minimized. For K = 1, and K = 2 (i.e., 1 and 2 stage designs) the two designs are essentially identical. For 3 and 4 stages, a savings in storage of at most 2:1 is possible using a minimized storage design instead of a minimum computation design. It was also found that the total computation for designs minimized in terms of storage was essentially the same as the total computation for designs minimized in terms of computation.

Figure 5 shows a plot of the function S versus D for optimized decimation rates for K = 1,2,3 and 4, and for Δf = 0.1. It can be

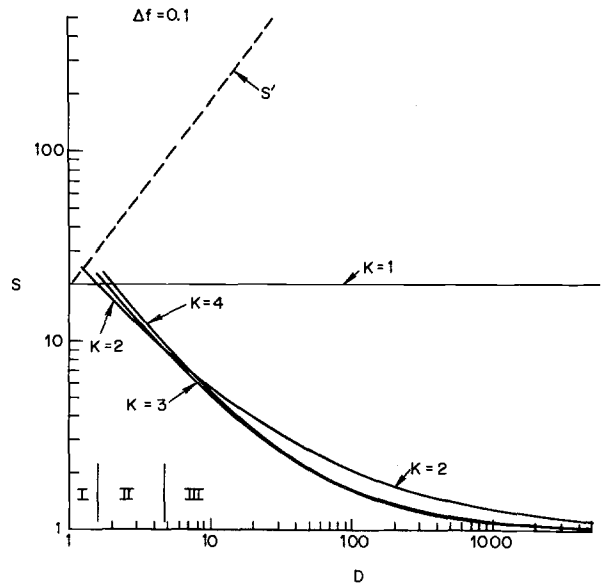

Figure 5: Plot of minimized values of S as a function of K, D, and Δf where Δf is 0.1.

seen that for a D of 100, the relative computation savings in going from a one-stage (K = 1) to a two-stage design is about 10 to 1, whereas for a three-stage design the relative savings over a one-stage design is about 13 to 1.

III. OPTIMAL DESIGN OF INTERPOLATORS AND NARROW BAND FILTERS

We have already shown that the decimation process can generally be implemented more efficiently as a multistage process than in a single stage. Similarly it can be shown by duality that the interpolation process can also be implemented more efficiently as a multistage process.[2] Thus all the design curves for multistage decimators apply equally to the design of multistage interpolators.

The ideas discussed above can also be applied to the implementation of narrow band filters in the following manner. If a signal is decimated down to a low sampling rate and then interpolated back to the high rate, we have, in effect, lowpass filtered the signal. Obviously the same result can be obtained directly with a lowpass filter operating at the high rate, f_{r0}. It has been shown[2] that the first method, that of decimation and interpolation, is generally a considerably more efficient way of implementing a narrow

band FIR lowpass filter than the standard direct form implementation at the high sampling rate. The savings is on the order of S'/3S (see Fig. 5).

IV. IMPLEMENTATION OF DECIMATORS AND INTERPOLATORS

It has been shown[2] that for a decimation stage, which lowers the sampling rate by a factor of M, the computation of each output point y(n) can be expressed in the form

$$y(n) = \sum_{k=0}^{N-1} h(k)x(nM-k) \qquad (3)$$

where N is the number of samples in the filter impulse response, h(n). For an interpolation stage which raises the sampling rate by a factor of L, the computation of each output point y(n) can be expressed in the form

$$y(n) = \sum_{k=0}^{Q-1} h(kL+n \oplus L)x([\tfrac{n}{L}] - k) \qquad (4)$$

where $\oplus$ denotes modulo, $[\cdot]$ corresponds to the integer part of the number in the brackets and Q = N/L is the number of nonzero input samples of x(n) which enter the computation.

Figure 6a shows a block diagram of a three-stage decimator in cascade with a three-stage interpolator, and Fig. 6b shows the corresponding control sequence. To realize either a decimator, interpolator, or a lowpass filter with fewer stages, appropriate parts of this structure can be partitioned off from the main structure. The implementation of the decimation stages is a straightforward application of Eq. (3). The implementation of the interpolation stages requires scrambling the filter coefficients (h(n)), so that sequential accesses of the coefficients can be used to compute each output sample as discussed in Ref. 2.

V. FURTHER IMPLEMENTATION ISSUES

5.1 Multiband Filters

At each stage of decimation or interpolation a lowpass filter has been used to remove appropriate frequency bands of the signal. For some of the stages in a multistage design the lowpass filter can be replaced by a multiband digital filter whose order is smaller than the order of the lowpass filter - thereby reducing the overall computation.

By way of example, Fig. 7 shows a plot of the percentage decrease in filter duration using a multiband design as a function of the relative bandwidth of the equivalent lowpass filter for a stage with a decimation rate of 5. It is seen that for a sufficiently narrow bandwidth, decreases on the order of 2 to 1 can be obtained.

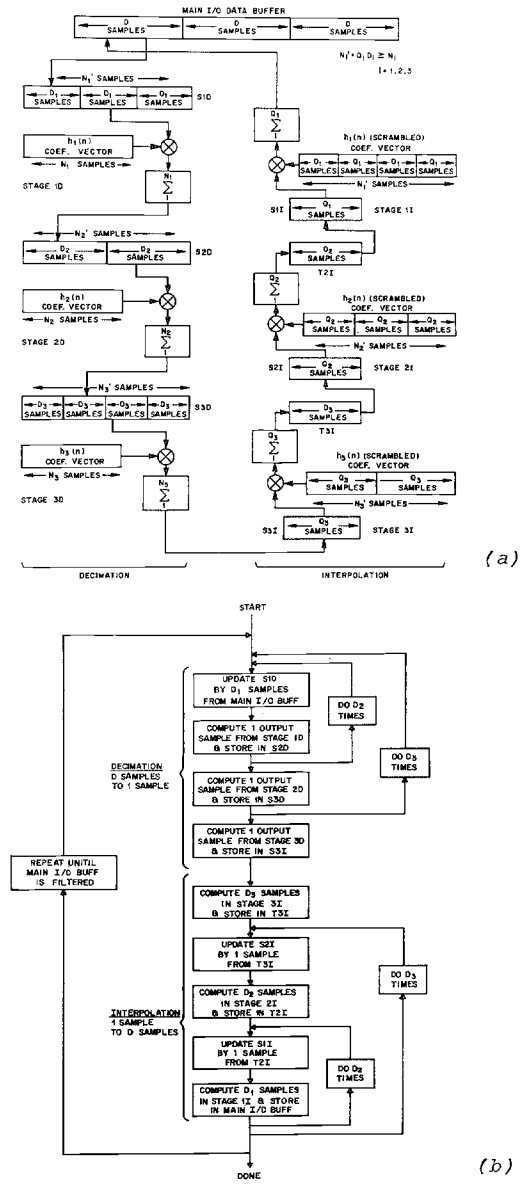

Figure 6: (a) A block diagram for implementation of a three-stage decimator followed by a three-stage interpolator, and (b) its control sequence.

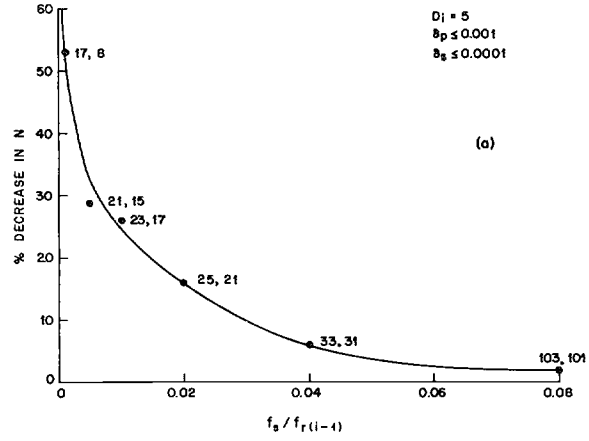

Figure 7: Percentage decrease in filter order using a multiband filter design.

5.2 IIR Filters

The suitability of using IIR filters instead of FIR designs for multistage implementations was also investigated. It was found that a multistage IIR design was only slightly more efficient computationally than a single stage IIR design, and that it was always less efficient, in terms of storage, than the single stage IIR design.

VI. SUMMARY

In this paper we have presented issues in the design of multistage decimators and interpolators. It was shown that designs which are optimized in terms of minimum storage requirements are essentially optimized in terms of computation as well. A practical scheme for implementing multistage decimators and interpolators was presented. Finally the use of multiband filter designs and IIR filter designs for decimators and interpolators was discussed.

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[2] R. E. Crochiere and L. R. Rabiner, "Optimum FIR Digital Filter Implementations for Decimation, Interpolation and Narrow Band Filtering," IEEE Trans. on Acoustics, Speech, and Signal Proc., Vol. ASSP-23, No. 5, pp. 444-456, October 1975.

[3] R. R. Shively, "On Multi-Stage FIR Filters with Decimation," IEEE Trans. on Acoustics, Speech, and Signal Proc., Vol. ASSP-23, No. 4, pp. 353-357, August 1975.