Localized Stability Checking and Design of IC Power Delivery With Distributed Voltage Regulators

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***Abstract*—Placing multiple voltage regulators onto the die is an effective way of enabling distributed on-chip voltage regulation and provides significant benefits in suppressing various types of power supply noise. However, the complex interactions between the active voltage regulators and the large passive subnetwork may render the complete power delivery network (PDN) unstable, leading to design failures. While traditional stability measures such as phase margin are not applicable to regulated PDNs that have a large number of loops, a brute-force analysis of network stability can be impractical due to the high complexity of a given PDN. We present a hybrid stability margin concept and the associated stability-checking method for PDNs with integrated linear low-dropout voltage regulators (LDOs). With theoretical rigor, the proposed approach is local in the sense that the stability of the entire network can be efficiently examined through a hybrid stability constraint that is defined locally for individual LDOs. In the same spirit, we propose a localized LDO design methodology that optimizes individual LDOs in a stand-alone manner while ensuring the network-level stability. Key circuit-level design considerations and tradeoffs involved in stability-ensuring LDO design are also discussed.**

***Index Terms*—Low-dropout voltage regulator (LDO), distributed on-chip regulation, passivity, power delivery, stability.**

I. Introduction

ON-CHIP integration of voltage regulators and converters has emerged as a promising means to address many IC power delivery challenges [1], [9], [11]. It is well known that on-chip voltage regulation reduces both static and dynamic supply voltage droops and also helps suppress the resonance caused by package inductances. Moreover, placing multiple regulators, e.g., low-dropout voltage regulators (LDOs), close to heavy noise sources on the die in a distributive manner (as illustrated in Fig. 1) can further maximize the benefit of localized regulation [4], [14], [13].

While integrating multiple on-chip voltage regulators to facilitate distributed active regulation is appealing and represents a significant ongoing design trend, a potential roadblock, the concern on instability, also arises. While stability is largely a nonproblem in traditional passive power distributions, the regulatory nature of active voltage regulators can indeed render the power delivery network (PDN) unstable. An unstable PDN can manifest itself with sustained supply voltage oscillations, which may cause severe degradation of circuit performance or even chip operation failure. But the understanding of the stability of the network is very challenging due to the complex interactions between multiple active regulators and the immense size of the passive *RLC* subnetwork.

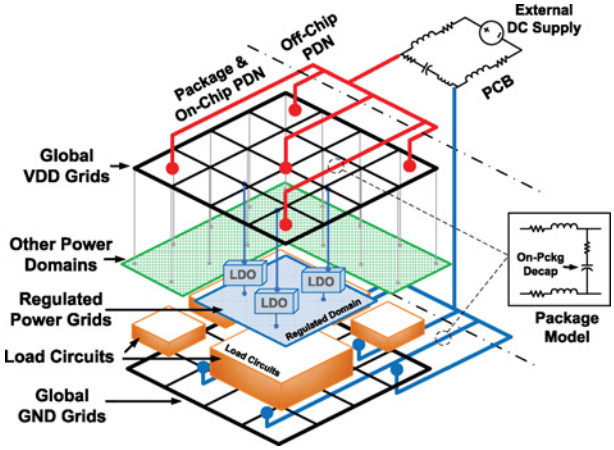

Fig. 1. Illustration of the PDN with distributed on-chip regulators.

Traditional small-signal stability analysis methods, as commonly employed in the standard LDO design process, are incapable of addressing the above challenge; they are either unable to capture the effects of inter-regulator loops, a key characteristic of multi-LDO-regulated PDNs or computationally intractable for PDNs with a practical size. Phase/gain margins are commonly used by analog designers for checking the small-signal stability of analog circuits including LDOs. However, these methods are single-loop-based, i.e., it is assumed that there exits only one dominant (outer) loop in the design and the stability analysis only pertains to this loop. In practice, phase or gain margins are computed mostly when the circuit is loaded with a simple lumped capacitor. In this paper, we show that the use of phase margin can lead to completely misleading prediction of the stability of PDNs regulated by distributed LDOs.

On the other hand, in theory, the small-signal stability of a PDN may be thoroughly detected by finding the existence of

Manuscript received October 9, 2012; revised January 23, 2013; accepted March 11, 2013. Date of current version August 16, 2013. This work was supported in part by Semiconductor Research Corporation and the Texas Analog Center of Excellence under Contract 2008-HC-1836. This paper was recommended by Associate Editor H. Qian.

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Digital Object Identifier 10.1109/TCAD.2013.2256393

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any right half-plane (RHP) poles of the closed-loop system. However, this has a computational cost that is cubic in the size of the PDN and is impractical for practical designs. The computational complexity exacerbates in an iterative design process in which LDOs may be tuned multiple times before it is finally pinned down.

It is pressing to develop localized and computationally tractable network stability checking and by building upon it establish a practical regulator design approach in the above application. One of our previous papers [15] presented a preliminary work to conquer these challenges.

In this paper, we first present a modeling and partitioning strategy of the PDN to describe the system-wide feedback loops in the PDN, making it possible to reason about stability while tracking the interactions between the LDOs and the passive *RLC* subnetwork. Putting the proposed approach on a firm theoretical footing, we then adopt and extend the recently emerged hybrid stability theory (HST) [5], developed originally for multivariable robust control, to examine the stability of PDNs with multiple LDOs. We rigorously prove that under a set of practical conditions, a PDN is guaranteed to be stable. The use of HST allows us to combine the notions of small gain (of system-level loops) and passivity (of individual regulators) to impose more relaxed sufficient conditions for guaranteeing the network stability. Moving one step further, we leverage our HST framework to achieve the goal of localized stability checking. That is, with one time AC simulation of the passive subnetwork, the stability of the complete PDN can be determined by locally characterizing the gain and the passivity of individual LDOs. While the passivity of analog circuits and gains of system-level loops are unfamiliar concepts to typical analog designers, we show how these properties may be leveraged to render feasible stability checking of a given large PDN and empower practical iterative LDO design in a typical analog design flow.

Apart from stability checking, the second key objective of this paper is to develop localized LDO design techniques and methodology that guarantee the stability of the PDN while achieving good power delivery performance. We first define a hybrid stability margin (HSM) concept that numerically assesses the network stability and guides the tradeoffs between stability and other design specifications for the optimization of LDOs. We show how HSM can be introduced to the standard LDO design process as one additional stability constraint to facilitate the goal of localized stability-ensuring design. One key aspect of the proposed design methodology is the investigation of circuit-level design techniques, e.g., a proper choice of LDO topologies, and the introduction of additional design freedoms, which may lead to the most efficient guarantee of the network stability and the best tradeoffs with other design specifications. Based on these developments, we identify transistor-level regulator design parameters that are key to the system-wide stability and develop an automated localized LDO design flow that jointly optimizes several important design specifications pertaining to stability, voltage regulation, and power efficiency.

Experimentally, we demonstrate that the classical phase margin approach, when applied to multiregulator PDNs, can lead to erroneous prediction of network stability, disqualifying it as a trustworthy network-wide stability metric. Furthermore, detailed studies are presented to demonstrate the effectiveness and efficiency of the proposed design methodology that provides a rigorous theoretical guarantee for the stability of several PDNs without any significant degradation of other LDO performances.

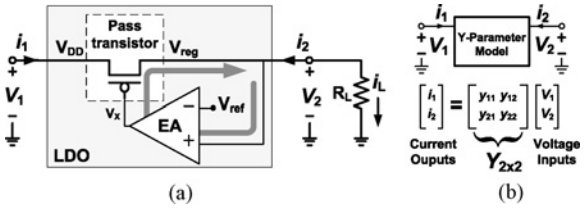

Fig. 2. (a) Generic LDO structure. (b) Two-port Y-parameter model of the generic LDO.

II. Stability Problem

While it is very attractive to apply the distributed on-chip voltage regulation in a PDN, the stability of the whole system has to be guaranteed in the first place.

Stability is a general concern for any feedback control system. For example, Fig. 2(a) depicts a generic LDO circuit structure which includes a pass transistor whose pass resistance is dynamically tuned by a negative feedback loop (referred to as the local loop in the rest of this paper) to counteract the change of the output voltage (V_{reg}). As a result, V_{reg} can be maintained at a preset value regardless of either fluctuations of the global supply voltage V_{DD} or variations of the load current i_L . Due to the feedback control, however, the circuit can be potentially unstable and circuit designers need to perform stability checking to verify the LDO's stability.

Unfortunately, it is particularly challenging in the LDO circuit design phase to guarantee the stability of the entire large-scale PDN in question, primarily due to the large network size and the complicated interactions among the on-chip regulators as well as the surrounding passive *RLC* subnetwork. The classical stability-checking approaches traditionally used for regulator design can be categorized into two groups: the ones that check, via an expensive pole analysis, the existence of RHP poles of the closed-loop transfer function of a system and the ones (e.g., phase margin or the Nyquist plot) that leverage characteristics of the open-loop transfer function of a system.

The methods in the first group are not applicable to this multi-LDO PDN design for the following reasons. To search for RHP poles of the closed-loop transfer function of the system, an eigenvalue problem needs to be solved at a runtime cost of $O(N^3)$, where N is the number of nodes in the network. It is even daunting that every time the LDO design is modified, the eigenvalue problem has to be solved once again. Considering that the PDNs in practical designs can easily have millions of circuit nodes, the prohibitive cost involved will obviously disqualify this type of methods as a practical option. Another disadvantage is that even if the system's instability has finally been identified, designers are usually left with no clue on how to fix the problem.

The second group of approaches, while perfectly suitable for single-input and single-output (SISO) systems and widely

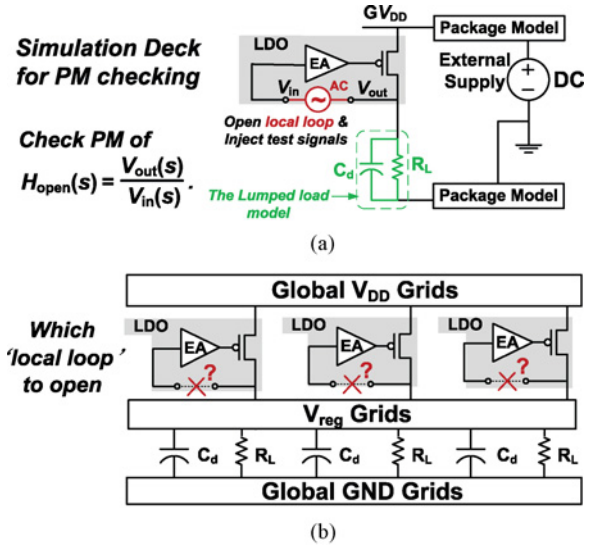

Fig. 3. Illustration of the problem when applying the open-loop methods to the stability problem under discussion. (a) Traditional stability checking in the design of a single LDO. (b) Problem illustration when applying the open-loop method to the PDN.

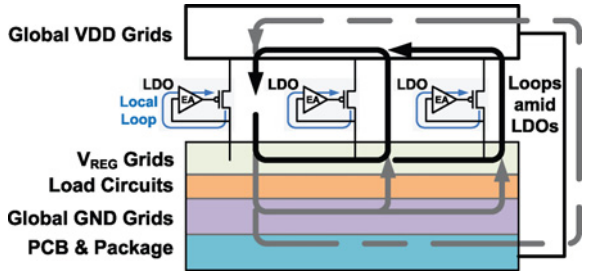

Fig. 4. Illustration of the inter-LDO loops in the PDN.

adopted by regulator designers, can hardly be applied to the stability problem under discussion. For example, the classical phase margin method, inspecting narrowly at the characteristics of the local loop inside an individual LDO as illustrated in Fig. 3(a), cannot find in the PDN a major loop to open for the stability analysis, as illustrated in Fig. 3(b). In this scenario, not only that the LDO under design is also a part of the load to itself, but there are also multiple inter-LDO feedback loops as depicted in Fig. 4 which may be accused of causing instability of the network but are invisible to the method. Therefore, it makes the stability conclusion given by this type of methods not reliable anymore.

To further illustrate this point, we adopted a realistic LDO design [8] as an example. We first designed the LDO in the traditional manner, achieving a phase margin of about 110° under a typical load capacitor (decap) of about 100 pF and above 40° under a wide range of decap from 1 pF to 1 nF, which was interpreted as a highly stable design by the conventional stability-checking method. Interestingly, we found that when multiple copies of this LDO design were integrated into a PDN, the entire network was possibly unstable. To gradually disclose how the stability of the PDN in this example was destroyed, we examined the network stability every time we added one more LDO into the PDN. To keep the loads to each LDO roughly constant as more LDOs were

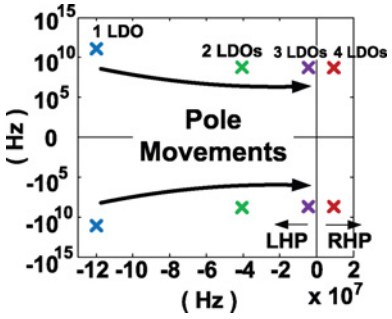

Fig. 5. Pole analysis results that demonstrate an instability-arousing pole movement (each cross represents a pole location).

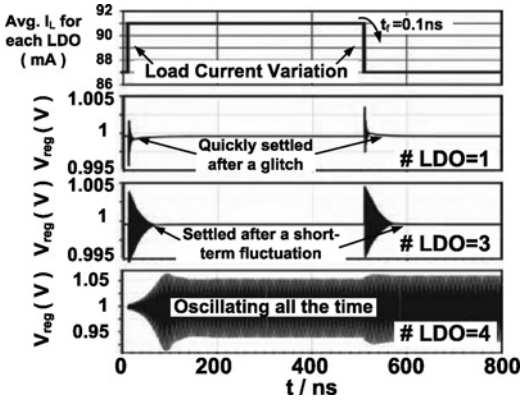

Fig. 6. Transient analysis results that demonstrate the stability problem.

added, the total amounts of decap and load current in the PDN were increased proportionally with the number of LDOs. As the size of the power grids in this illustrative example was intentionally made small (about 20 nodes with the parasitic grid resistance being a few hundreds of mΩ), the thorough pole analysis on the whole network could be applied to check the stability. The package model given in [18] was adopted in this example. Fig. 5 demonstrates the problematic pole movements extracted from the analysis results. It is observed that as the number of LDOs in the PDN increases, there are a pair of complex poles moving from the left half of the *s*-plane toward the right half-plane (i.e., from the stable region toward instability), which is further confirmed by the corresponding transient simulation results shown in Fig. 6 which demonstrates that heavy oscillation of the local supply voltage (V_{reg}) occurs when there are four LDOs in the PDN.

The above example clearly shows that achieving a high phase margin for each stand-alone LDO does not provide any guarantee for the stability of the integrated network. One of the major reasons for the phase margin method to fail is the inappropriate handling of signal loops in the network. The phase-margin based LDO stability analysis is only positioned to capture the interaction between one LDO and the rest of the network. As already pointed out, this treatment is unable to take the interactions among the LDOs into account. Not surprisingly, inspecting one LDO at a time while assuming the rest of the circuit may be modeled as a simple passive load, as implied in the application of the phase margin method, can lead to erroneous conclusions about network stability.

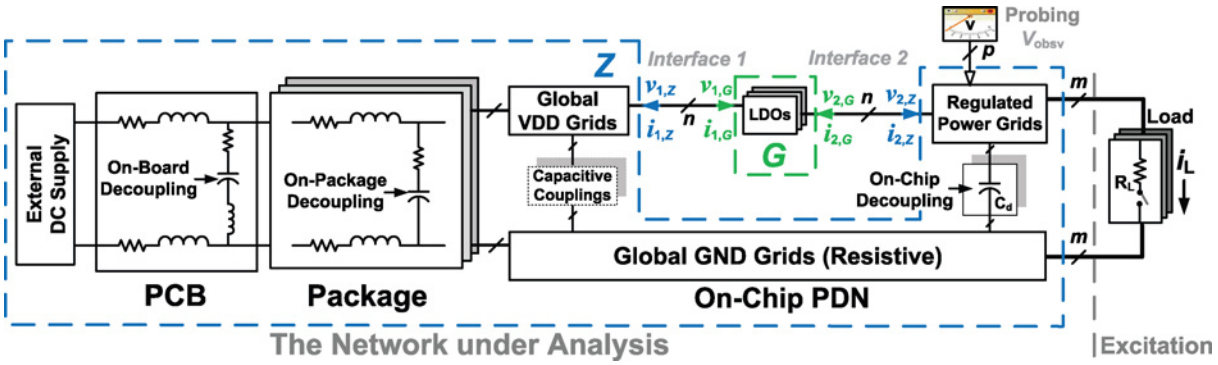

Fig. 7. Partition of the PDN model.

Therefore, building a sensible network model that captures all stability-endangering signal loops is the first critical step toward tackling the problem.

III. PDN Partitioning and Modeling

Partitioning is a common practice in the divide-and-conquer paradigm for solving large complex problems. Toward the goal of establishing a theoretically rigorous and practically useful treatment of the stability challenge, we first present an effective way of partitioning and modeling of the PDN, which facilitates the identification of a complete set of system-wide signal-flow loops responsible for the stability of the entire network.

A. Concepts

The PDN can be partitioned in a way to properly account for all key signal paths at the network level, which contribute in a significant way to stability. This requires us to move away from SISO-based approaches as typically adopted by analog designers and take a multiport-based modeling approach.

Furthermore, partitioning should be done in a way to facilitate the iterative design process in which network stability may be checked multiple times as the LDOs are tuned. Thus, it is highly desirable to detach the bulky passive *RLC* subnetwork, which requires a great effort to analyze, from this iterative design process. This leads us to consider a partition that separates the passive *RLC* subnetwork from all the LDOs, resulting in two multiport subsystems: one that contains only the regulators and the other comprised merely of the passive *RLC* subnetwork serving as the load to the LDOs. This partitioning strategy has an appealing advantage. As will be shown later in this paper, it allows us to spend only a one-time cost to characterize the passive subnetwork using the AC analysis, based on which stability constraints that are local to each individual LDOs are extracted prior to the iterative LDO design process. In the subsequent design process, these extracted local stability constraints are used to drive the optimization of each LDO while guaranteeing the stability of the complete network.

Note that in the proposed partitioning scheme, all the LDOs are grouped in a single multiport subsystem despite the fact that their physical locations are spread out. In other words, the partitioning is done not based on physical vicinity, rather to electrically separate the LDOs from the passive subnetwork.

B. Proposed Network Partition and Modeling

The proposed partition of the PDN with n on-chip LDOs is illustrated in Fig. 7, where the dashed lines represent the partition boundaries and the two subsystems are, respectively, represented by block $\boldsymbol{G}$ that only contains the LDOs and the passive subnetwork $\boldsymbol{Z}$ which is enclosed in the U-shaped dashed box. Between $\boldsymbol{G}$ and $\boldsymbol{Z}$, there are two types of interfaces corresponding to the V_{DD} ports and V_{reg} ports of the LDOs. Therefore, for n on-chip LDOs in the PDN, each subsystem has $2n$ interfacing ports. Besides the interfacing ports, block $\boldsymbol{Z}$ is also connected to both the PDN's excitation inputs, which are the variations of the load currents $\boldsymbol{i}_L$ and the whole system's outputs, which can be any nodal voltages of interest on the power grids ($\boldsymbol{V}_{\text{obsv}}$).

As the LDOs are commonly linearized and in order to utilize the signal-flow graph, we model the LDO block by a $2n$-port $\boldsymbol{Y}$-parameter model with each LDO described by the 2×2 Y-parameter matrix shown in Fig. 2(b). The transfer matrix of block $\boldsymbol{G}$ is then given by

$$\underbrace{\begin{bmatrix} i_{1,1} \\ i_{2,1} \\ \vdots \\ i_{1,i} \\ i_{2,i} \\ \vdots \\ i_{1,n} \\ i_{2,n} \end{bmatrix}}_{2n \times 1} = \underbrace{\begin{bmatrix} \boldsymbol{Y}_{2\times2,1} & \cdots & \boldsymbol{0} & \cdots & \boldsymbol{0} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \boldsymbol{0} & \cdots & \boldsymbol{Y}_{2\times2,i} & \cdots & \boldsymbol{0} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ \boldsymbol{0} & \cdots & \boldsymbol{0} & \cdots & \boldsymbol{Y}_{2\times2,n} \end{bmatrix}}_{\boldsymbol{G}_{2n\times2n}} \underbrace{\begin{bmatrix} v_{1,1} \\ v_{2,1} \\ \vdots \\ v_{1,i} \\ v_{2,i} \\ \vdots \\ v_{1,n} \\ v_{2,n} \end{bmatrix}}_{2n \times 1} \tag{1}$$

where $i_{j,k}$ $(j = 1, 2; k = 1, \ldots, n)$ represents the jth port current of the kth LDO, and similarly $v_{j,k}$ is its port voltage.

It is worth noting that because of the way in which block $\boldsymbol{G}$ is constructed, the LDOs are isolated to each other; accordingly, the matrix $\boldsymbol{G}_{2n\times2n}$ is block-diagonal with the ith block being the 2×2 Y-parameter matrix of the ith LDO, as can be observed from (1). The computational benefit from this property will be discussed in Section V.

The PDN then can be abstracted into a block diagram of a feedback control system shown in Fig. 8(a), where block $\boldsymbol{G}$ interfaces with block $\boldsymbol{Z}$ through $2n$ voltage signals and $2n$ current signals. Furthermore, the excitation inputs and the outputs can be removed for the stability analysis because for

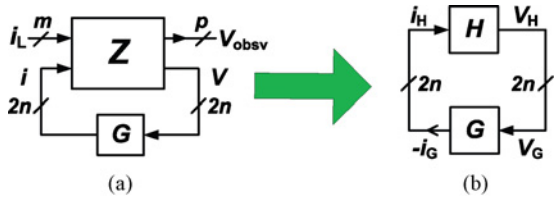

Fig. 8. PDN modeling with the system-wide feedback loop. (a) Complete PDN model with system inputs and outputs. (b) PDN model reduced to contain only signals pertaining to the stability issue.

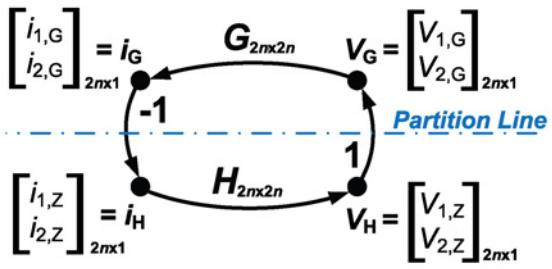

Fig. 9. Signal-flow graph of the system. ($i_{1,G}, i_{2,G}, V_{1,G}, V_{2,G}$ and $i_{1,Z}, i_{2,Z}, V_{1,Z}, V_{2,Z}$ are the same as in Fig. 7.)

LTI systems, stability is an intrinsic property regardless of external system inputs or outputs. Thereby during the stability analysis, block $\boldsymbol{Z}$ can be reduced into block $\boldsymbol{H}$ which only retains the interfacing ports with $\boldsymbol{G}$. By modeling $\boldsymbol{H}$ with a $2n$-port Z-parameter model whose inputs are $2n$ currents ($\boldsymbol{i}_H$) with the outputs being $2n$ voltages ($\boldsymbol{v}_H$), we simplify the system model into the one as shown in Fig. 8(b), to which stability theory can be readily applied.

By modeling the LDO block and the passive subnetwork in the above way, the system's signal-flow graph can be built as shown in Fig. 9, where every electrical quantity (i.e., a current or voltage) or a "node" is only dependent on the upper stream node. Therefore, when we partition as illustrated by the dash-dotted line in Fig. 9, the output signals of the two partitions, namely $\boldsymbol{i}_G$ and $\boldsymbol{V}_H$, are, respectively, determined only by the corresponding inputs (namely $\boldsymbol{V}_G$ and $\boldsymbol{i}_H$) as well as the partition transfer matrices $\boldsymbol{G}_{2n\times 2n}$ and $\boldsymbol{H}_{2n\times 2n}$. In this way, the stability evaluation of the LDO block can be confined within the partition itself without any overlook of loading effect between the two partitions, which is important to the rigorousness of our method.

From Fig. 9, the system-wide multivariable feedback loop is identified starting from the inputs ($\boldsymbol{i}_H$) of block $\boldsymbol{H}$ to its outputs ($\boldsymbol{V}_H$), which are directly fed to block $\boldsymbol{G}$, and the loop finally ends at the outputs ($\boldsymbol{i}_G$) of $\boldsymbol{G}$. As the positive directions of port currents are defined as flowing into the corresponding blocks, $\boldsymbol{i}_G$ and $\boldsymbol{i}_H$ are of the same magnitude but the opposite directions, i.e., the loop is a negative feedback.

IV. Theoretical Framework

Toward a rigorous theoretical guarantee rather than an empirical educated guess about the PDN stability, in this section, we lay out the development of the theoretical framework that is not only suitable for effective and efficient stability checking, but offers more flexibility for achieving superior system performance.

An ideal stability-checking method should have the following desirable properties: 1) it should be able to handle multi-input and multioutput (MIMO) feedback systems such as the one in Fig. 8(b); 2) it needs to avoid or at least greatly reduce the analysis cost associated with the large passive network (block $\boldsymbol{H}$) in order to be computationally efficient; 3) the stability conditions adopted in the method shall not lead to poor system performance.

Based on the above discussion, the use of a combination of passivity and small-gain principles offers an appealing solution to the stability problem at hand. This approach goes naturally with the network partitioning presented in the previous section and facilitates a localized checking methodology. Prior to delving into this theoretical framework, we first introduce several key concepts and relevant mathematical backgrounds [3], [5], [12], followed by the theoretical framework we specifically developed for the targeted PDNs.

A. Preliminaries

The stability concerned in this paper is referred to as signal convergence in terms of the norm in the L_2-space. The L_2-space is the space of square-integrable functions defined by $L_2 = \left\{\boldsymbol{v} : \mathbb{R}^+ \mapsto \mathbb{R}^m \middle| \int_0^\infty \boldsymbol{v}^{\mathrm{T}}(t)\, \boldsymbol{v}(t)\, dt < \infty\right\}$, where $\boldsymbol{v}$ is an arbitrary vector function of time and $\boldsymbol{v}^{\mathrm{T}}$ is its transpose. The L_2-space is a Hilbert space, where the inner product defines the norm

$$\langle \boldsymbol{w}, \boldsymbol{v}\rangle = \int_0^\infty \boldsymbol{w}^{\mathrm{T}}(t)\, \boldsymbol{v}(t)\, dt, \quad \|\boldsymbol{v}\|_2 = \sqrt{\langle \boldsymbol{v}, \boldsymbol{v}\rangle} \tag{2}$$

where $\boldsymbol{v} \in L_2, \boldsymbol{w} \in L_2$, and $\langle\cdot,\cdot\rangle$ is the inner product.

Definition 1: (System gain) Consider a general square system with an input $\boldsymbol{w}(t) \in L_2$ and an output $\boldsymbol{y}(t) \in L_2$ mapped through an operator $\boldsymbol{M} : L_2 \to L_2$, the induced L_2-gain, or simply the system gain, is defined by

$$\gamma = \sup_{\forall \boldsymbol{w}\in L_2, \boldsymbol{w}\neq 0} \|\boldsymbol{y}\|_2 / \|\boldsymbol{w}\|_2. \tag{3}$$

A system possesses *finite gain* if there exists $0 < \gamma < \infty$ such that

$$\gamma\langle \boldsymbol{w}, \boldsymbol{w}\rangle \geq \gamma^{-1}\langle \boldsymbol{y}, \boldsymbol{y}\rangle, \quad \forall \boldsymbol{w} \in L_2. \tag{4}$$

For any LTI system, the induced L_2-gain is equivalent to the $\mathcal{H}_\infty$-norm of the system transfer matrix, $\boldsymbol{M}$, which is defined by $\|\boldsymbol{M}\|_\infty = \max_{0\leq\omega<\infty} \|\boldsymbol{M}(j\omega)\|_2$, and

$$\|\boldsymbol{M}(j\omega)\|_2 = \max_i \left[\lambda_i(\boldsymbol{M}^{\mathrm{H}}(j\omega)\boldsymbol{M}(j\omega))\right]^{\frac{1}{2}} \tag{5}$$

where $\lambda_i(\boldsymbol{M})$ denotes the ith eigenvalue of $\boldsymbol{M}$ and $\boldsymbol{M}^{\mathrm{H}}$ denotes the complex conjugate transpose of $\boldsymbol{M}$.

Definition 2: (Passive systems) A general square system with an input $\boldsymbol{w}(t) \in L_2$ and an output $\boldsymbol{y}(t) \in L_2$ mapped through the operator $\boldsymbol{M} : L_2 \to L_2$ is passive if there exist constants $\delta \geq 0$ and $\epsilon \geq 0$ such that $\forall \mathbf{w}$,

$$\langle \boldsymbol{w}, \boldsymbol{y}\rangle \geq \delta\langle \boldsymbol{w}, \boldsymbol{w}\rangle + \epsilon\langle \boldsymbol{y}, \boldsymbol{y}\rangle. \tag{6}$$

Furthermore, if $\delta > 0$, then the system is called *input strictly passive*; if $\epsilon > 0$, then the system is *output strictly passive*;

the system is *very strictly passive* if both $\delta > 0$ and $\epsilon > 0$. Based on (3) and (4), it can be easily derived that a system that is already input strictly passive with finite gain is output strictly passive, and hence is very strictly passive.

The passivity of LTI systems can also be examined in the frequency domain. Consider that $\boldsymbol{M}$ is an LTI system which has a minimal realization that is asymptotically stable; then, we have [3]:

1) $\boldsymbol{M}$ is passive if and only if its transfer matrix satisfies $\boldsymbol{M}(j\omega) + \boldsymbol{M}^{\mathrm{T}}(-j\omega) \geq 0, \forall \omega \in \mathbb{R}$;

2) $\boldsymbol{M}$ is input strictly passive if and only if its transfer matrix satisfies that $\exists \delta > 0, \boldsymbol{M}(j\omega) + \boldsymbol{M}^{\mathrm{T}}(-j\omega) \geq \delta \boldsymbol{I}, \forall \omega \in \mathbb{R}$, i.e., all eigenvalues of $\boldsymbol{M}(j\omega) + \boldsymbol{M}^{\mathrm{T}}(-j\omega)$ are greater than or equal to δ.

Unfortunately, for many systems, a passive input–output map defined by (6) does not always exists. When a system's passive input–output relationship does not hold for a certain input case, we say that passivity violation occurs. In particular, for LTI systems, if there exists a frequency ω where the condition $\boldsymbol{M}(j\omega) + \boldsymbol{M}^{\mathrm{T}}(-j\omega) \geq 0$ is not met, then passivity violation occurs.

On the other hand, we also define the passiveness of the system with passivity violations as local passivity. Before rigorously defining it, we first define a passivity filter $\mathcal{A}{:}L_2 \rightarrow L_2$, which is a causal convolution operator; also, we define $\mathbb{A} = \mathcal{A}\boldsymbol{I}$, where $\boldsymbol{I}$ represents the identity matrix.

Definition 3: (Local passivity) A general square system with an input $\boldsymbol{w}(t) \in L_2$ and an output $\boldsymbol{y}(t) \in L_2$ mapped through the operator $\boldsymbol{M} : L_2 \rightarrow L_2$ is locally passive, if there exists a passivity filter $\mathbb{A}$ and constants $\delta \geq 0$ and $\epsilon \geq 0$, such that

$$\langle \mathbb{A}\boldsymbol{w}, \mathbb{A}\boldsymbol{y} \rangle \geq \delta \langle \mathbb{A}\boldsymbol{w}, \mathbb{A}\boldsymbol{w} \rangle + \epsilon \langle \mathbb{A}\boldsymbol{y}, \mathbb{A}\boldsymbol{y} \rangle. \tag{7}$$

If $\exists \delta > 0, \textit{and } \epsilon > 0$ that satisfy (7), the system is referred to as locally very strictly passive.

For LTI systems, denoting the frequency set where the system meets the passivity condition by $\Omega \triangleq \{\omega \in \mathbb{R} | \boldsymbol{M}(j\omega) + \boldsymbol{M}^{\mathrm{T}}(-j\omega) \geq 0\}$, we define a frequency-dependent function $\alpha(\omega){:}\mathbb{R} \rightarrow \{0, 1\}$ as [5]

$$\alpha(\omega) \quad = \quad \begin{cases} 1, & \omega \in \Omega \\ 0, & \text{otherwise.} \end{cases} \tag{8}$$

Let $A(s)A(-s)$ be the spectral factorization of the Laplace transform of the inverse Fourier transform of $\alpha(\omega)$. Then, we have

$$\alpha(\omega) = A(j\omega)A(-j\omega). \tag{9}$$

Furthermore, the time domain equivalent to $A(s)$ is a causal convolution operator $\mathcal{A}{:}L_2 \rightarrow L_2$, referred to as the frequency selection operator in the rest of this paper. Obviously, $\mathcal{A}$ can be a passivity filter for LTI cases. Again, $\mathbb{A}$ is also defined accordingly and has its Fourier transformation $\boldsymbol{A}(j\omega) = A(j\omega)\boldsymbol{I}$. Note that if an LTI system is passive, then it is locally passive with respect to any Ω including $\Omega = \{\omega | \omega \in \mathbb{R}\}$.

B. Two Classical Stability Theorems

Considering the Barkhausen oscillation conditions, it is intuitive that if the loop gain of a feedback system is less than 1, then any oscillation through the loop will finally be attenuated and hence the system remains stable. The intuition leads us to the *small-gain theorem*, a classical stability theorem for general feedback systems.

Given the feedback system in Fig. 8(b) and the system gain defined by (3), the small-gain theorem states the following result [12].

Theorem 1: (Small-Gain theorem) The negative feedback interconnection of the subsystems $\boldsymbol{G}{:}L_2 \rightarrow L_2$ and $H{:}L_2 \rightarrow L_2$ is L_2-stable if the product of the gains of the two subsystems is strictly less than 1.

That is, the whole system is L_2-stable as long as $\gamma_{\mathrm{G}}\gamma_{\mathrm{H}} < 1$, where γ_{G} and γ_{H} are, respectively, the gain of blocks $\boldsymbol{G}$ and $\boldsymbol{H}$. As such, the theorem allows γ_G and γ_H to be separately evaluated through (5). Therefore, if one subsystem is fixed (as the passive subnetwork) while the design of the other one is in process (as the LDOs), the gain evaluation on the fixed subsystem can be done once for all and be used to assist the iterative design of the other subsystem. Thus, the stability of the entire system can be checked locally on the other subsystem.

The small-gain theorem, however, utilizing merely gain information of the subsystems, tends to give a Pyrrhic victory for ensuring stability. This is because one of the subsystems (e.g., the passive subnetwork in our case) once has a very high gain at any operational frequencies of interest, the other one (e.g., the LDO block) would be mandated by the theorem to have a rather low gain, resulting in poor closed-loop system performance.

In addition to exploiting the characteristics of system gains of the subsystems, another property that LDO designers may easily resort to is the phase information of the open-loop transfer function of an SISO system. For MIMO systems, *passivity* can be deemed, in some sense, as a quantity that correlates with the phase information of the system transfer matrix. Thus, as we are trying to relax the harsh constraint on the gains (performance) imposed by the small-gain theorem, the *passivity* property is considered as another avenue to ensure stability.

The *passivity theorem* states the following useful result for the system in Fig. 8(b) [12].

Theorem 2: (Passivity theorem) The negative feedback interconnection of the subsystems $\boldsymbol{G}{:}L_2 \rightarrow L_2$ and $\boldsymbol{H}{:}L_2 \rightarrow L_2$ is L_2-stable if one system is passive while another is very strictly passive.

The theorem implies that the whole system is L_2-stable if both $\epsilon_{\boldsymbol{G}} \geq 0, \delta_{\boldsymbol{G}} \geq 0$ and $\epsilon_{\boldsymbol{H}} > 0, \delta_{\boldsymbol{H}} > 0$, where $\epsilon_{\boldsymbol{G}}$ and $\delta_{\boldsymbol{G}}$, respectively, represent the ϵ and δ of block $\boldsymbol{G}$ as defined in (6), so do $\epsilon_{\boldsymbol{H}}$ and $\delta_{\boldsymbol{H}}$ of block $\boldsymbol{H}$. Similar to the small-gain theorem, the passivity of each subsystem can also be checked separately.

While a system with only passive elements is necessarily passive, a system containing active elements cannot usually be passive. Therefore, the passivity theorem alone cannot be the silver bullet either. In fact, it is more often the case that analog circuits (such as regulators) behave like a passive system over a certain frequency range, suggesting potential good use of local passivity for ensuring stability.

C. Hybrid Stability Theorem

Recently, stability theories that simultaneously exploits small-gain and passivity properties of a general system have

emerged [5], [6]. In particular, a *hybrid stability theorem* has been proposed to make use of the local passive behaviors. If a general system has passivity violations, the finite gain property is instead exploited for stability by the following theorem [5].

Theorem 3: (Hybrid stability theorem) The negative feedback interconnection of the subsystems $\boldsymbol{G}$:$L_2 \rightarrow L_2$ and $\boldsymbol{H}$:$L_2 \rightarrow L_2$ is L_2-stable if the following three conditions are met: 1) $\exists \epsilon_{\mathbf{G}} \geq 0$, $\delta_{\mathbf{G}} \geq 0$ and $\exists \epsilon_{\mathbf{H}} \geq 0$, $\delta_{\mathbf{H}} \geq 0$, such that $\boldsymbol{G}$ and $\boldsymbol{H}$ are both locally passive with respect to a common passivity filter $\mathbb{A}$; 2) $\epsilon_{\mathbf{G}} + \delta_{\mathbf{H}} > 0$ and $\epsilon_{\mathbf{H}} + \delta_{\mathbf{G}} > 0$; 3) when passivity violation occurs, $\gamma_{\mathbf{G}}\gamma_{\mathbf{H}} < 1$ holds.

While providing a sufficient condition for stability, Theorem 3 nevertheless offers much greater design freedom in achieving superior closed-loop performance by combining the two previous basic stability theorems.

D. Hybrid Stability Framework for PDNs

Based upon the above general stability theory, we develop a specific hybrid stability framework for PDNs. The proposed framework is based on the following two key observations of any realistic PDN of our concern. LDOs are connected to the passive subnetwork (e.g., the global VDD grids and the regulated power grids in Fig. 7) through resistive metal wires and vias, which contribute to non-zero input serial resistance of the corresponding ports of the passive subnetwork as illustrated by the resistors $r_1 \ldots r_{2n}$ in Fig. 10. Note that the impedance model of the passive subnetwork is denoted as block $\boldsymbol{H}$ in the figure. Furthermore, the system gain of the passive subnetwork in a realistic PDN, i.e., $\|\boldsymbol{H}(j\omega)\|_\infty$, cannot reach infinity, i.e., it is always upper bounded.

By virtue of the above observations, we derive the following important property of the passive subnetwork in such a PDN.

Property 1: The passive subnetwork of Fig. 10 is very strictly passive.

Proof: According to Definition 2, we would like to show that for the realistic passive subnetwork $\boldsymbol{H}$:$\boldsymbol{i_H}(t) \in L_2 \rightarrow \boldsymbol{v_H}(t) \in L_2$, $\exists \epsilon_{\boldsymbol{H}} > 0$ and $\delta_{\boldsymbol{H}} > 0$, such that $\langle \boldsymbol{i_H}(t), \boldsymbol{v_H}(t)\rangle \geq \epsilon_{\boldsymbol{H}} \langle \boldsymbol{i_H}(t), \boldsymbol{i_H}(t)\rangle + \delta_{\boldsymbol{H}} \langle \boldsymbol{v_H}(t), \boldsymbol{v_H}(t)\rangle$.

To begin with, we know that $2\langle \boldsymbol{i_H}(t), \boldsymbol{v_H}(t)\rangle = \{\langle \boldsymbol{i_H}(t), \boldsymbol{v_H}(t)\rangle + \langle \boldsymbol{v_H}(t), \boldsymbol{i_H}(t)\rangle\}$, which, by Parseval's theorem, is equivalent to the expression

$$\frac{1}{2\pi}\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)[\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)]\boldsymbol{i}(j\omega)d\omega. \tag{10}$$

As well known that an LTI *RLC* network is passive [10], the matrix $\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)$ is therefore positive semidefinite. If we denote the passive network excluding those input resistors r_i $(i = 1, \ldots, 2n)$ by $\widetilde{\boldsymbol{H}}$, then $\widetilde{\boldsymbol{H}}$ is also passive. From Fig. 10, it can be easily inspected that

$$\boldsymbol{v_H} = \begin{bmatrix} v_1 \\ \vdots \\ v_{2n} \end{bmatrix} = \begin{bmatrix} v_1' \\ \vdots \\ v_{2n}' \end{bmatrix} + \boldsymbol{R}\begin{bmatrix} i_1 \\ \vdots \\ i_{2n} \end{bmatrix} = (\widetilde{\boldsymbol{H}} + \boldsymbol{R})\boldsymbol{i_H} \tag{11}$$

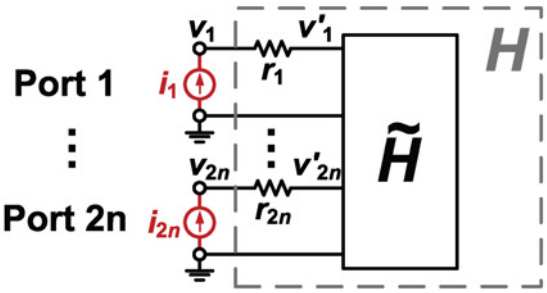

Fig. 10. Illustration of serial resistances at each port of the $\boldsymbol{H}$ block.

where $\boldsymbol{R}$= diag$\{r_1, \ldots, r_{2n}\}$, where $r_i \in \mathbb{R}_+$ $(i = 1, \ldots, 2n)$. Then, we have $\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega) = \widetilde{\boldsymbol{H}}(j\omega) + \widetilde{\boldsymbol{H}}^{\mathrm{T}}(-j\omega) + 2\boldsymbol{R}$. Therefore, for $\forall \boldsymbol{X} \in \mathbb{R}^{2n}$ and $\boldsymbol{X} \neq \boldsymbol{0}$, we have

$$\begin{aligned} &\boldsymbol{X}^{\mathrm{H}}\left[\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)\right]\boldsymbol{X} \\ &= \boldsymbol{X}^{\mathrm{H}}\left[\widetilde{\boldsymbol{H}}(j\omega) + \widetilde{\boldsymbol{H}}^{\mathrm{T}}(-j\omega) + 2\boldsymbol{R}\right]\boldsymbol{X} \\ &= \underbrace{\boldsymbol{X}^{\mathrm{H}}\left[\widetilde{\boldsymbol{H}}(j\omega) + \widetilde{\boldsymbol{H}}^{\mathrm{T}}(-j\omega)\right]\boldsymbol{X}}_{\geq 0} + \underbrace{\boldsymbol{X}^{\mathrm{H}}(2\boldsymbol{R})\boldsymbol{X}}_{> 0} \\ &\geq \min_{k=1,\ldots,2n}\{2r_k\}\boldsymbol{X}^{\mathrm{H}}\boldsymbol{X} \\ &> 0. \end{aligned} \tag{12}$$

Since $\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)$ is continuous with respect to ω and, according to (12), is positive definite, there exists $l_{\min} = \inf_{\omega\in\mathbb{R}} \underline{\lambda}(\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)) > 0$, where $\underline{\lambda}(\cdot)$ means the minimum eigenvalue. Also since $\|\boldsymbol{H}(j\omega)\|_\infty$ is upper bounded, $s_{\max} = \sup_{\omega\in\mathbb{R}} \|\boldsymbol{H}(j\omega)\|_2$ exists. Hence by selecting $\epsilon > 0$ and $\delta > 0$ that meet the inequality

$$l_{\min} \geq \epsilon + \delta s_{\max}^2 > 0 \tag{13}$$

we have

$$\begin{aligned} &\tfrac{1}{2\pi}\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)[\boldsymbol{H}(j\omega) + \boldsymbol{H}^{\mathrm{T}}(-j\omega)]\boldsymbol{i}(j\omega)d\omega \\ &\geq \tfrac{l_{\min}}{2\pi}\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)\boldsymbol{i}(j\omega)d\omega \\ &\geq \tfrac{1}{2\pi}(\epsilon + \delta s_{\max}^2)\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)\boldsymbol{i}(j\omega)d\omega \\ &\geq \tfrac{1}{2\pi}\epsilon\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)\boldsymbol{i}(j\omega)d\omega \\ &\qquad + \tfrac{1}{2\pi}\delta\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)\boldsymbol{H}^{\mathrm{T}}(-j\omega)\boldsymbol{H}(j\omega)\boldsymbol{i}(j\omega)d\omega \\ &\geq \tfrac{1}{2\pi}\epsilon\textstyle\int_{-\infty}^{\infty} \boldsymbol{i}^{\mathrm{H}}(j\omega)\boldsymbol{i}(j\omega)d\omega + \tfrac{1}{2\pi}\delta\textstyle\int_{-\infty}^{\infty} \boldsymbol{v}^{\mathrm{H}}(j\omega)\boldsymbol{v}(j\omega)d\omega. \end{aligned} \tag{14}$$

That is, $\exists \epsilon_{\boldsymbol{H}} = \epsilon/2 > 0$ and $\delta_{\boldsymbol{H}} = \delta/2 > 0$, such that $\langle \boldsymbol{i_H}(t), \boldsymbol{v_H}(t)\rangle \geq \epsilon_{\boldsymbol{H}} \langle \boldsymbol{i_H}(t), \boldsymbol{i_H}(t)\rangle + \delta_{\boldsymbol{H}} \langle \boldsymbol{v_H}(t), \boldsymbol{v_H}(t)\rangle$. ■

Based on Theorem 3 and Property 1, we come up with the following corollary that serves directly as the theoretical foundation for the proposed localized stability-checking method as well as the automated stability-aware system optimization presented in the next sections.

Corollary 1: The feedback interconnection of a subsystem $\boldsymbol{G}$:$L_2 \rightarrow L_2$ and a very strictly passive subsystem $\boldsymbol{H}$ is L_2-stable if at $\forall \omega \in \mathbb{R}$, either one of the following two conditions is met: 1) $\gamma_{\mathrm{G}}(j\omega)\gamma_{\mathbf{H}}(j\omega) < 1$; 2) $\boldsymbol{G}(j\omega) + \boldsymbol{G}^{\mathrm{T}}(-j\omega) \geq 0$.

Proof: Apparently, when applying Corollary 1 to our design scenario, the passive subnetwork would be the subsystem $\boldsymbol{H}$ according to Property 1, and the LDO block would be the subsystem $\boldsymbol{G}$. If the first condition (i.e., $\gamma_G\gamma_H < 1$) is met, then there is no need for block $\boldsymbol{G}$ to be locally passive as prescribed by Theorem 3. To prove this corollary, we only need to show that if the transfer matrix $\boldsymbol{G}(s)$ satisfies the second condition (i.e., $\boldsymbol{G}(j\omega) + \boldsymbol{G}^{\mathrm{T}}(-j\omega) \geq 0$) over some frequency range Ω, then there exist $\epsilon_{\boldsymbol{G}} \geq 0$, *and* $\delta_{\boldsymbol{G}} \geq 0$, such that block $\boldsymbol{G}$ is locally passive with respect to Ω. On the other hand, according to Property 1, block $\boldsymbol{H}$ is locally very strictly passive with respect to Ω. Therefore, there exist $\epsilon_{\boldsymbol{H}} > 0$ and $\delta_{\boldsymbol{H}} > 0$ satisfying $\epsilon_{\boldsymbol{G}} + \delta_{\boldsymbol{H}} > 0$ and $\epsilon_{\boldsymbol{H}} + \delta_{\boldsymbol{G}} > 0$.

Given the transfer matrix $\boldsymbol{G}(s)$, define a frequency set $\Omega \triangleq \{\omega \in \mathbb{R} | \boldsymbol{G}(j\omega) + \boldsymbol{G}^{\mathrm{T}}(-j\omega) \geq 0\}$ and the corresponding $\alpha(\omega)$ as well as the corresponding frequency selection operator $\mathbb{A}$. We define the convolution operator $\mathbb{G}$:$\boldsymbol{v_G}(t) \in L_2 \rightarrow \boldsymbol{i_G}(t) \in L_2$ that corresponds to $\boldsymbol{G}(s)$. Then, according to the positive semidefiniteness of $\boldsymbol{G}(\omega) + \boldsymbol{G}^{\mathrm{T}}(-\omega)$, for $\forall \boldsymbol{v_G}(t) \in L_2$, we have

$$\frac{1}{2\pi}\int_{\Omega} \boldsymbol{v}_{\boldsymbol{G}}^{\mathrm{H}}(j\omega)\left[\boldsymbol{G}(\omega) + \boldsymbol{G}^{\mathrm{T}}(-\omega)\right]\boldsymbol{v_G}(j\omega)d\omega \geq 0. \tag{15}$$

By introducing $\alpha(j\omega)$ into the integral to convert the integration range to be from $-\infty$ to $+\infty$, (15) is turned into

$$\begin{aligned}\frac{1}{2\pi}[&\int_{-\infty}^{\infty} \boldsymbol{v}_{\boldsymbol{G}}^{\mathrm{H}}(j\omega)\boldsymbol{G}^{\mathrm{H}}(\omega)(\alpha(\omega)\boldsymbol{I})\boldsymbol{v_G}(j\omega)d\omega \\ &+ \int_{-\infty}^{\infty} \boldsymbol{v}_{\boldsymbol{G}}^{\mathrm{H}}(j\omega)(\alpha(\omega)\boldsymbol{I})\boldsymbol{G}(\omega)\boldsymbol{v_G}(j\omega)d\omega] \geq 0.\end{aligned} \tag{16}$$

By substituting (9) for $\alpha(j\omega)$ into (16) and by Parseval's theorem, we get

$$\begin{aligned}&\langle \mathbb{A}\boldsymbol{v_G}(t), \mathbb{A}\mathbb{G}\boldsymbol{v_G}(t)\rangle + \langle \mathbb{A}\mathbb{G}\boldsymbol{v_G}(t), \mathbb{A}\boldsymbol{v_G}(t)\rangle \\ &\qquad = 2\langle \mathbb{A}\boldsymbol{v_G}(t), \mathbb{A}\mathbb{G}\boldsymbol{v_G}(t)\rangle \geq 0\end{aligned} \tag{17}$$

i.e., $\exists \epsilon_{\boldsymbol{G}} \geq 0$ and $\delta_{\boldsymbol{G}} \geq 0$, such that $\langle \mathbb{A}\boldsymbol{v_G}(t), \mathbb{A}\boldsymbol{i_G}(t)\rangle \geq \epsilon_{\boldsymbol{G}}\langle \mathbb{A}\boldsymbol{v_G}(t), \mathbb{A}\boldsymbol{v_G}(t)\rangle + \delta_{\boldsymbol{G}}\langle \mathbb{A}\boldsymbol{i_G}(t), \mathbb{A}\boldsymbol{i_G}(t)\rangle \geq 0$. ■

With the theoretical foundation built, in the next section, we demonstrate how to perform stability checking for the PDN based on Corollary 1.

V. New HSM Concept and Efficient Stability Checking of the PDN

Based on the hybrid stability theorem and the corollary, we come up with a rigorous and efficient stability-checking method. We further propose a new HSM that assesses the system's stability, such that the stability-checking method can be incorporated into an *automated* optimization flow. The computational cost of the method is also analyzed.

A. Stability Checking of the PDN

The stability of the entire PDN is examined according to a frequency-sampling approach. Given a set of P points $\omega_k, k = 1, \ldots, P$ sampled in the frequency range of interest, the passivity and gain conditions are evaluated at each frequency ω_k. If for all frequencies at least one condition is satisfied, then the stability of the system is guaranteed.

1) *Passivity Evaluation:* Given a total number of n LDOs in the network, the passivity of the LDO block at ω_k is evaluated by finding the smallest eigenvalues of the $2n \times 2n$ matrix $\boldsymbol{G}(j\omega_k)$+$\boldsymbol{G}^H(j\omega_k)$.

More efficiently, the evaluation can be performed on one LDO at a time, thanks to the fact that the transfer matrix $\boldsymbol{G}$ is block-diagonal, a feature of the LDO model mentioned in Section III-B. The 2×2 admittance matrix of the jth LDO is denoted as $\boldsymbol{Y}_j(j = 1, \ldots, n)$. Therefore, the passivity of $\boldsymbol{G}$ is evaluated by finding the value $\lambda_{min}(j\omega_k)$ given by

$$\lambda_{\min}(j\omega_k) = \min_{i=1,2;j=1,\ldots,n}\{\lambda_i(\boldsymbol{Y}_j(j\omega_k) + \boldsymbol{Y}_j^H(j\omega_k))\}. \tag{18}$$

If $\lambda_{\min}(j\omega_k) \geq 0$, the LDO exhibits passivity at ω_k; otherwise, passivity violation occurs.

Note that there is no need to perform such a passivity check for the large-scale passive load subnetwork.

2) *System Gain Evaluation:* To decouple the design of LDO from the passive network, the evaluations of the L_2-gain of the two subsystems are separately performed and inequality $\|\boldsymbol{G}\|\|\boldsymbol{H}\| < 1$ is targeted. At ω_k, $\|\boldsymbol{G}(j\omega_k)\|_2$ and $\|\boldsymbol{H}(j\omega_k)\|_2$ are first calculated using (5). Again, as $\boldsymbol{G}$ is block-diagonal, $\|\boldsymbol{G}(j\omega_k)\|_2$ can be obtained by

$$\|\boldsymbol{G}(j\omega_k)\|_2 = \max_{j=1,\ldots,n}\|\boldsymbol{Y}_j(j\omega_k)\|_2 \tag{19}$$

where $\|\boldsymbol{Y}_j(j\omega_k)\|_2$ is the jth block corresponding to the jth LDO.

If $\|\boldsymbol{G}(j\omega_k)\|_2\|\boldsymbol{H}(j\omega_k)\|_2 < 1$, then the system passes our stability checking at ω_k.

3) *Cost of Evaluation:* Due to the small size of the LDO circuit, the cost of the passivity and gain evaluation for each LDO is very low. The overall cost of evaluation is dominated by the evaluation of the gain of the large passive load network $\|\boldsymbol{H}(j\omega_k)\|_2$, which involves an AC analysis to determine the transfer matrix $\boldsymbol{H}(j\omega)$ at ω_k.

Given that the total number and locations of the LDOs are predetermined and the passive load subnetwork is fixed, the evaluation only needs to be done once. Whenever the design of LDO is tuned, we only need to recompute (18) and (19) for the stability checking, which is very efficient because of the small size of the LDO.

If there are P sampling points, n LDOs, and N nodes in the passive subnetwork, the cost of AC analysis for the passive subnetwork is $O(PN^{\alpha})$, given $n \ll N$, $P \ll N$ and typically α is somewhat greater than 1.0 depending on the sparsity of the circuit matrices. Note that the AC characterization of on-chip power grids including the package is routinely done in existing design flows even for PDNs without on-chip voltage regulation. In this sense, the proposed stability checking for regulated PDNs does not incur any significant additional analysis cost.

B. Hybrid Stability Margin (HSM)

We further define an HSM that integrates the evaluations of passivity and gain into a single quantitative measure. HSM can be incorporated as a localized stability constraint into an automated stability-ensuring LDO design flow, as described in the next section.

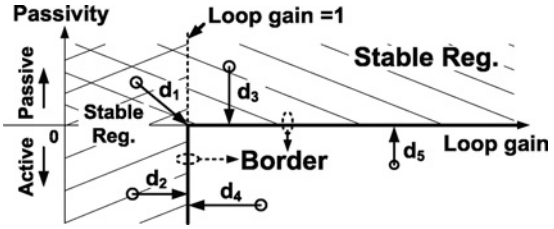

Fig. 11. HSM at a frequency point.

We first define the HSM on an individual frequency basis. In Fig. 11, the horizontal axis represents $\|\boldsymbol{G}(j\omega_k)\|_2\|\boldsymbol{H}(j\omega_k)\|_2$ and the vertical axis represents $\lambda_{\min}(j\omega_k)$. Based on the evaluation of gain and passivity, an LDO design can be represented by a point in the plane. According to the hybrid stability theorem, the stability-guaranteed region is the band area $0 < \|\boldsymbol{G}\|_2\|\boldsymbol{H}\|_2 < 1$ in union with the quadrant where $\lambda_{\min} > 0$. The border of the region is depicted with the bold solid lines.

The hybrid stability metric is defined as a signed distance to the border of the stability-guaranteed region. In Fig. 11, there are five design cases evaluated at frequency ω_k and each case is represented by a circle. The HSM(ω_k) for each case is the signed length of the corresponding arrowed line. The sign is positive if the circle is in the stability-guaranteed region, and negative otherwise.

VI. Practical PDN Network Design

The proposed stability-checking approach provides a basis for evaluating the stability of a given PDN by means of a localized LDO HSM design constraint. This makes it possible to efficiently leverage this constraint to drive the LDO design optimization in an enhanced design flow. On the other hand, from a design perspective, the introduction of HSM into the design process of LDOs does introduce new design issues. In many aspects, the techniques one may take to meet the proposed HSM are with a flavor similar to ones that are commonly employed by the designers to meet conventional phase/gain margin targets. This similarity may help the adoption of the proposed design approach by typical designers. Nevertheless, our in-depth design analysis reveals unique design considerations pertaining to tradeoffs between the new HSM and other LDO performances, choice of key transistor-level design parameters, and LDO design topologies. In this section, we demonstrate a localized automated LDO design flow and discuss key circuit-level design issues involved.

A. Design Flow

As elaborated in the previous section, all the information required by the proposed stability-checking approach can be obtained from AC simulations which circuit designers are well familiar with. Thus, the approach can be easily integrated into the conventional LDO design flow which the LDO designers are already accustomed to. As such, the stability-ensuring LDO design flow can be built upon the conventional flow with the inclusion of one additional stability constraint.

The integration of the stability-checking approach is illustrated in Fig. 12. First of all, an initial LDO design with

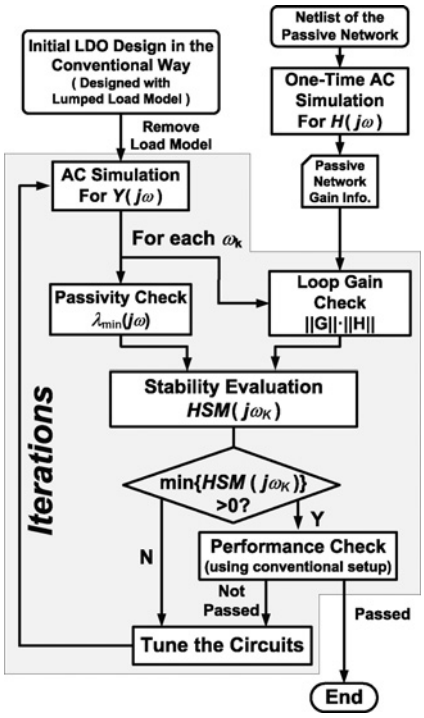

Fig. 12. Stability-ensuring design flow.

sufficient circuit performances is obtained using the conventional design methodology. The network stability evaluation over the specified frequency samples is then performed at each iteration until the stability is guaranteed and the performance requirements are satisfied. Note that only the low-cost LDO circuit evaluations (as in the gray box in Fig. 12) are repeated in each design iteration, on the premises that the LDO sizing during the optimization is well contained without affecting the passive subnetwork structure, which may be achieved by measures like prescribing a fixed chip area large enough to accommodate sizing of the LDO within the optimization boundaries.

B. LDO Design Insights and Performance Tradeoffs

From a design point of view, the key issues in ensuring system stability are to properly control the gain, bandwidths, etc. These are in some sense not more than what are manually done in the standard LDO design process, including, but not limited to, reducing the 3-dB bandwidth (pole splitting), increasing the quiescent current, and adjusting the gain of the local loop. Clearly, just like in the case of conventional phase or gain margin, there are tradeoffs between stability and other performances. However, there exist several new design issues and opportunities for the case of hybrid stability, which we discuss below.

One powerful aspect of the proposed stability-ensuring framework is that it leverages the notions of passivity and small gain in a complimentary way. This provides very useful degrees of design freedom for guaranteeing stability and trading off with other performances. We discuss two types of design freedom: one that immediately exploits the frequency-dependent nature of the hybrid stability framework and another that creates freedom through circuit or topology modifications.

1) *Exploiting Frequency Dependence:* As described earlier, hybrid stability can be ensured by satisfying either the passivity or gain condition at each frequency. The optimal design of LDOs can be approached by choosing judiciously one of the two conditions to satisfy for each frequency in a way to minimize area and power overhead and influences on other performances. It is instructive to examine how such optimal designs may vary across different frequency ranges.

At *DC and low frequencies*, through investigations on the 2×2 Y-matrix of an LDO, we found that it is advantageous for the LDO designed to satisfy the gain condition $(\gamma_{\mathrm{G}}(j\omega)\gamma_{\mathrm{H}}(j\omega) < 1)$. Specifically speaking, in this frequency band, the elements in the first column of the Y-matrix are smaller in magnitude than the corresponding elements in the second column roughly by a factor of A_{LL}, where A_{LL} represents the loop gain of the local loop of each individual LDO, a critical performance metric in the LDO design. For good closed-loop regulation performances, a large A_{LL} is normally desired. On the other hand, by examining the property of the Y-matrix, it can be observed that the LDO can simply become not passive under large A_{LL}. Therefore, it is extremely hard, if not impossible, for an LDO to achieve good regulation performances while exhibiting passive characteristics in this frequency range. The conflict between passivity and regulation performance is somewhat intuitively straightforward since this is what active regulation is supposed to be as to differentiate from passive regulation. In order to pass the HSM check while keeping good regulation performance, satisfying the gain condition should be targeted.

On the other hand, it is critical to note that satisfying the gain condition does not necessarily imply lowering A_{LL}. Importantly, we have developed a constraint-relaxing technique that allows us to lower the gain of the system-wide loop without introducing much degradation of regulation performance (corresponding to a high A_{LL}). We discuss the design implications resulted from the technique below while directing the interested readers to Appendix A for more details.

First, take a look at a typical LDO structure illustrated in Fig. 13(a) as well as some important AC currents labeled as i_p, i_s, and i_{EA}. i_p and i_{EA} are, respectively, the dynamic currents flowing in or out of the pass transistor and the error amplifier, while i_s is the dynamic ground current in the output stage. The technique then reveals that a generally effective way of satisfying the gain condition is to make $|i_s|$ larger than $|i_{\mathrm{EA}}|$.

At *mid- and high-frequencies*, it is well known that the impedance peaking due to package parasitic inductance usually occurs, which is around the typical on-chip LDO's unity-gain bandwidth (GBW). Since the gain of $\boldsymbol{Z}$-parameter matrix of block $\boldsymbol{H}$ is in a sense of impedance, the package resonance peakings are reflected in $\gamma_{\boldsymbol{H}}$ as similar peaks of value. While we observed that LDOs usually exhibit local passivity in a frequency band beyond its GBW, it is usually of less performance cost to force the LDO to meet the passivity condition than the gain condition at those peaking frequencies. Tuning the LDO's GBW below the peaking frequencies can be one of the effective measures to meet the passivity condition and it can be done by varying the value of LDO's internal capacitors (e.g., some compensation capacitors or some zero-generation capacitors) and/or reducing the LDO's bias current.

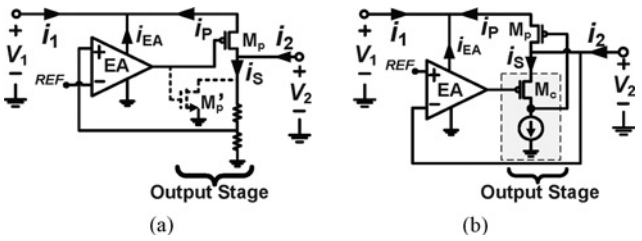

Fig. 13. Demonstrations of exemplary stability-enhancing schemes for the LDO output stage design. (a) Scheme I: simple circuit modification on the output stage. (b) Scheme II: topology change for the output stage.

In addition, it is also observed that the active devices in LDO can no longer react to fast signal changes beyond a certain high frequency ω_h and only their intrinsic and parasitic capacitors remain in play. For example, i_p in Fig. 13(a) is mostly conveyed through the path consisting of the gate-to-source capacitor and the gate-to-drain capacitor of M_p; i_s is through the grounded capacitors associated with the output port, including the drain diffusion capacitance of M_p. Because of the fact that the size of M_p is hundreds to thousands of times larger than the transistors in EA, so are the capacitors associated, thus, $|i_s|$ can easily exceed $|i_{\mathrm{EA}}|$, and the gain condition can be met in this frequency band with little design effort.

Summarily, the passivity condition is chosen in the package impedance peaking frequency range to relieve the efforts on handling the rugged impedance peaks, while the gain condition is selected at either DC and low frequencies or ultrahigh frequencies.

2) *Exploiting Circuit/Topology Modifications:* Another important source of design freedom comes from LDO topology modifications. In particular, if the output stage is designed in such a way that $|i_s|$ is greater than $|i_{\mathrm{EA}}|$, the gain condition can be more easily met. Appendix A gives a more detailed analysis on this claim.

According to this insight, a topological modification on the output stage is identified, i.e., by adding a pull-down pass transistor to the output stage [shown as the dashed NMOS M'_p in Fig. 13(a)] which is seldom seen in existing LDO topologies and is, to our best knowledge, the first time acknowledged for its effectiveness in enhancing stability. Alternatively, in the same spirit, designers can choose another type of output stage topology, e.g., a source follower, as shown in Fig. 13(b) to fulfill the same purpose. Since the selection of LDO topology should be made at the very beginning of the design process, this insight may help designers to make the right choice earlier, reducing possibility of design respinning.

C. Illustrative Design Optimization

To illustrate the application of the proposed techniques, we develop an optimization-based automated design flow using an optimizer to run the iterations shown in Fig. 12. The objective function for this optimization contains two classes of terms: one for penalizing performance degradations and the other for penalizing instability. In general, any performance metric can be considered in the optimization. For an illustration purpose, the LDO's performance metrics considered in this objective function include, but not limited to, the load regulation accu-

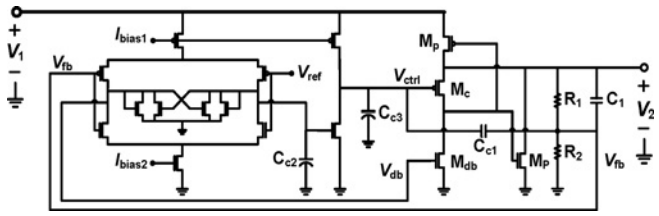

Fig. 14. LDO topology used in the practical implementations [8].

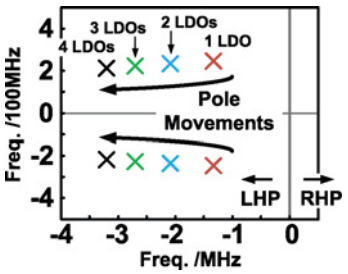

Fig. 15. Pole analysis showing the stability of the PDN desdigned with the proposed approach.

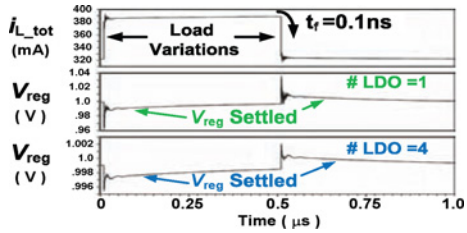

Fig. 16. Transient analysis confirming the stability of the PDN with the stability-ensured LDOs.

racy of the LDO (ACC) defined by $1 - \frac{|V_{\text{reg}} - V_{\text{preset}}|}{V_{\text{preset}}}$ which is an important DC characteristic that measures how close the actual output voltage V_{reg} is to the target voltage V_{preset}; the gain-bandwidth product, GBW; the quiescent current I_q, which emphasizes the quiescent current efficiency; the average output admittance y_{avg}, which can largely reflect how good the dynamic regulation is. y_{avg} is defined by $\frac{1}{\omega_n - \omega_0}\int_{\omega_0}^{\omega_n} |y_{22}(j\omega)|d\omega$, where ω_0 and ω_n are, respectively, the lowest and highest frequencies of interest. These terms are properly normalized and included in the objective function to be minimized

$$f = \alpha\left(\frac{\text{ACC}_n}{\text{ACC}}\right)^k + \beta\left(\frac{\text{GBW}_n}{\text{GBW}}\right)^t + \eta\left(\frac{I_q}{I_{q\_n}}\right)^p + \gamma \lg\left(\frac{y_{\text{avg}\_n}}{y_{\text{avg}}}\right) + \theta 10^{-\text{HSM}} \quad (20)$$

where α, β, η, γ, and θ are the weights for respective performance penalty terms, which reflect optimization biases according to a specific practical set of design requirements; the exponential or logarithmic functions are used to prevent the optimizer from straying far away from the optimal point, and to deal with large differences in the orders of magnitude of those quantities. Specifically, the first four terms in (20) indicate that the greater ACC, GBW, $1/I_q$, and y_{avg} are with respect to the ones achieved by the initial design (i.e., ACC_n, GBW_n, I_{q_n}, and y_{avg_n}), the smaller f is, and the closer the design will be to the optimum. Note that in the situation where there are hard constraints on these performances, we can also change the penalty functions into the ones dealing with the differences between the actual values and the hard constraints. Since negative HSMs do not guarantee stability, an exponential function is chosen to heavily penalize any negative HSM so that stability will be enforced.

For the LDO shown in Fig. 14 [8], due to their importance to hybrid stability and other performance specifications, several transistor-level design parameters are chosen: the widths of M_p, M_c, and M_{db}, and the amounts of pole/zero-tuning capacitors C_{c1}, C_{c2}, C_{c3}, and C_1. The width of the pass transistor (M_p) influences ACC, ω_{-3} dB, GBW, and y_{avg} in a major way, whereas the widths of M_c and M_{db} are influential on the bias current I_q and i_s in Fig. 13. The results of the proposed optimization are presented in detail in the following section.

VII. Experimental Study

In this section, two experimental PDN designs are showcased to demonstrate the effectiveness and efficiency of the proposed approach. While the PDN sizes are different in the two cases, the adopted LDO topology is the same as shown in Fig. 14. And the same package model [8] is adopted. Both cases aim at an optimized PDN design with four on-chip LDOs. An LDO is initially designed in the traditional manner with sufficient circuit performances and a good phase margin (referred to as the initial LDO design in the rest of this paper), and then, respectively, the proposed approach is adopted to optimize the initial LDO design. The circuits are designed and optimized in a commercial 90 nm CMOS technology. The APPS optimizer [7] is adopted to tune the LDO.

A. Multiple LDOs in a Small Network

As discussed in Section II, the brute-force method for stability checking is only feasible for small networks. To verify the effectiveness of the proposed stability-ensuring LDO design approach, we purposely continue the use of the small PDN (of about only 20 nodes) as in the example discussed in Section II and apply our approach to optimize the LDO for the PDN's stability, such that the classical pole analysis method can be adopted to judge the effectiveness of our approach. Comparisons are also made with the example in Section II which showed that an LDO designed in a traditional manner with a good phase margin cannot guarantee the network stability.

In the pole analysis, we target a pair of complex poles that move most evidently as the number of LDOs changes. Fig. 15 shows the movement of the poles on the s-plane as the number of LDOs integrated into the network is increased. In contrast to the rightward pole movement occurred in the counterexample shown in Fig. 5, in this PDN with stability-enforced LDOs, the movement is leftward and there are no RHP poles, meaning that the system is stable and the proposed approach is effective in ensuring the stability of the whole network. It is further confirmed by the transient simulation results shown in Fig. 16 which demonstrates the waveforms of the regulated voltage V_{reg} under load current variations. Compared with the heavy oscillation of V_{reg} in the counterexample shown in Fig. 6, V_{reg} in this case settles after the load current disturbance, reflecting the stability of the system.

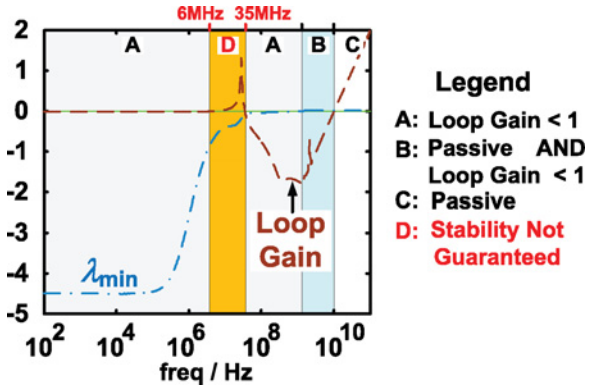

Fig. 17. Loop gain and $\lambda_{\min}$ of the initial design.

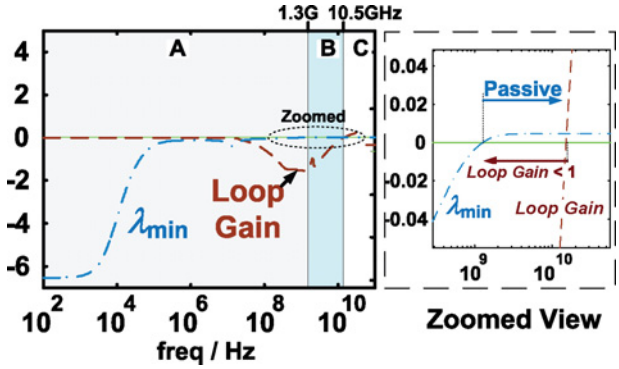

Fig. 18. Loop gain and $\lambda_{\min}$ of the stability-ensured design.

B. Multiple LDOs in a Large Network

We further present the application of our approach to the optimization of LDOs for a PDN of over 200 000 nodes, in an attempt to demonstrate the effectiveness and efficiency of the approach in large PDN design scenarios.

1) *Stability Checking Along the Frequency Axis:* The frequency-wise stability checking on the initial LDO design and the one designed in the stability-ensuring method are, respectively, illustrated in Figs. 17 and 18, with the loop gain and passivity metric $\lambda_{\min}$, being plotted in dashed lines and in dash-dotted lines, respectively. In both figures, the frequency ranges in which the gain condition is met are labeled as A, the ranges where the passivity condition is met are labeled as C, and the ranges where both conditions are met are B, while the potentially unstable range is D. As shown in Fig. 17, the initial design violates the hybrid stability criteria at the frequency band from about 6 to 35 MHz where the loop gain exceeds unity while $\lambda_{\min} < 0$. It is shown in Fig. 18 that, by the proposed approach, the initial design can be successfully optimized into the design that satisfies the HSM criteria over all frequencies and thus guarantees the stability of the whole network.

2) *Effectiveness of the Approach:* In this case, since the pole searching method is impractical, the transient simulation results are instead used to confirm the stability of the system. We first plug in four copies of the initial LDO. As shown in Fig. 19, an arbitrarily selected nodal voltage on the regulated power grids (V_{reg}) as well as the one on the global VDD grids (GV_{DD}) renders continuing oscillations. In contrast, the PDN with LDOs given by our approach shows only slight

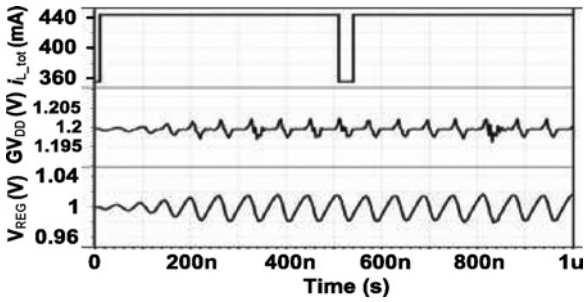

Fig. 19. Transient simulation results showing the instability of the PDN with the LDOs designed in a standard manner.

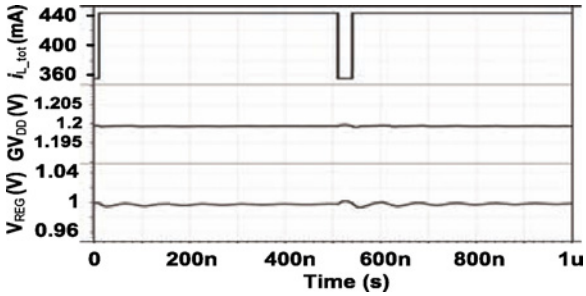

Fig. 20. Transient simulation results confirming the stability of the PDN with the stability-ensured LDOs.

fluctuations when i_L variations occur, after which the voltages become settled, as shown in Fig. 20.

3) *Efficiency of the Approach:* As indicated by Fig. 12, there are two additional sources of design time cost: the AC simulations for the gain characterization of the passive network and the iterations of stability checking.

The former are performed at frequencies ranging from 1 Hz up to 1 THz with 200 samples per decade. There are four LDOs in this case and hence eight ports in the passive network, and the simulation by using an in-house simulator takes about 11 hours. Note that AC simulations are also a common practice in the power grid analysis without regulators. So we do not actually add any additional cost by doing so.

The rest of the stability-assurance procedure (the iterations) is taken over by the optimizer. The optimization takes about 116 minutes (including simulator invocation time) to reach the optimal performance tradeoffs while ensuring stability.

In summary, the total design time in this case is about 13 hours with 11 hours being consumed in the one-time simulation of the passive subnetwork.

C. Performance Tradeoffs

When designing an on-chip regulated PDN, stability is the primary design target. Without stability, the whole chip is easily subjected to power failure. Therefore, comparisons between the stability-ensured LDO designs in the above two cases with the unstable initial LDO design are, in this sense, not meaningful. However, to gain the insights, we perform the comparisons on several performance metrics in this section. Also, in order to get a more complete picture of the tradeoffs, we set up the two optimization cases with different sets of performance weights (i.e., α, β, η, and γ) to represent different performance biases: in the small PDN case, the quiescent current consumption is particularly stressed, while in the large

TABLE I
PERFORMANCE TRADEOFFS

	Initial LDO	Opt. LDO in the large PDN	Opt. LDO in the small PDN
HSM	-18.9	0.01	$5e-3$
Stability	Unstable	Stable	Stable
Load Reg. Acc.	99.96%	99.90%	99.91%
GBW (MHz)	511	422	380
I_q (μA)	469	518	340
y_{avg} (S)	5.21	7.18	4.26
y_{avg}/I_q (S/μA)	0.011	0.0139	0.0125

PDN case, the dynamic regulation performance is emphasized more than the other two performances.

Table I lists the comparisons among the three designs. The network stability metric HSM, negative in the initial design, is greatly optimized to be positive in both optimization cases indicating that the PDN stability is ensured. While it is obvious that the unstable LDO design cannot be used in the PDN, we first show that, in the large PDN case, by consuming 10.4% more quiescent power, the network stability is ensured. In addition, we also gain an improvement of 37.8% on the dynamic regulation performance metric y_{avg}, bringing forth a 26.3% improvement on y_{avg}/I_q, an efficiency quantity that measures the regulation performance gained per unit quiescent power consumed. By emphasizing low power consumption, in the small PDN case, the stability is ensured at a cost of 25.6% GBW reduction and a 18.2% degradation of y_{avg}, associated with a quiescent power saving by 27.5%. The resultant y_{avg}/I_q is however improved by 13.6%.

VIII. CONCLUSION

We have presented a hybrid theoretical framework for addressing the stability challenges of large PDNs with integrated LDOs. A practical design methodology was developed to allow for the localized design of LDOs while ensuring the system-wide stability, leading to trackable stability-driven design optimization of large PDNs. By virtue of unique design freedoms in the framework, useful design insights into the stability-ensuring LDO design were discussed. Experimental results demonstrated the effectiveness and efficiency of our method and also showed that the enforced PDN stability does not necessarily incur significant performance degradations.

APPENDIX A
CONSTRAINT-RELAXING TECHNIQUE TO MEET THE GAIN CONDITION

In Sections VI-B1 and VI-B2, the inequality $|i_s| > |i_{\text{EA}}|$ is pointed out as a helpful design guide for meeting the gain condition prescribed by Corollary 1 without compromising regulation performance significantly. The detailed development of this insight is discussed as follows.

To begin with, reconsider the LDO's 2×2 Y-matrix in Fig. 2(b). To lower the gain of block $\boldsymbol{G}$, the element values of the Y-matrix are inevitably to be decreased, especially the dominant elements. As mentioned in Section VI-B1, y_{12} and y_{22} are the dominant ones at low frequencies. Given the fact that a large y_{22} is the key to achieve good load regulation, the on-chip voltage regulation can be compromised if y_{22} is significantly reduced.

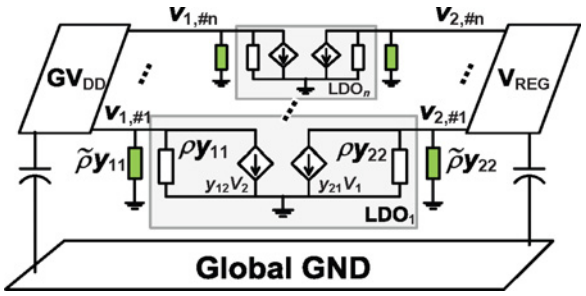

Fig. 21. Illustration of splitting self-admittances in the LDO's Y-parameter model.

In order to solve this dilemma and further relax the stability versus performance tradeoff, we propose to repartition the system by splitting the self-admittances (y_{11} and y_{22}) into two parts with one part remaining in the LDO block and the other part pushed into the passive network, as illustrated in Fig. 21.

Note that the splitting is only performed to meet the gain condition as part of the stability-checking process. In order to have a uniform mathematical description of the two subsystems before and after the repartitioning, we introduce a frequency-dependent splitting coefficient ρ ($= 1 - \tilde{\rho}$) defined in the same way as $\alpha(\omega)$ discussed in Section IV-A

$$\rho(\omega) = \begin{cases} 1, & \omega \in \Omega \\ 0, & \text{otherwise} \end{cases}$$

where Ω is the set of frequencies at which the LDO block satisfies the passivity condition. This splitting is automatically controlled by $\rho(\omega)$ as the stability checking is being performed along the frequency axis. At frequency bands where the gain condition is preferred to satisfy, the self-admittances of LDO block are deemed as elements in block $\boldsymbol{H}$ (i.e., $\rho = 0$); otherwise, they are assigned back to the LDO block (i.e., $\rho = 1$). Obviously, the splitting coefficient is the same as the frequency selection function $\alpha(\omega)$. Thus, the splitting is perfectly synchronized with the switching of the two hybrid stability conditions to meet. Specifically, when to meet the passivity condition, the splitting is not performed and block $\boldsymbol{H}$ is still locally very strictly passive and the local passivity of block $\boldsymbol{G}$ is to be examined; when to meet the gain condition, additional elements are hooked up to the passive subnetwork. For the latter case, because block $\boldsymbol{H}$ is changed, recalculation of its gain is needed, which can be easily done since $\boldsymbol{H}(j\omega)$ is only a small $2n$-port model.

The benefit from repartitioning is that when targeting at the gain condition, block $\boldsymbol{G}$ loses self-admittance elements in the matrix which results in lowered γ_{G}, while on the other hand, the self-impedances of block H are lowered too (due to additional impedance in parallel), resulting in lowered γ_{H}. In this way, meeting the gain condition is in fact helped by increasing $|y_{22}|$. For example, at DC and low frequencies, after moving self-admittances out of block $\boldsymbol{G}$, $\gamma_{\text{G}}(\omega)$ is approximately $|y_{12}(\omega)|$, while $\gamma_{\text{H}}(\omega)$ is roughly as large as $1/|y_{22}(\omega)|$. Therefore, $\gamma_{\text{G}}(\omega)\gamma_{\text{H}}(\omega) \approx |y_{12}(\omega)/y_{22}(\omega)|$, which shows that an increase of $|y_{22}|$ actually reduces the gain of the system-wide loop.

Since increasing $|y_{22}|$ with respect to $|y_{12}|$ is helpful to meet the gain condition, we further examine its design implications. By definition of admittance matrix, $y_{12} = \frac{i_1}{V_2}|_{V_1=0}$; $y_{22} = \frac{i_2}{V_2}|_{V_1=0}$. From Fig. 13(a), it is shown that $|i_1| = |i_p + i_{\text{EA}}|$ and $|i_2| = |i_p + i_s|$. Therefore, one way to increase $|y_{22}|$ with respect to $|y_{12}|$ is to make $|i_s|$ greater than $|i_{\text{EA}}|$, which can be accomplished by designers through one of many means as discussed in Section VI-B2.

In essence, the fundamental reason for this splitting to work is the conservativeness brought by meeting $\gamma_{\text{G}}\gamma_{\text{H}} < 1$ which is only a sufficient condition for stability. Different partitions of the system can lead to different degrees of such conservativeness and hence potential benefits can be obtained by seeking a proper partition of the system. Since the repartitioning does not add or remove any elements into or from the system, the entire system is physically unchanged; the only thing it changes is the way we analyze the whole system.

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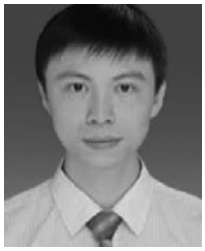

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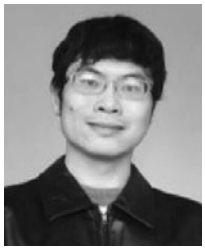

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