ECE137A Notes Set 12:
IC process flows,
Current mirror biasing,
IC design

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MOS process flow

1) Pattern Nitride, implant P+
2) Grow thick oxide, strip nitride, PE/CVD deposition of N+ polysilicon
3) Pattern poly to form gate, form sidewalls
4) Implant N+ source/drain regions, etch SO2
5) Self-aligned cobalt silicide contacts

6) Coat with SiO2, form open holes, form W via

7) Aluminum interconnects and dielectric insulators

CMOS (NMOS + PMOS) process is similar but more complex...

N-MOSFET

P-MOSFET
Varying the "size" of a MOSFET

\[ I_d = \text{constant} \times W_g \times (V_{gs} - V_{th}) \]

\[ V_S \]

\[ W_g \text{ increased} \]

\[ L_y \text{ kept constant} \]
Substrate connections - MOSFETs

There are p-n junctions from the source and drains of the n-MOSFETs to the p substrate. The p substrate must be connected to the most negative voltage in the circuit.

There are n-p junctions from the source and drains of the p-MOSFETs to the n-wells in which they sit. The n wells must be connected to the most positive voltage in the circuit.

There are depletion capacitances from the wells/substrate to the source/drain regions.
SiGe HBT process flow

1) P- wafer, form N+ buried layer, form N- collector drift layer, etch isolation trenches, fill with insulator

2) etch primary collector pedestal, replanarize by Spin-on-glass and chemical-mechanical polishing

3) grow P SiGe intrinsic base layer

4) deposit Si3N4 dummy emitter, use this to control location of growth of extrinsic base

5) remove dummy emitter, form dielectric sidewalls, implant second collector pedestal

6) grow polysilicon N+ emitter, pattern and etch

7) etch through dielectric, pattern/etch base, form new dielectric sidewalls

8) form self-aligned cobalt/tungsten silicide contacts

9) interconnect back end (W plugs, Al wiring, SiO2 dielectric)
Modern SiGe BJT

wide emitter contact: low resistance
narrow emitter junction: scaling (low $R_{bb}/A_e$)

thick extrinsic base: low resistance
thin intrinsic base: low transit time

wide base contacts: low resistance
narrow collector junction: low capacitance
Varying the "size" of a FET:

\[ A_E = 0.1 \times 0.5 \mu m \]

\[ I_s = \frac{g m_0 D_n \cdot A_E \times A_E}{W_6} \]

or, more precisely:

Each \( A_E = 0.1 \times 0.5 \mu m \)

\( A_E \) and \( I_s \) vary as \( A_E \) increases.
Substrate connections: 8.575

There are p-n junctions from each collector to the substrate. The p substrate must be tied to the most negative voltage in the circuit.

There is a depletion capacitance from each collector to the substrate.
To make resistors:

- These can be made from the gate polysilicon in MOS processes or the base or emitter polysilicon in bipolar processes.

- Or, they can be formed from n+ source diffusion.

- Or, through extra layers of resistive metal such as Ni:Cr alloys or W:Si:Al.

**Top View**

\[ R = 2 \cdot \text{length} + \rho \cdot \text{width} \]

\[ R = \text{thickness} \]

\[ \rho = \text{bulk resistivity} \]

Defining \( \rho_{\text{sheet}} = \rho / t \) per square

\[ R = 2 \cdot \text{length} + \rho_{\text{sheet}} \cdot \text{L/W} \]
Resistors made from semiconductor layers
- vary with temperature considerably
- have poor absolute tolerance
  (doping & thickness & linewidth variations)

Identical-geometry resistors placed close together
will have matching of a few %

Sheet resistivities are in the range of 10-100 Ω/□
The 10 Ω value is typical of thicker, heavily doped
layers. Large resistance values therefore
require very large L/W ratios, and
consume large IC areas.
On a bipolar IC

- Transistors are small & cheap.
- Transistors of identical dc will have similar Is
- Transistors obey $I = I_s e^{g V_{BE} / (kT)}$
  - Exploit this to control currents!

- Resistors formed from silicon layers
  - are not high in absolute precision
  - are somewhat better, but not great, in matching
- Have parasitic capacitance to substrate

Resistors formed from thin metal films

- Can be added at added cost
- Are more precise → ADC processes etc
- Low sheet resistance → low values only.

Capacitors of more than a few pF are very large and therefore very expensive
Capacitors:

Capacitance per unit area.

S: O₂: \( E_r = 3.8 \)

S: N₂: \( E_r = 7.5 \)

\[ C = \varepsilon \frac{A}{t} = (E_r \varepsilon_0 t) \cdot A \]

\( C_{1A} = 0.34 \text{ pF/µm}^2 \) for a 1000Å thick SiO₂ layer

A 1 pF capacitor would have an area of 55x55 µm

A 100 pF capacitor would be 550x550 µm
Consequences: IC design

In most analog applications, resistors and capacitors use should be minimized. Biasing is therefore DC coupled and bias currents supplied by current mirrors

In Radio-Frequency IC designs, inductors and capacitors and resistors are key components determining IC performance. In these ICs, passive element quality is key, and IC density is constrained by the large size of these elements.
Conclusions: IC design

- Transistors are small = cheap
- BJTs of identical size will match well in Vce, but not β.
- MOSFETs of identical size will match reasonably in Vds, but Cov, Wg, and Vt.

But

Resistor absolute precision is poor
Resistor matching is reasonable
Large resistor values are large area = very expensive

=> Avoid using large resistors whenever possible

Capacitors above 1μF are very large and very expensive
Ratios in current mirrors

(transistor with emitter area = 2Ae)

(transistor with emitter area = Ae)

Notation:

\[ A_0 \rightarrow \frac{A_0}{A_e} \rightarrow \frac{A_0}{A_e} \rightarrow (2) \]