Problem 1: The supplies are +/- 5 V. The transistors all have beta=750 and Va=100 Volts. The Emitter resistors (Re3 and Re4, Ree8, Ree9) all have 200 mV DC voltage drop. Ri=10 kOhm. RL=1 kOhm. Ree5=Ree6=50 Ohm

The DC input voltages are 0 V, the DC output voltage is to be 0 V. Q1 and Q2 are biased at 200 uA, Q5 and Q6 at 0.5 mA, and Q7 at 5 mA. Q9 has a Vce of 0.7 Volts. Find all bias values, all resistor values, the differential and common-mode voltage gains, the CMRR, and the output impedance.

Problem 2:
The NMOS FETS have
\[ K_\mu = 10 \text{mA/V}^2 \cdot \left( \frac{W}{L} \right) \mu \text{m} \]
\[ K_s = 2.0 \text{mA/V} \cdot \left( \frac{W}{L} \right) \mu \text{m} \]
\[ \Delta V = 100 \text{mV}, \frac{1}{\lambda} = 5 \text{ Volts, and a } 0.25 \text{ V threshold. The PMOS FETs are the same. The sign of the PMOS threshold voltage is of course reversed.} \]

The FETs are to all operate at Id1=Id2=25 uA, Id5=Id6 Id8=Id9=50 uA. Ic3=Ic4. Ic10=1mA. Pick the FET widths so that all FETs operate at Vgs corresponding to the boundary between mobility-limited and velocity-limited operation.

The voltage drops across Re3 and Re4 are 150 mV. The supplies are +/- 2 V, and the gates of Q8 and Q9 are at +0.5 V. The load is 3000 Ohms

Vin- and Vin+ are at zero volts DC, as is Vout. The BJTs have beta=200. RgA is 1 MOhm.