

ECE137b First Design Project Option

Update 4/21/15

You must purchase lead-free solder from the electronics shop. Do not purchase solder elsewhere, as it will likely be tin/lead solder, which is toxic. "Solder-sucker" desoldering tools are not permitted in the lab, as they disperse a dust of solder granules into the air and onto surrounding surfaces. If you are also foolishly using tin/lead solder, you will then poison yourself. Again, use lead-free solder from the shop, and use desoldering wick to remove solder. Projects assembled using lead-containing solder will receive a grade of zero.

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General Comments

You have a choice of doing one of three design projects, a fiber optic link, a switched mode power amplifier, or an acoustic phased array. All are intended to be

-Representative of real applications, incorporating aspects of both circuit and system design.

- Highly independent in character. It is strongly expected that there should be minimal similarity between projects designed by different groups.

-A significant fraction of the class grade and hence a significant time commitment

You will be working in groups of 2.

Construction Hints

These are high frequency circuits. Construction on a proto-board is of value for DC testing and for AC functional testing at signal frequency well below that of the real design. Functional high speed operation will require a soldered design with tight physical construction practices. Construction on a circuit board with a ground plane is very strongly recommended, as is signal wiring with adhesive copper tape. See the 137a web site for information on construction practices.

Pulse width Digital Amplification

You have previously studied power amplifiers in 137a, including a lab project and the material in the notes. Class A power amplifiers, those in which a single transistor is on for the whole signal cycle, are at an absolute maximum 50% efficient, while class AB push pull power amplifiers can reach at maximum a theoretical efficiency of $\pi/4$, a little over 75%. This efficiency is only approached when the amplifier is delivering its maximum output power, and efficiency drops off considerably when the output power is below the maximum.

A very large fraction of the total cost of a power amplifier is in the power transistors, the heat sinks used to cool them, and in the transformer, diodes, and capacitors within the power supply. Increasing the efficiency towards 100% can dramatically reduce the cost and size. Improved battery life through increased efficiency is of substantial importance in portable devices, including audio systems of laptop computers, portable MP3 players, and car audio systems. Most now use digital audio power amplifiers.

The modern method of obtaining near-100% efficiency is the switched-mode amplifier. An idealized zero-resistance switch can dissipate zero power... power is $V \cdot I$, and an open switch has zero current while a closed switch has zero voltage. The challenge is to convert such a digital on-off output into an analog signal. The general concept is below (Figure 1). This switch circuit, plus a filter, can produce a sine wave with 100% efficiency. To produce an arbitrary output waveform, we must use a pulse-width-modulated digital drive waveform.

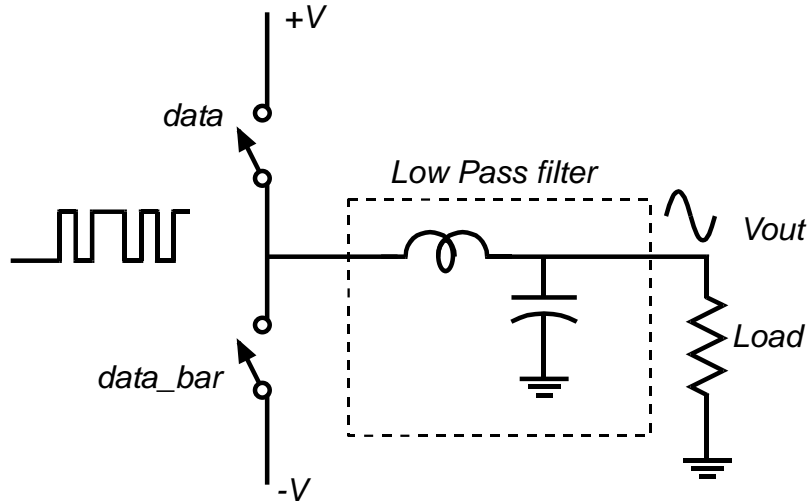


Figure 1: Generating a sine wave with 100% efficiency

Basic Pulse Width Modulation

The basic Pulse Width Modulator is illustrated in Figure 2.

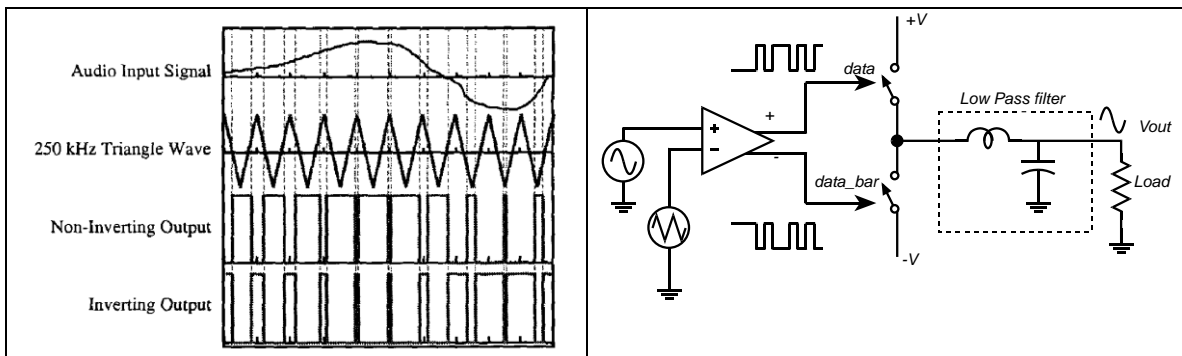


Figure 2: Pulse-width modulation amplifier.

In Figure 2, a high gain comparator (the op-amp-like symbol is a comparator, not an amplifier) is used to compare the input signal to a high frequency triangle wave at perhaps 250 kHz. In a comparator, digital output voltages (high or low) are generated if the differential input is positive or negative. The comparator output is thus a 250 kHz pulse train whose pulse width is proportional to the input voltage. This assumes that the input signal frequency is far below 250 kHz. The low pass filtered output is then a faithful representation of the input signal. This configuration, sometimes known as class D (confusingly, the term also used for a completely different RF amplifier configuration), is widely used in low-frequency high-power linear amplifiers in many applications, including Audio. Much more complex implementations of this, incorporating both negative feedback and pulse width modulation by high speed digital techniques, are now used in modern audio power amplifiers. The March 2003 Issue of IEEE Spectrum has an article on such amplifiers. Or, see [Wikipedia](#).

A simple pulse-width modulator is as below (Figure 3). This simply converts the input to a pulse-width-modulated waveform.

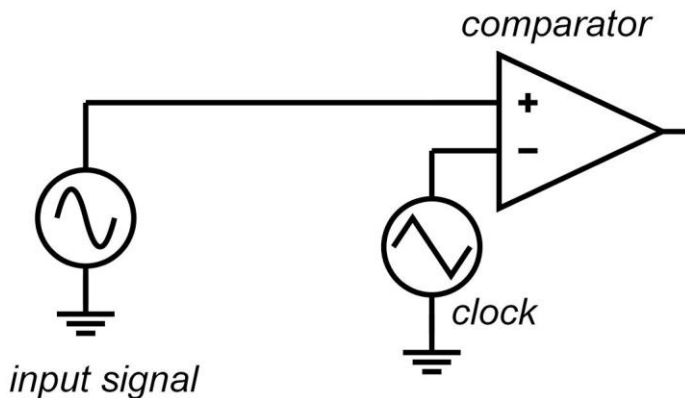


Figure 3: basic pulse-width modulator

A pulse-width-modulation *amplifier* (Figure 4) consists of the pulse-width-modulator driving a pair of power MOSFETs as the power switch. High speed pulse driver circuits are needed to (1) generate the correct voltages to drive the power FETs and (2) produce sufficiently fast rise and falltime waveforms in the presence of large MOSFET input capacitances. Finally, the low-pass-filter converts the pulse-width-modulated square wave back to the AC signal waveform of interest. Please note that if the triangle wave has a voltage swing of $\pm V_{\max}$, then when the input signal is V_{\max} the output will be $-V_{DD}$, while when the input signal is $-V_{\max}$ the output will be V_{DD} . Consequently, the circuit has a voltage gain of $A_{pwa} = -V_{DD}/V_{\max}$. We can easily change the sign by interchanging the two inputs of the comparator.

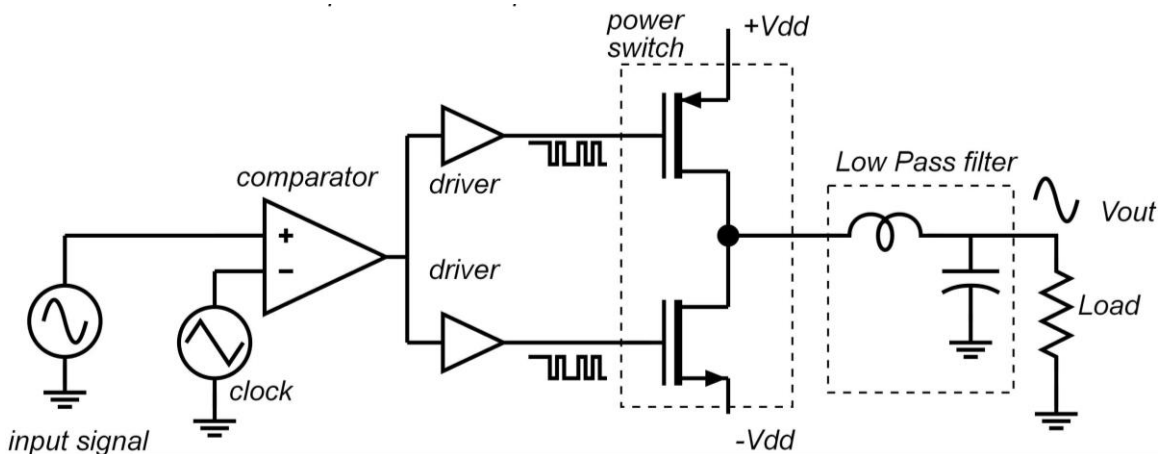


Figure 4: Pulse-width-modulation amplifier.

The amplifier will have various distortions. We can suppress these to some extent using negative feedback. First, let us model this approximately. In Figure 5 we have modeled the pulse width amplifier as a gain block with gain $A_{pwa} = -V_{DD}/V_{\max}$, plus a summation of an error (distortion) signal V_{error} . The circuit of Figure 5 has a feedback loop

transmission of approximately $T(s) = A_{pwa}(1 + sR_zC) / sR_2C$; the main function is an integration, and there might also be a zero for phase-lead ("lead") compensation of the feedback loop. Analysis of this system would give:

$$V_{out}(s) = \frac{-R_2}{R_1} \frac{T(s)}{1+T(s)} V_{gen}(s) + \frac{1}{1+T(s)} V_{error}(s)$$

Defining the loop bandwidth f_{loop} by $\|T(j2\pi f_{loop})\|=1$, at frequencies well below f_{loop} , $\|T(j2\pi f)\| \gg 1$, and the error (distortion) voltage is suppressed.

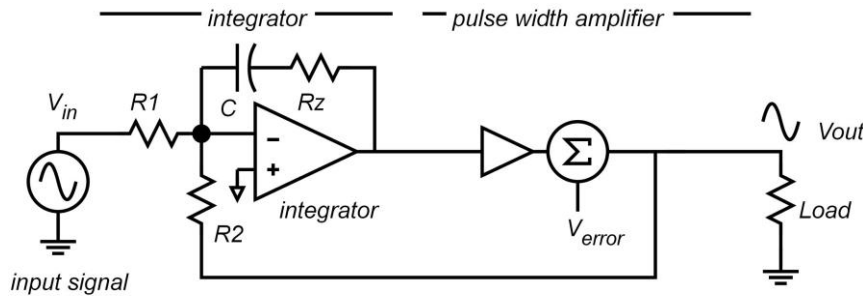


Figure 5: Modeling the effect of negative feedback

Figure 6 shows a block diagram with the driver amplifiers.

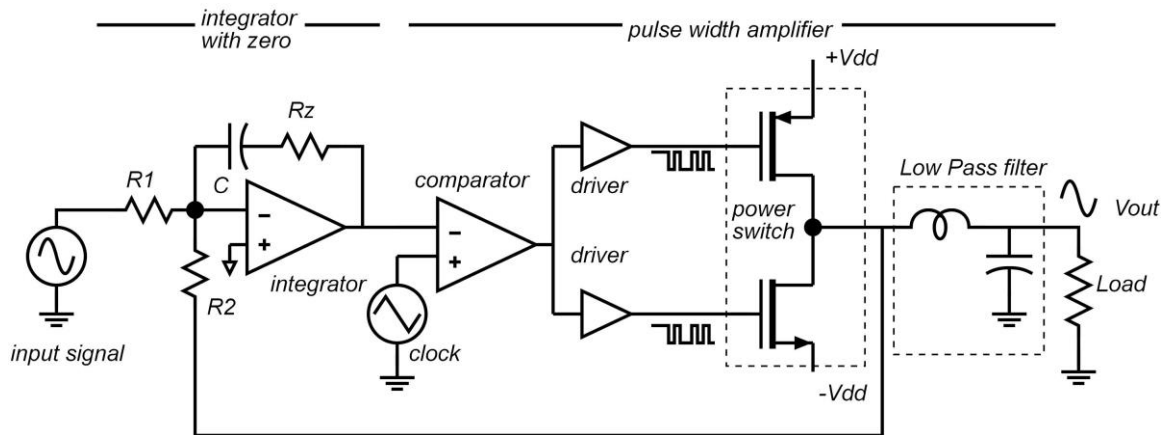


Figure 6: Pulse-width-modulation amplifier with negative feedback

Figure 7 shows a second feedback loop design with *two* integrators in the feedback loop. This increases $T(j2\pi f)$ at frequencies of interest, providing better suppression of the error signal. This circuit needs careful design. Please note that you should use *fast* op-amps for the two integrators. Perhaps the TL074, possibly even the AD8031 or AD8032, though this may be excessive.

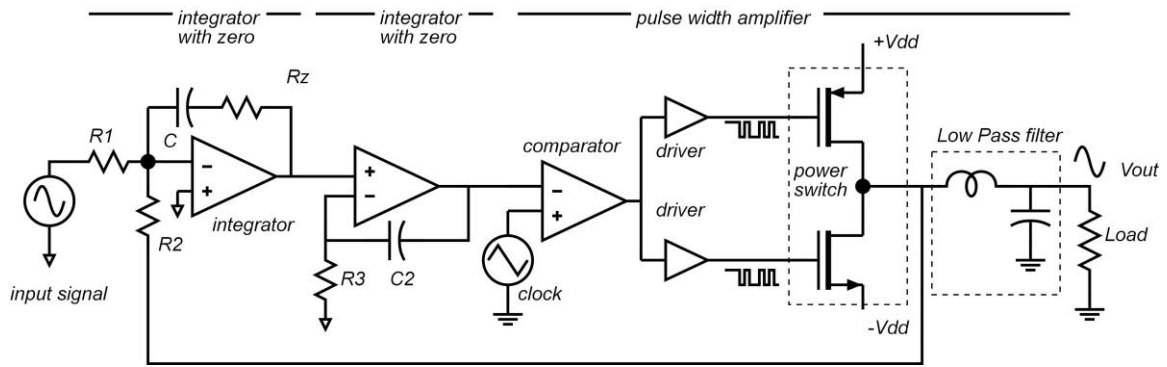


Figure 7: Pulse-width-modulation amplifier with more sophisticated negative feedback

Pulse driver circuit: challenges.

The pulse driver is the key circuit design challenge. First, the two power MOSFETs have some on-resistance which depends upon V_{gs} . If this on-resistance is significant, there will be a voltage drop across the MOSFET when the FET is on. This will cause power dissipation in the FET, making it hot and reducing the circuit efficiency. From the data sheet you will be able to determine the necessary drive voltages.

The drive waveforms must be *fast*. If the risetime of the waveform driving the power FETs are long, then the FETs will be in a moderate-resistance state for some time. Again, there will be dissipation in the power FETs.

The drive waveforms must not *overlap*. If the drive waveforms for the N-FET and PFET result in the FETs being on at the same time during the switching transient, then a temporary yet very large pulse of current will flow through the two transistors. This will again heat the power FETs and impair efficiency.

The goal, then, is to design pulse drivers with *fast* rise and fall times and *non-overlapping* waveforms. Please note that these need to be *switching* stages: this are high-gain amplifiers which are driven into clipping to set their high and low voltage values. For MOSFETs, either knee voltage or cutoff is acceptable to set the low and high voltage levels. For normal bipolar transistors (but not double-heterojunction bipolar transistors) minority carrier storage in saturation causes slow switching, and you must avoid saturation, using only cutoff to set low and high voltage levels.

Noting that you will likely use the IRFU014 IRFU9014 for the output FETs, below I give a couple of rough sketches of pulse driver designs. There is much to consider in the design of these, and you will have to carefully analyze the DC, clipping (high and low) levels, and switching times. Or, better still, create your own design ! In Figure 8 and Figure 9, the resistor R_x provides unequal turn-on/turn-off times, providing the desired non-overlapping waveforms. In Figure 8, the resistors R_y are necessary to prevent the emitter-followers from oscillating. This, again, requires analysis. In Figure 8, the diodes in the differential pair are necessary to prevent reverse breakdown of the base-emitter

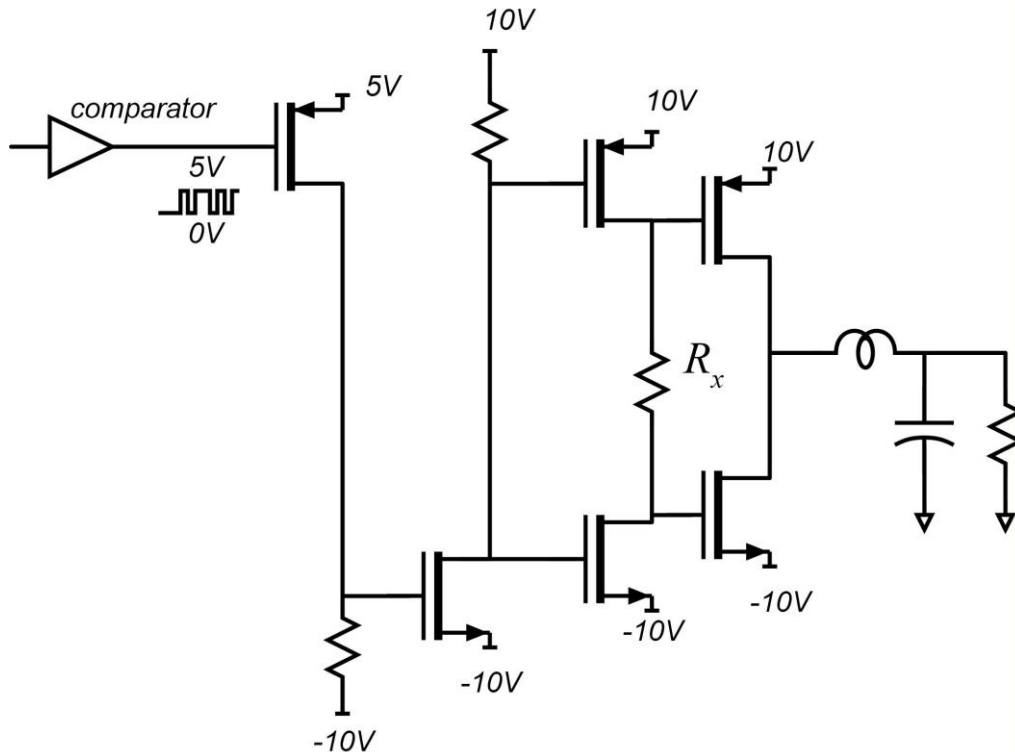
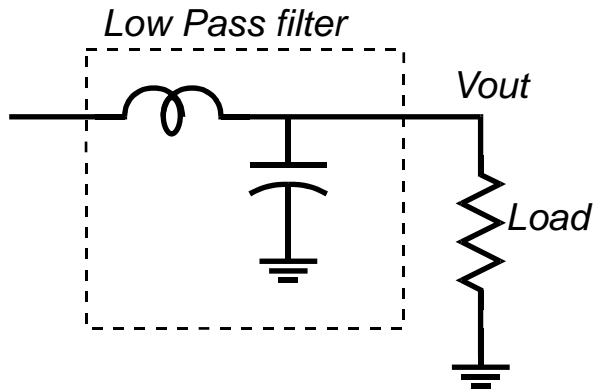


Figure 9: Example FET pulse driver for the FET output stage

Overall switching speed of the pulse driver and output stage will determine your maximum clock frequency, which will in turn determine the feasible signal/(quantization noise) performance of the ADC and the maximum useful signal bandwidth. Ideally, for audio (20 Hz-20 kHz) operation with 2nd-order noise shaping (Figure 7), a switching frequency of 500kHz, 1 MHz would be desired. Such a high clock frequency may be quite difficult to obtain with the available power MOSFETs. In that case, you must design for the highest switching frequency you find feasible. You must carefully analyze your drive stage in terms of the drive voltages required to turn the transistors on at the required operating current level (specifically, the on-state resistance as a function of V_{gs}), the rate at which the input capacitance C_{gs} of the MOSFETs can be charged [$I = C(dV/dt)$], and the amount of power wasted charging and discharging the input capacitances. You need to be careful to ensure that the 2 power mosfets are not simultaneously turned ON except momentarily during the switching transients.

Low-pass filter



There is also an output low-pass filter. It is essential that the input impedance be high at frequencies above its cutoff frequency; otherwise, the switch output stage will be short-circuited. Design this low-pass filter to have a natural resonant frequency of 30-40 kHz and a damping factor of 0.6. The load impedance is 8 Ohms (a loudspeaker). You can purchase some values of inductors from the ECE electronic shop, or you can wind your own, wrapping solid copper ("magnet") wire around a dowel core (purchased at a local hardware store), and then removing the dowel. For this, please either see your physics textbook, or see

http://www.colomar.com/Shavano/inductor_info.html

<http://www.arrl.org/files/file/Technology/tis/info/pdf/9708033.pdf>

<http://en.wikipedia.org/wiki/Inductor>

Matlab simulation

On the main class web site there is matlab code for simulating the loop and its SNR and gain. You will need both the main program and the subroutines:

[hann.m raised_cos_baseband_filter2.m](#)

These must be placed in the same directory as the main program. You

Triangle-wave generator

With fast op-amps available, this can be easily constructed (Figure 10). The Schmitt trigger is a positive-feedback circuit whose output changes state between the supply voltages (say, $\pm V_{\text{supply}}$), when its input changes between $\pm V_{\text{supply}}(R_1/R_2)$. Clearly, you should make R_1 less than R_2 . The trigger output is a squarewave of amplitude $\pm V_{\text{supply}}$; this is then integrated with a time constant R_3C . The output is a triangle wave of amplitude $\pm V_{\text{max}} = \pm V_{\text{supply}}(R_1/R_2)$ and frequency $f = (R_2/4R_1R_3C)$. It is optional, but please consider constructing this as part of your design.

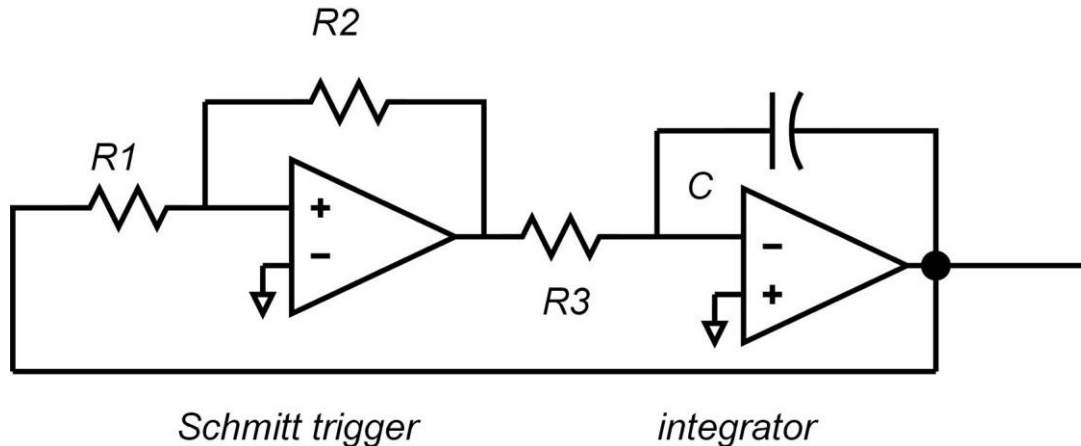


Figure 10: Triangle-wave generator

The specific assignment

Your objective is to obtain

- A high output power into an 8 Ohm load. As high as is feasible, with the constraint that the supply voltage on the switch shall not exceed + and - 15 Volts.
- A high clock frequency. This is to obtain high suppression of quantization noise. The 137b lab does not, unfortunately, have the equipment to measure quantization noise, hence the clock frequency will instead be used as a direct measure of performance.
- A second order loop is preferable to a first order loop.
- As high a circuit bandwidth as is feasible, up to the 30-40 kHz limit specified by the filter network.

The latched comparator runs from *****4***** power supply connections. These are +Vss, -Vss, Vlogic, and ground. +Vss and -Vss can be +/-5 Volts or +/-7.5 volts, but Vlogic must be at least 4 volts and NOT more than 7 volts. I recommend either 5 or 6 volts. **The output of the comparator is Vlogic for a high level and 0 volts for a low level. This forces the D-latch driven by the comparator to operate from a power supply whose negative lead is zero volts and whose positive voltage is +Vlogic. There is then a**

significant level-shift design challenge between the D-latch output and the power output switch.

The project has three check off dates

First Check off date:

Test the pulse width modulator alone.

Second check off date

At this point, you must have a circuit board consisting of the comparator, the drive amplifier, the power switch, and the low pass filter.

The following quantities should be measured:

1) Pulse rise time and fall time at the output of the power switch output under 2 conditions

with the low pass filter and load present.

with the switch connected directly to the load (low pass filter removed)

Based upon this rise and fall time, what is your maximum usable clock frequency ? One would like the rise and fall times to be less than 10% of the clock period

2) Peak-peak output voltage into the load. A first estimate of the power amplifier maximum output would be

$$P_{\max, \text{estimated}} = (V_{pp})^2 / 8R_{load}$$

3) Wasted switching power. With the test setup above, and with the low pass filter removed, and no load connected, how much power does the circuit dissipate as a function of the clock frequency ? This will vary as a function of clock frequency due to the current expended charging and discharging the MOSFET capacitances.

You will measure the DC supply voltage and DC supply current to determine the power consumed by the circuit. You will measure the load voltage and load resistance to determine the output power.

Your objectives are to get the best possible clock frequency, output power, and minimum wasted switching power.

Third check off date

At this point, MATLAB simulations should have been run, so feasible performance as a function of loop bandwidth is understood. Secondly, op-amp integrators should have been designed, constructed, and tested. Finally, at this point, you have completed the full circuit. ***In connecting the loop, please be very careful to connect it with the correct***

(negative) sign for the feedback. This will require you to examine the sign of the gain of each stage in the loop.

You will measure the full circuit (Figure 6 or Figure 7, or your own feedback loop design).

The measurements are as follows

- 1) Circuit gain at low frequencies. V_{out}/V_{in} as a function of frequency with a 0.1 Vpp output. Bandwidth should ideally be limited by the output filter.
- 2) Maximum undistorted peak-peak output voltage measured at 100 Hz, and 1,5, 10 & 20 kHz
- 3) Power dissipation with zero input signal.
- 4) Power dissipation as a function of output power with a 1 kHz output signal. From this, efficiency as a function of output power.
- 5) Matlab simulations of the overall loop should be turned in at this point. These should document the required unity gain frequency for the integrator, expected signal levels, expected SNR.
- 6) Some attempt should be made to measure the signal to distortion ratio. Unfortunately, without a spectrum analyzer, this will be subjective.

At this point the full report is due, including the design and measurements of the power switch, the op-amp integrators, the matlab simulations, and the full system measurements.

References on Class D Audio Power Amplifiers

You can download the papers below by accessing IEEE_explore
<http://ieeexplore.ieee.org/Xplore/DynWel.jsp> from a computer within the UCSB network.
Outside UCSB, this cannot be accessed.

It is also helpful to search the web for class D audio etc

A power-efficient audio amplifier combining switching and linear techniques

van der Zee, R.A.R.; van Tuijl, E.A.J.M.;

Solid-State Circuits, IEEE Journal of, Volume: 34 Issue: 7, Jul 1999

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12 V Σ - Δ class-D amplifier in 5 V CMOS technology

Ballan, H.; Declercq, M.;

Custom Integrated Circuits Conference, 1995., Proceedings of the IEEE 1995, 1-4
May 1995

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PowerDAC: a single-chip audio DAC with a 70%-efficient power stage in 0.5 μ m CMOS

Philips, K.; van den Homberg, J.; Dijkmans, C.;

Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999 IEEE
International, 1999

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A 3.3 V/1 W class D audio power amplifier with 103 dB DR and 90% efficiency

Tousi, V.M.; Sahandi, F.; Atarodi, M.; Shojaei, M.;

Microelectronics, 2002. MIEL 2002. 23rd International Conference on, Volume: 2,
2002

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Class-d audio amplifiers with separated baseband for low-power mobile applications

Streitenberger, M.; Felgenhauer, F.; Bresch, H.; Mathis, W.;

Circuits and Systems for Communications, 2002. Proceedings. ICCSC '02. 1st IEEE
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Class d audio power amplifier with fine hysteresis control

Sang-Hwa Jung; Nam-In Kim; Gyu-Hyeong Cho;

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Digital control circuit for class-D audio power amplifier

Sozanski, K.P.; Strzelecki, R.; Fedyczak, Z.;

Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual,
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Zero-position coding with separated baseband in low-power class-D audio amplifiers for mobile communications

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Reducing distortion of audio class D (PWM) power amplifier by using feed-forward techniques

Shuanghe Zhu; Caizhang Lin;

Circuits and Systems, 2000. IEEE APCCAS 2000. The 2000 IEEE Asia-Pacific

Conference on , 2000

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Class-D audio power amplifiers: an overview

Dapkus, D.;

Consumer Electronics, 2000. ICCE. 2000 Digest of Technical Papers. International Conference on , 2000

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