Overview

Goals:
(a) Learning how to measure S-parameters of active devices, including reference plane offset techniques
(b) Obtaining data which you can use for later lab projects!

Safety Precautions:
(a) Observe static precautions when working with the network analyzer. Wear the wrist strap.
(b) Never connect a network analyzer directly to a circuit carrying dc. Make sure your circuit is dc blocked, or you will destroy the NA.

Reading:
Refer to HP 8751A Network Analyzer User’s Guide (RBR and in lab - do not remove!)
Transistor RF Characterization.

Use either an MRF901 or MRF951 bipolar transistor for this lab.

DC bias circuits

To provide gain, transistors must be provided DC bias currents and voltages. These bias circuits are built into normal amplifier designs. To simplify transistor measurements, and to prevent the bias circuits from corrupting the measurements, NWAs have internal bias networks (bias Tees) for transistor biasing. If you use the NWA’s internal bias Tees, and accidentally apply a short-circuit, or apply excess voltage, you will damage or destroy the instrument. So, we will not use the NWA bias Tees in this class.

Instead, we will use the bias networks of Figure 1, which shows both bipolar junction transistor BJT and HEMT (junction FET) bias circuits. Bias for a MOSFET would be similar to that of a HEMT, except for a MOSFET the gate voltage is usually positive and for a HEMT it is usually negative.

![Figure 1: Circuit Diagrams for BJT and HEMT biasing](image)
Addressing first the BJT circuit, the base is biased with a large voltage $V_{BB}$, chosen much larger than the base-emitter turn-on voltage $\phi$, ~0.7-1.0 Volts, through a bias resistor $R_B$, setting up a base current $I_B = (V_{BB} - \phi) / R_B$. The collector current is $I_C = \beta I_B$. The collector voltage is $V_{CE} = V_{CC} - I_C R_C$.

Caution: this base-current bias method is simple and easy for laboratory testing. Because production BJTs have highly variable $\beta$, base-current-biasing provides poor control of the collector current and is almost never used in production circuits. More on this in lectures!

We must talk about how to pick resistor values and how to adjust voltages. We would like the four resistors $R_B$, $R_{BX}$, $R_C$, and $R_{C,X}$ all to be much larger than the transistor parallel input/output resistance, so as to minimize the effect of measurement. If we pick $V_{BB}$ to be 10-15 Volts, then for the required base current, $R_{BX}$ will be quite large. The monitoring resistor $R_{BX}$ is made large, 100 k$\Omega$, so that it does not load the circuit. A voltmeter is connected to the other terminal of $R_{BX}$; this is used to measure the base-emitter voltage $V_{BE}$. Remember that the voltmeter has some input resistance, and the measurement of $V_{BE}$ is changed by the resulting voltage-divider between $R_{BX}$ and this input impedance.

With some collector current $I_C$, the voltage drop across $R_C$ is $I_C R_C$ and hence $V_{CE} = V_{CC} - I_C R_C$. Here we have a trade-off; large values of $R_C$ give the desired minimal circuit loading but result in a large voltage drop across the resistor; small values of $R_C$ provide heavy circuit loading, changing the measurement. Try to pick $R_C$ as large as is possible, and hence use as large a $V_{CC}$ as is possible, given the maximum allowable DC power dissipation in the resistor. Again monitoring resistor $R_{CX}$ is made large, 100 k$\Omega$, so that it does not load the circuit. Through this resistor a voltmeter measures the collector voltage.

Later in the class, when you are building a tuned microwave circuit, you will use microstrip-line tuning elements to add inductive reactance in series with the bias elements $R_B$ and $R_C$, so as to minimize their loading on the circuit. You can then measure the S-parameters of the transistor plus these bias elements, and then use these S-parameters as starting data to design the transistor impedance-matching networks.

The bias circuit for HEMTs (Schottky barrier FETs) and MOSFETs are similar. FET gate currents are tiny, so set $R_G$ at 100 k$\Omega$. The gate supply is directly adjusting $V_{GS}$. $V_{GS}$ is usually positive for MOSFETs and negative for HEMTs, but check the data sheets.

**Test fixture construction**

reference plane offset measurement
Once again, we must measure the reference plane offsets as part of the procedure. First (Figure 2) construct a 50 Ohm microstrip line on a board. At the exact center of the board, drill a small hole. This hole should no larger than the minimum needed to mount the transistor. The metal line should then be cut, separating ports 1 and 2. If done well, the metal lines reach up to the edge of the hole with zero gap whatsoever. If done well, the hole is exactly the size of the transistor package.

Figure 2: First steps in fixture construction. Through line (top), after drilling a hole (center) and after cutting the lines (bottom)

We now must measure the reference plane offset. To do this, calibrate the network analyzer, measure the board's S-parameters, and adjust the port 1 and port 2 reference
plane offsets until you have nearly a perfect open-circuit on ports 1 and 2. Record the values of these offsets.

\[ \text{Figure 3: mounting the DC blocking capacitors} \]

Then (Figure 3), make small (1mm or less) cuts in the signal conductors, very close to ports 1 and 2, and solder in place 1 microfarad DC blocking capacitors. Again, precise work is critical here.

**Fixture construction**

Figure 4 shows details of fixture construction. Mount the *leaded* (not chip) resistors vertically as shown. By mounting them vertically, centered in the microstrip line, capacitive loading from the resistor body to the ground plane is minimized. The long vertical wire lead, raised far above the ground plane, on the "cold" (no RF) side of the resistor adds series inductance, further reducing the resistive loading. The cold side of the resistor is grounded with a chip capacitor, copper pad, and via made by drilling a narrow hold in the board, running a wire through (think: inductance) and soldering it in place.

Figure 4 also shows transistor mounting. Emitter (or source) lead inductance should be made very small, so the hole is the board is very small, the transistor is mounted close to the ground plane side, and the leads are bent and soldered in place.
The key is again tight control of dimensions. In the signal path (the microstrip lines, the transistor leads, the DC blocking capacitances, the launcher tabs) we need keep lead lengths between microstrip lines less than 1mm. In the resistor paths, we are trying to create large series inductance (hence the elevated "cold" leads to the resistors) and are trying to minimize shunt capacitive loading from the resistor bodies to the ground plane, hence the vertical resistor mounting which keeps the resistor body far from the ground plane.

Note also (Figure 5), that the bias networks should be as close to the transistor as possible. In particular, the collector resistor $R_c$ should be within 1/8 inch of the transistor end of the microstrip. If this is not done, your measurements from this lab will not be useful for the next lab project, and you will have to re-do your measurements later.
Figure 5: The bias networks should be as close to the transistor as possible.

Note that for resistors in series with (as opposed to in shunt to) the RF signal path, the series inductance must be minimized. In that case we would use leadless chip resistors mounted flush to the PC board, soldered across a narrow gap in the microstrip line.

Assignment

You must construct the above fixture, mounting the transistor MRF-901, and choosing resistor values appropriate to bias the transistor at 10 mA collector current and 5 Volts collector-emitter voltage. Use a collector resistance of 500 Ohms; this will result in 5 Volts drop across the resistor (and a small 50mW power dissipation in it). The 500 Ohm parallel loading on the collector should have only a small effect on the transistor S-parameters at high frequencies. Note that these bias conditions are the same as those used in the data sheet. Calibrate the instrument (reference plane offsets must be zero when you do this), dial in the reference plane offsets, and measure and store the resulting S-parameters for future use. Make a Bode plot (dB magnitude vs. log frequency) of the maximum available/maximum stable gain. Make a similar plot of $20\log_{10}(|H_{21}|)$ vs. log frequency, manually entering the $20\log_{10}(|H_{21}|)$ expression rather than using the dB function, as ADS will in error use $10\log_{10}(|H_{21}|)$ if you ask for its dB magnitude. From this, attempt to determine the current-gain and power-gain cutoff frequencies.

You should now compare your measurement with the available transistor data. One source is the table of S-parameters on the data sheet. Use ADS to make plots of the
transistor S-parameters from the data sheet table of S-parameters. Compare your measurements to these models.

*Keep your measured S-parameters, and your board: you will use it for later lab projects.*