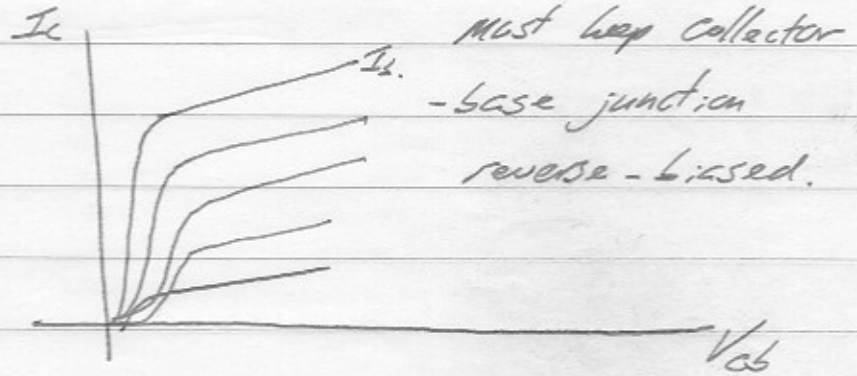
Power Considerations

Hard Limits

bipolar: $I_C = I_{es} e^{V_{be}/V_T}$ → I_C can't go negative

$$I_C = I_{es} e^{V_{be}/V_T} - \alpha_R I_{cs} e^{V_{bc}/V_T}$$

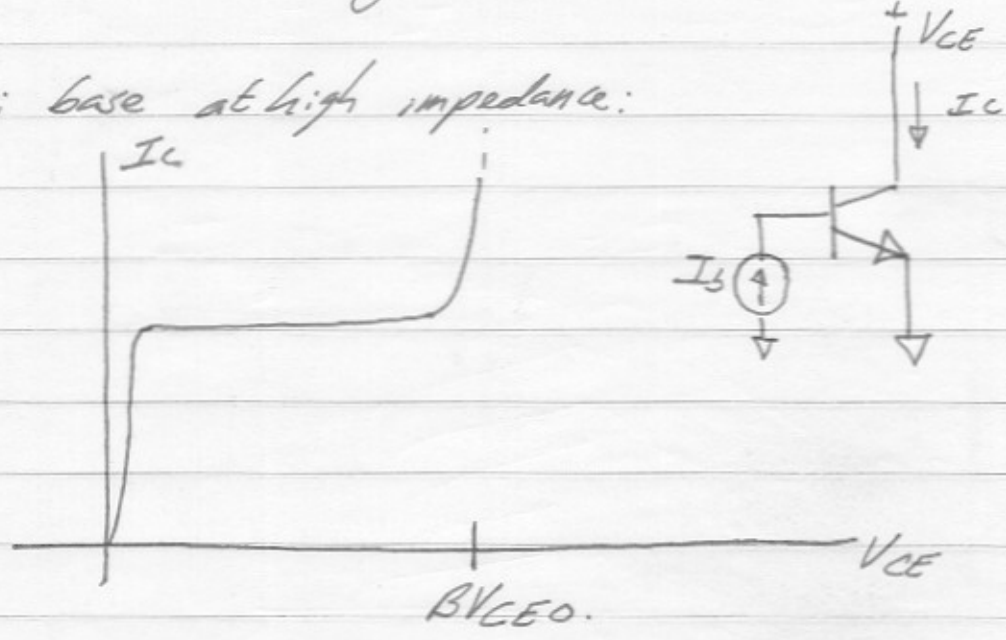


these two limits are called cutoff and saturation.

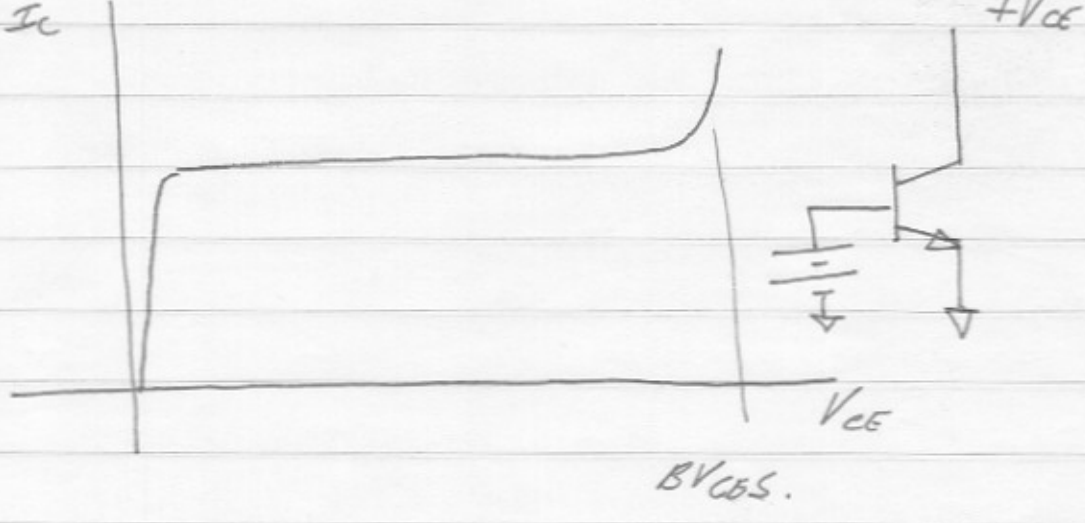
Additional limits:

Maximum collector voltage:

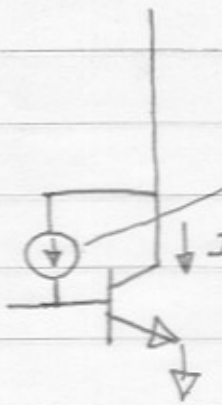
Case 1; base at high impedance:



Case 2; base at low (near zero) impedance.



Difference is in the current gain of the transistor:



avalanche multiplication factor $= M(V_{CB})$

$$\cong \frac{1}{1 - [|V_{CB}|/BV_{CBO}]^n}$$

$2 < n < 6$

empirically.

Collector-base breakdown with base shorted at BV_{CBO}.
Breakdown when $M = \infty$

When: $I_{B_{ex}} = I_{AV} - I_{B,int} = 0$; V_{CEO} occurs.

$= MI_C - \frac{I_C}{\beta} \Rightarrow V_{CEO}$ when $M = 1/\beta$.

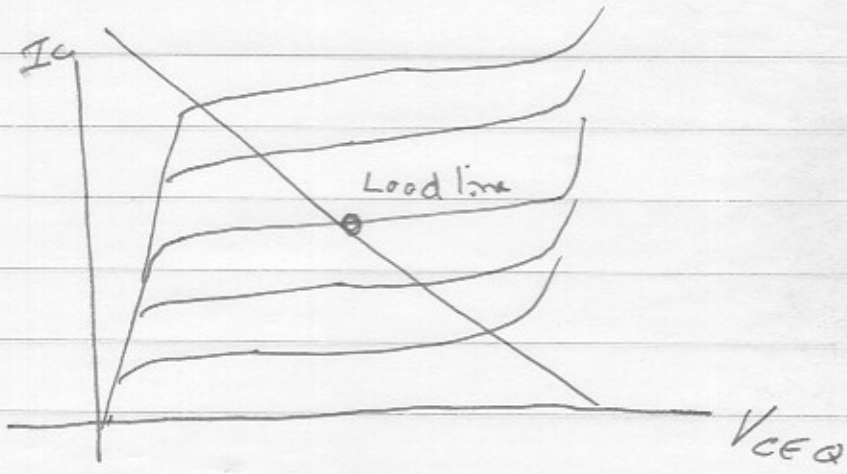
Current limits:

Power dissipation.

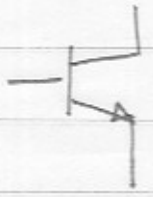
1. High-level effects: Kirk effect (base pushout)

High-level injection in base.

Power limits (heating).



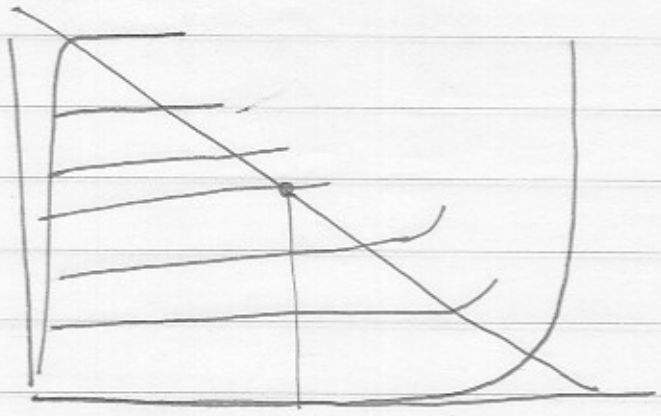
How so for CE stage:



Maximum positive swing set by:
- difference between bias and breakdown.
- inability to reverse transistor current
$\Delta V_{out} \uparrow = I_{CQ} \times R_{LOAD}$.

Maximum Negative Swing set by:
- Quiescent voltage - CE saturation voltage.
- Any limits on I_C.

Best loadline:

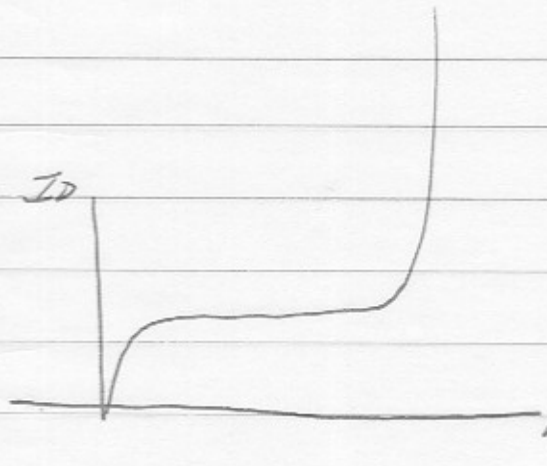


bias point
midway between breakdown & saturation.

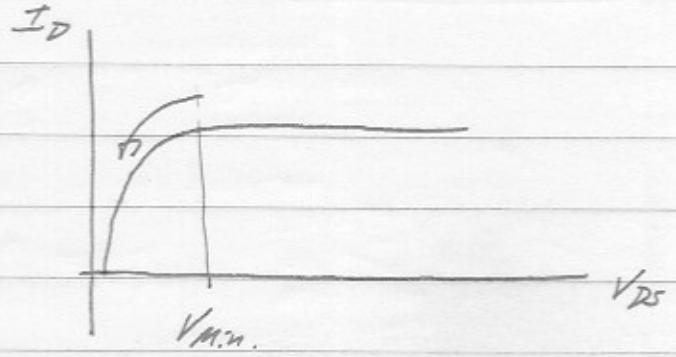
FETS:

Limits are

Breakdown,
upper V_{ds} limit.

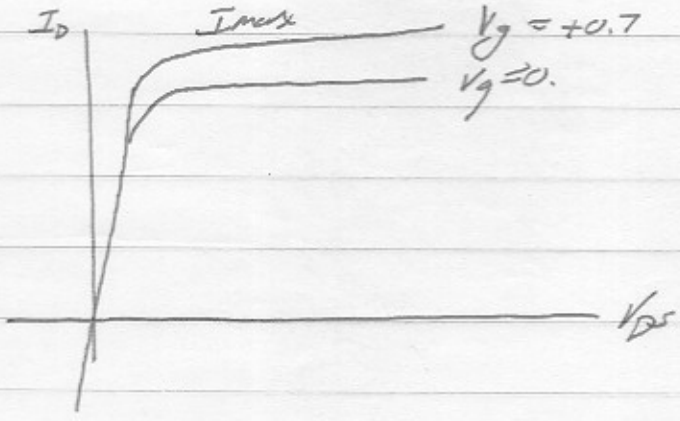


Output Knee;
lower V_{DS} limit.



Input Diode

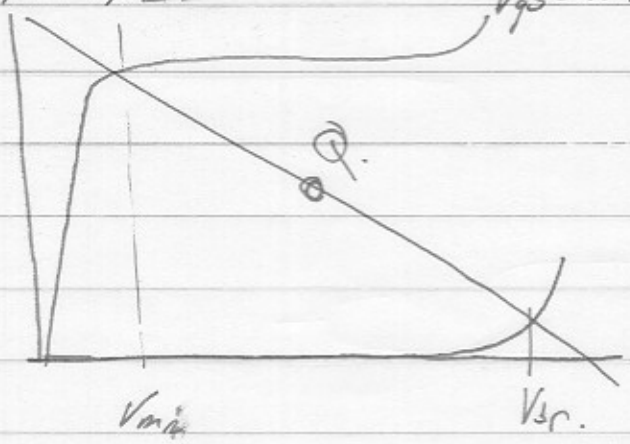
$V_{gs\,max} \cong 0.7\,V$
upper limit on V_{gs}
$\Rightarrow$ upper limit on I_D



Pinchoff

I_D can't be negative
lower limit on I_D
upper limit on V_{gs}

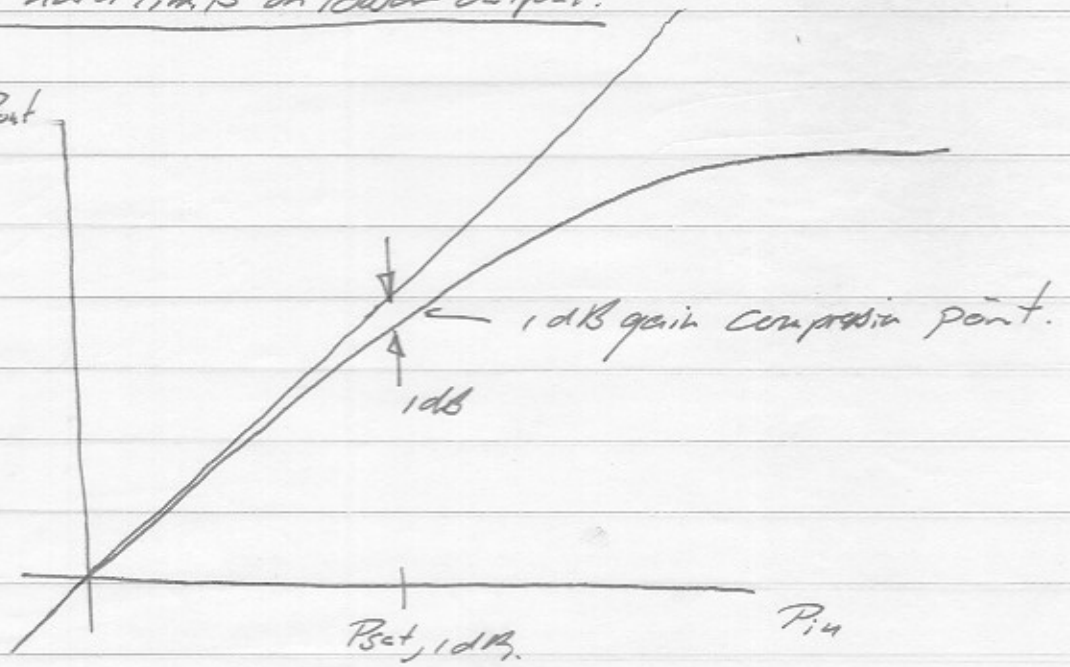
Best loadline for FET



$$P_{max} = \frac{1}{8}(V_{br} - V_{min})(I_{max})$$

$$\text{if } R_L = \frac{V_{br} - V_{min}}{I_{max}}$$

These are hard limits on Power output:



third-order intercept:

small nonlinearities: $I_d \cong I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2$ Fet.

$$\delta I_d \cong g_m \delta V_{gs} + K \delta V_{gs}^2 + \dots$$

$$I_c = \alpha I_e e^{V_{be}/V_t} \quad \text{BJT}$$

$$\delta I_c \cong g_m V_{be} + K_2 \delta V_{be}^2 + K_3 \delta V_{be}^3 + \dots$$

C_{be}, C_{gs}, C_{gd}, C_{cb} all vary with voltage.

$$C_{be} = C_{be_{diff}} + C_{be_{diff}} + \tau_f \frac{\partial g_m}{\partial I_c} \frac{\partial I_c}{\partial V_{be}} \delta V_{be}$$

$$C_{cb} = C_{cbo} / (1 + V_{cb}/\phi)^{1/2}, \text{ if uniform doping.}$$

General Circuit has some "taylor series" behavior.

$$V_{out} = A_v V_{in} + K_1 V_{in}^2 + K_2 V_{in}^3 + \cdots$$ to an amp.

↑ Not really general enough: nonlinear capacitors give nonlinear terms which have phase shifts, etc

If input signal is sinewave $\left(e^{\pm j\omega_0 t}\right)$

$$A_v V_{in} \rightarrow A_v e^{\pm j\omega_0 t} V_i$$

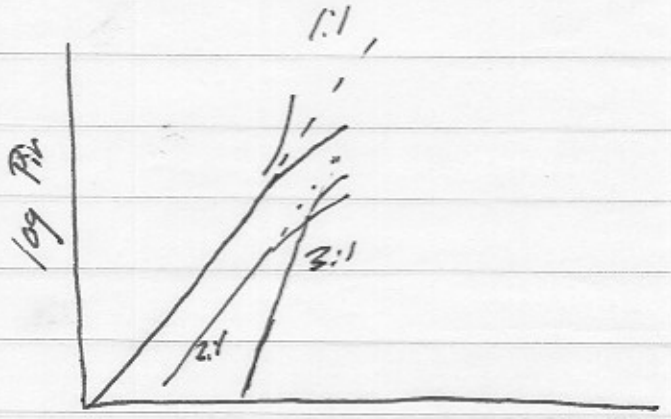
$$K_1 V_{in}^2 \rightarrow A_v \left(e^{j\omega_0 t} + e^{-j\omega_0 t}\right)^2 V_i^2$$

terms at dc and at $e^{\pm j2\omega_0 t}$

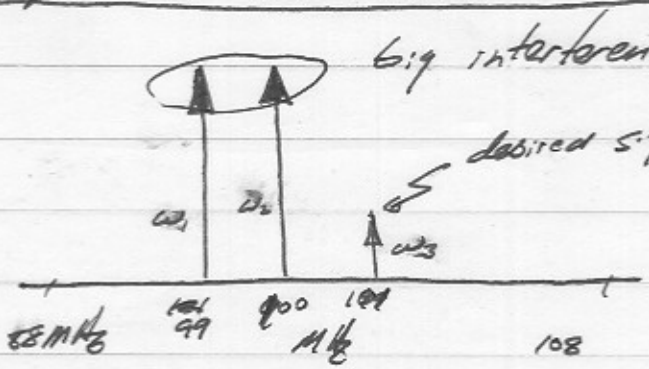
proportional to V_{in}^2

$K_2 V_{in}^3 \rightarrow$ terms at $e^{\pm j\omega_0 t}$ & $e^{\pm j3\omega_0 t}$

proportional to V_{in}^3.



Real problem in communication



$$V_{in} = v_1\left(e^{\pm j\omega_1 t}\right) + v_2\left(e^{\pm j\omega_2 t}\right) \qquad v_1 = v_2.$$

Quadratic term gives responses at DC and $\pm\omega_1 \pm \omega_2$

$\Rightarrow$ 1 MHz, 201 MHz

$\rightarrow$ outside band, Filtered out.

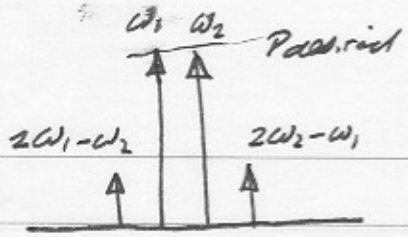
Cubic term gives responses at ω_3

$$v_1\left(e^{\pm j\omega_1 t} + e^{-j\omega_1 t} + e^{+j\omega_2 t} + e^{-j\omega_2 t}\right)^3$$

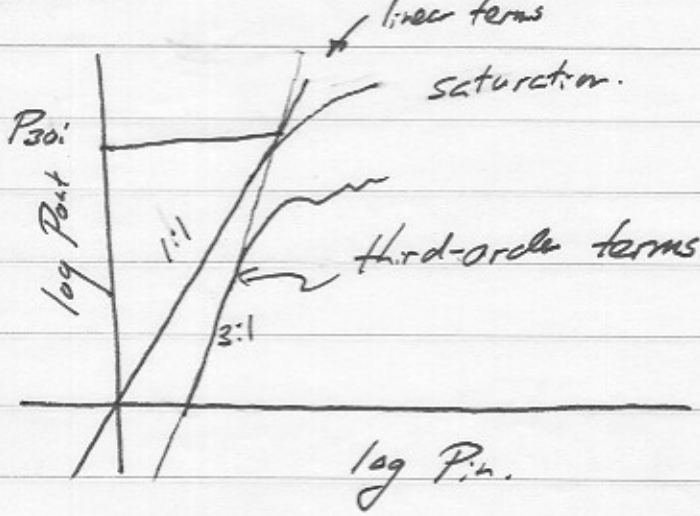
$\rightarrow$ responses at ω_1, ω_2 (dont care)

and at ω_3 $\quad e^{j\omega_2 t} e^{j\omega_2 t} e^{-j\omega_1 t} \rightarrow$ 101 MHz.

$\Rightarrow$ interference with desired signal.



Increasing Input Power:



for $P << P_{3oi}$

$$\{P_{desired} - P_{undesired}\}(dB) = 2\{P_{desired} - P_{3oi}\}.$$