ECE202A Fall 1999, EESOF introductory exercise #1.

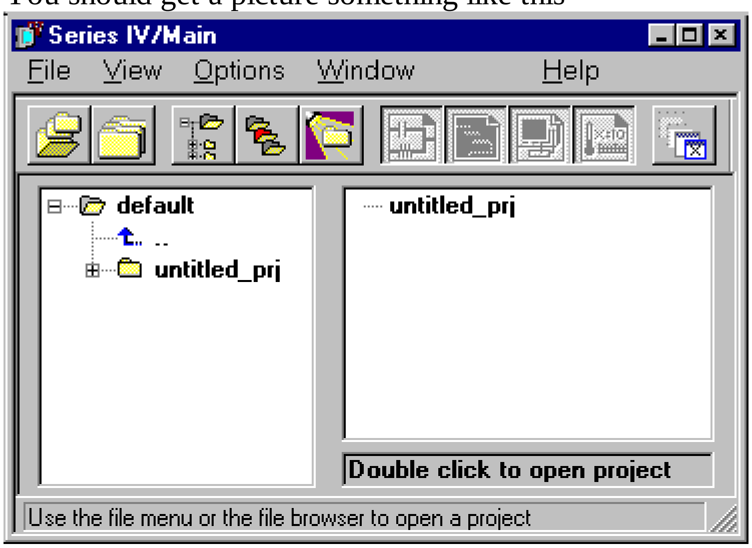
I have put (and will put more) eesof project directories on my PC in the FTP download directory.

These are presently EESOF (not ADS) directories

The first of these is called logic_fam_prj
(sorry about the silly name)

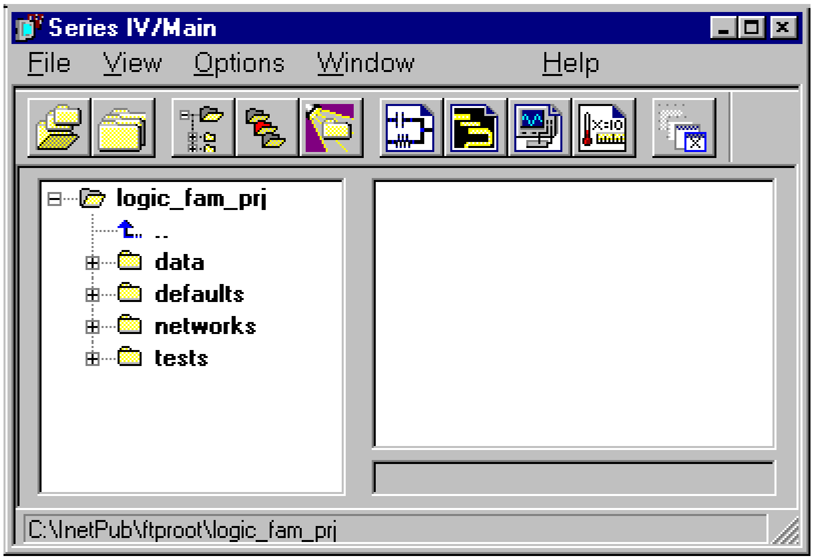
First
Download a copy of the directory
If using NT, be sure to put it in your HOME DIRECTORY, so you can access it from ALL ECI machines. We don't want to fill the NT machines with multiple duplicate copies of this.

Second
Start EESOF.
You should get a picture something like this



> File > open project …….open the project logic_fam_prj

The window will now look like this:



Numbering the row of icons from left to right,
button 6 opens a schematic design ("networks") window…this is for circuit designs
button 7 opens a mask layout window…don't need this presently
button 8 opens a test bench ("tests")window.

you place an icon representing your ckt within the test bench, and then run a simulation

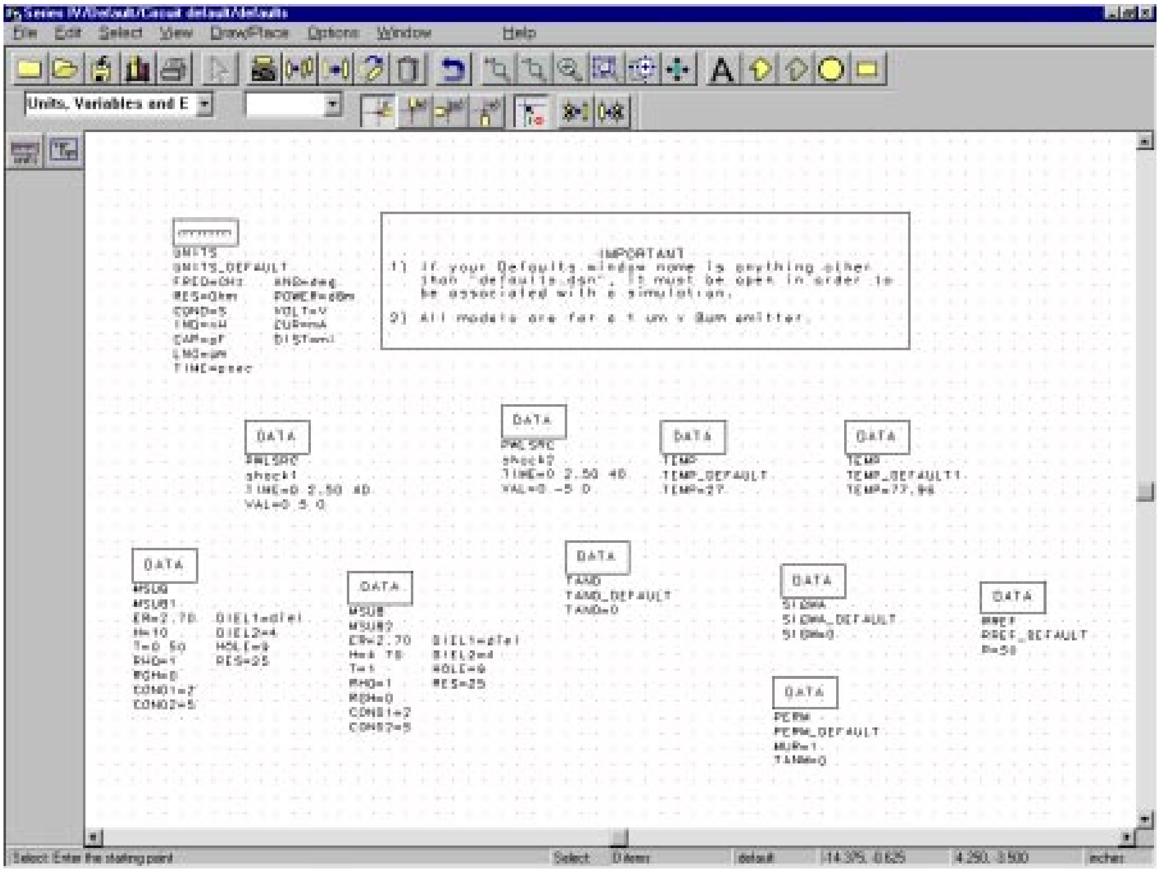
button 9 opens a "defaults" window

this holds standard transistor models, units definitions, etc

you can also access various networks, tests, etc, via the directory structure on the lower left

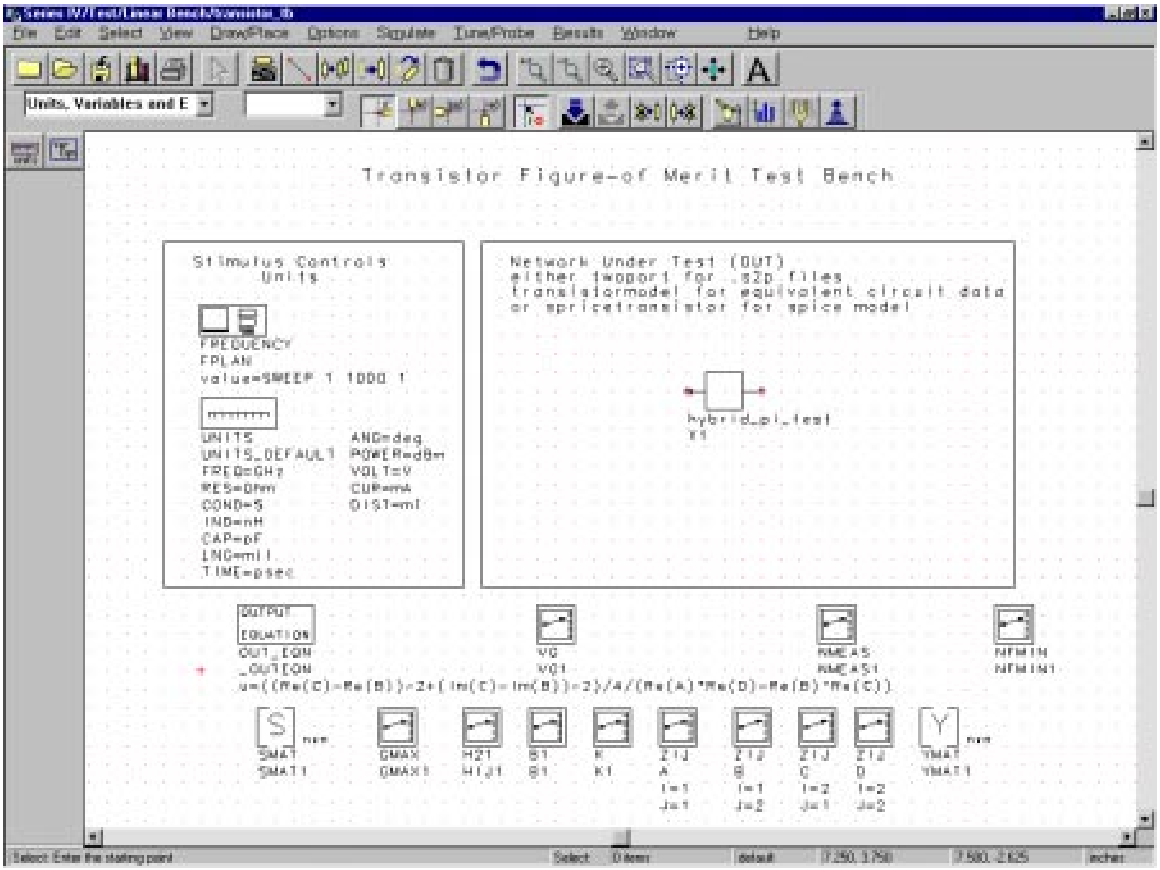
Third

Open the defaults window.

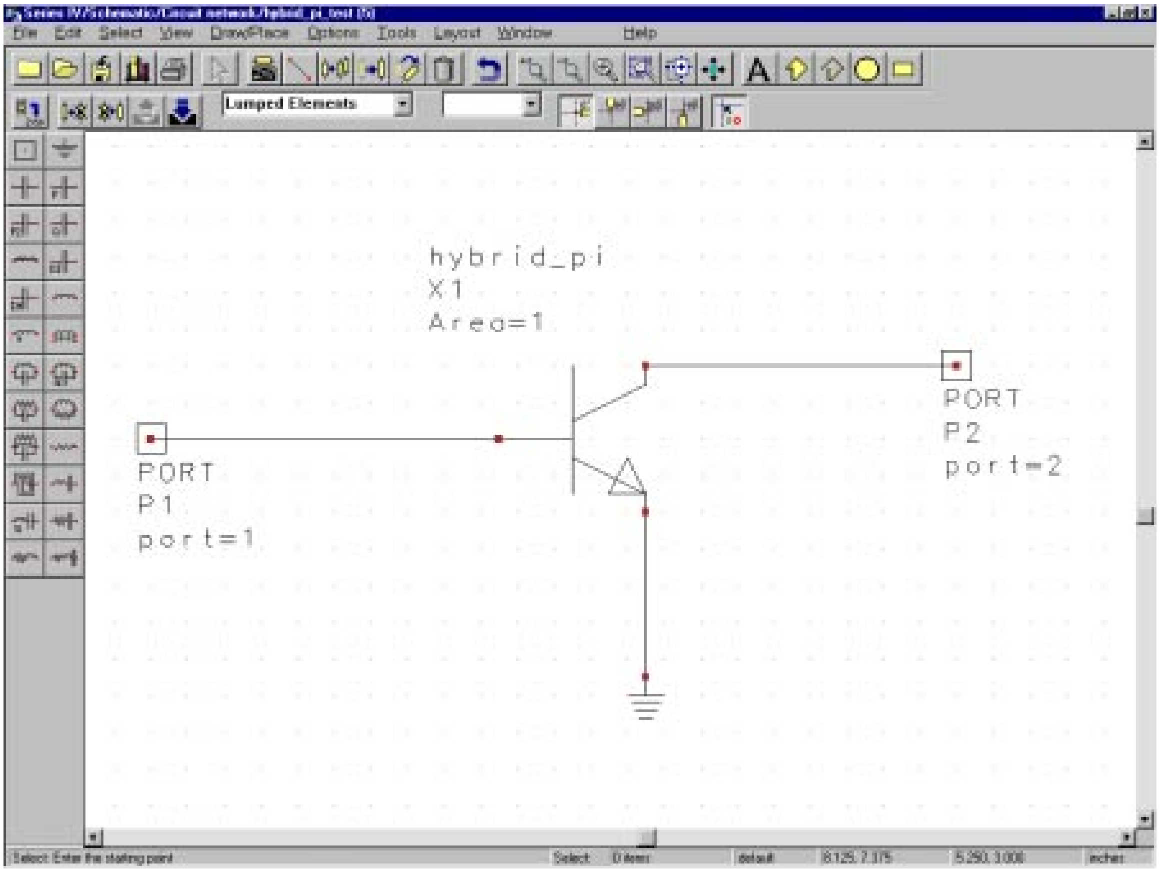


It will look something like this. The data files walled MSUB1 and MSUB 2 define microstrip substrate parameters. Units are defined here too. Click the window to close it.

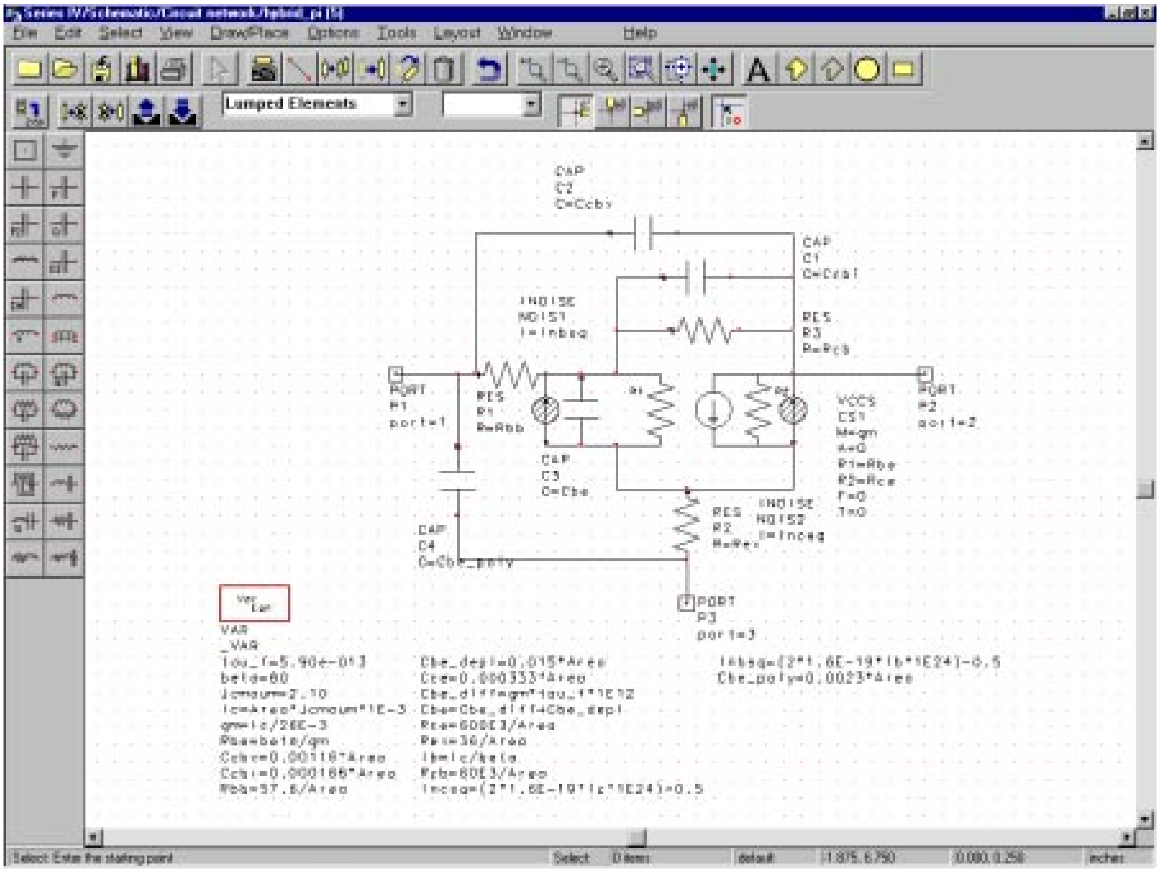
Fourth
Open up the "test" window, then open the test bench "transistor_tb.dsn
It looks like this:



Click on the Circuit under test "hybrid PI_test", then open up the circuit by clicking on the downward-pointing arrow ("push into") on the toolbar, and you will see this.



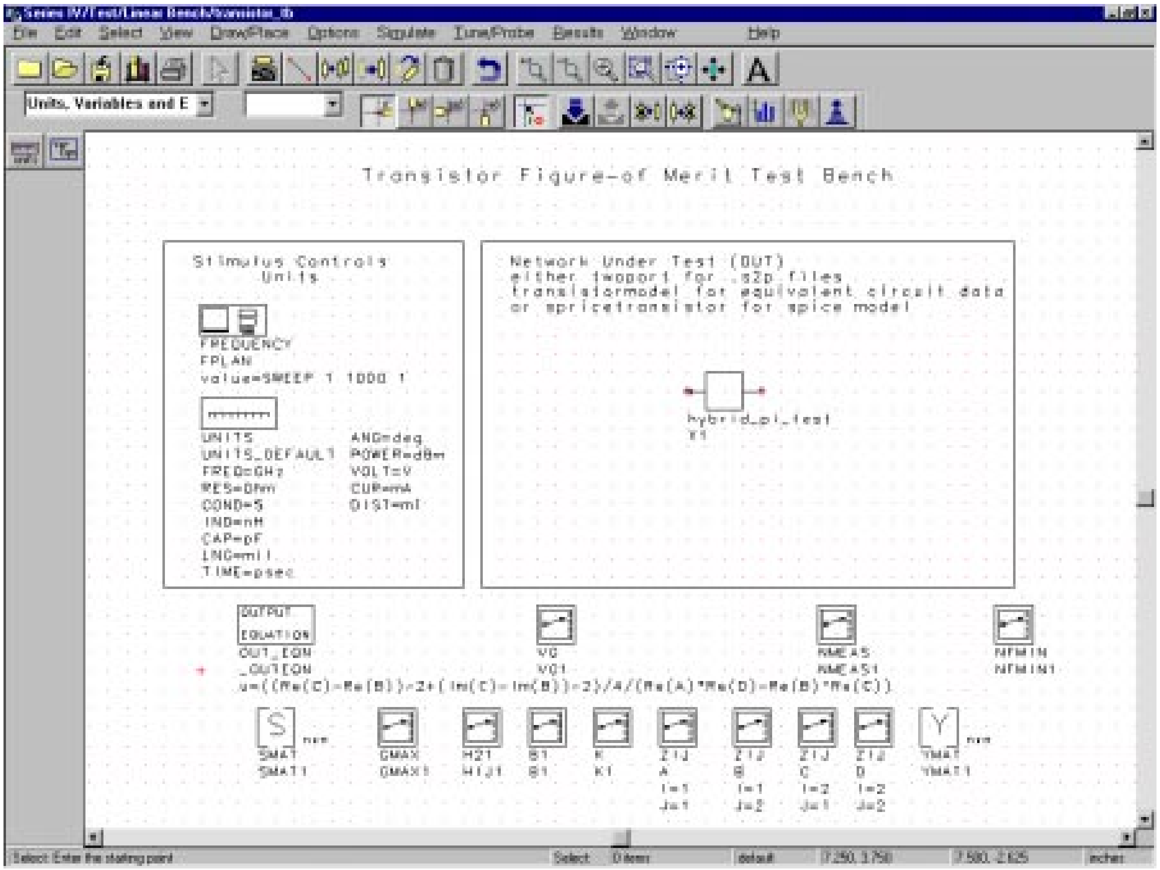
This is the circuit we are going to simulate: it is in fact built of a single subcircuit. Select the transistor "hybrid_pi", and push into it by clicking on the down arrow on the toolbar…



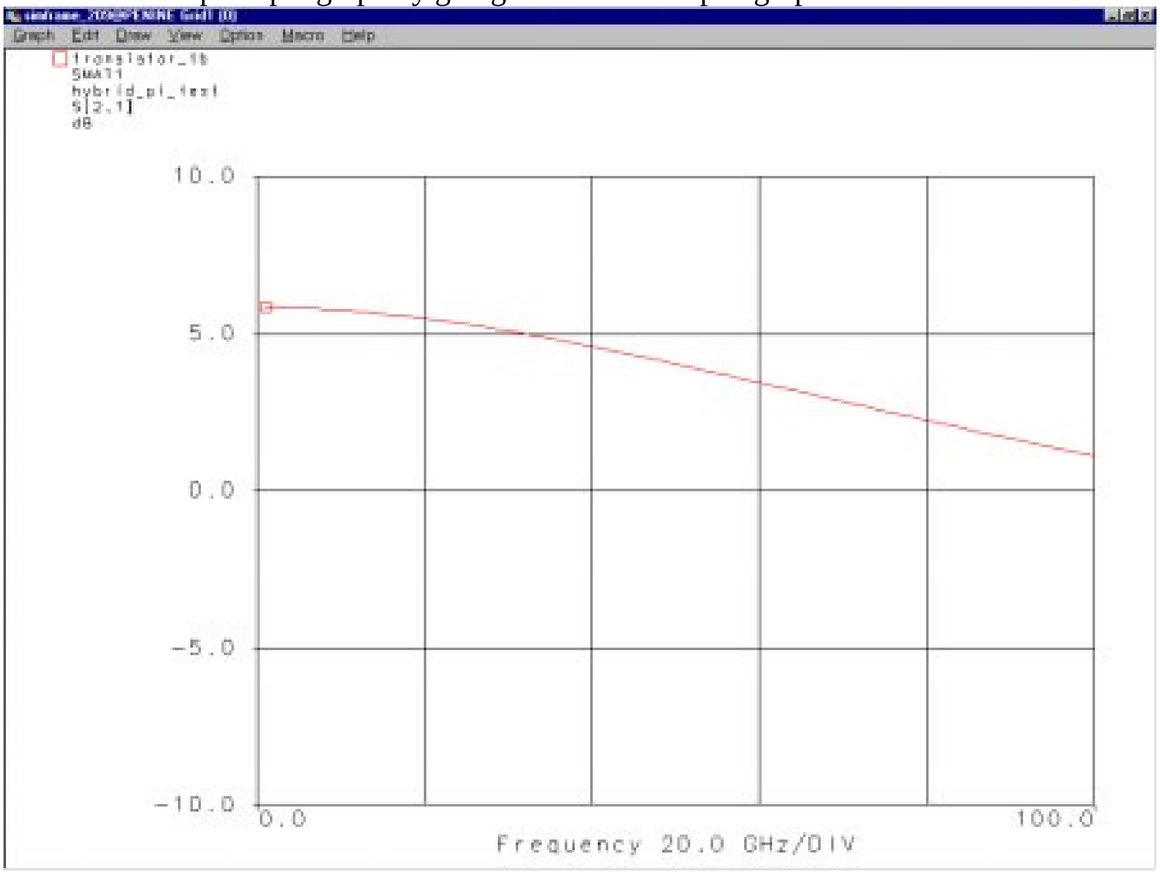
…and this is the network we will be simulating. It is a hybrid-pi (see class notes) description of a bipolar transistor.

You can move up and down in the hierarchy by pushing the up arrow and down arrow on the toolbar.

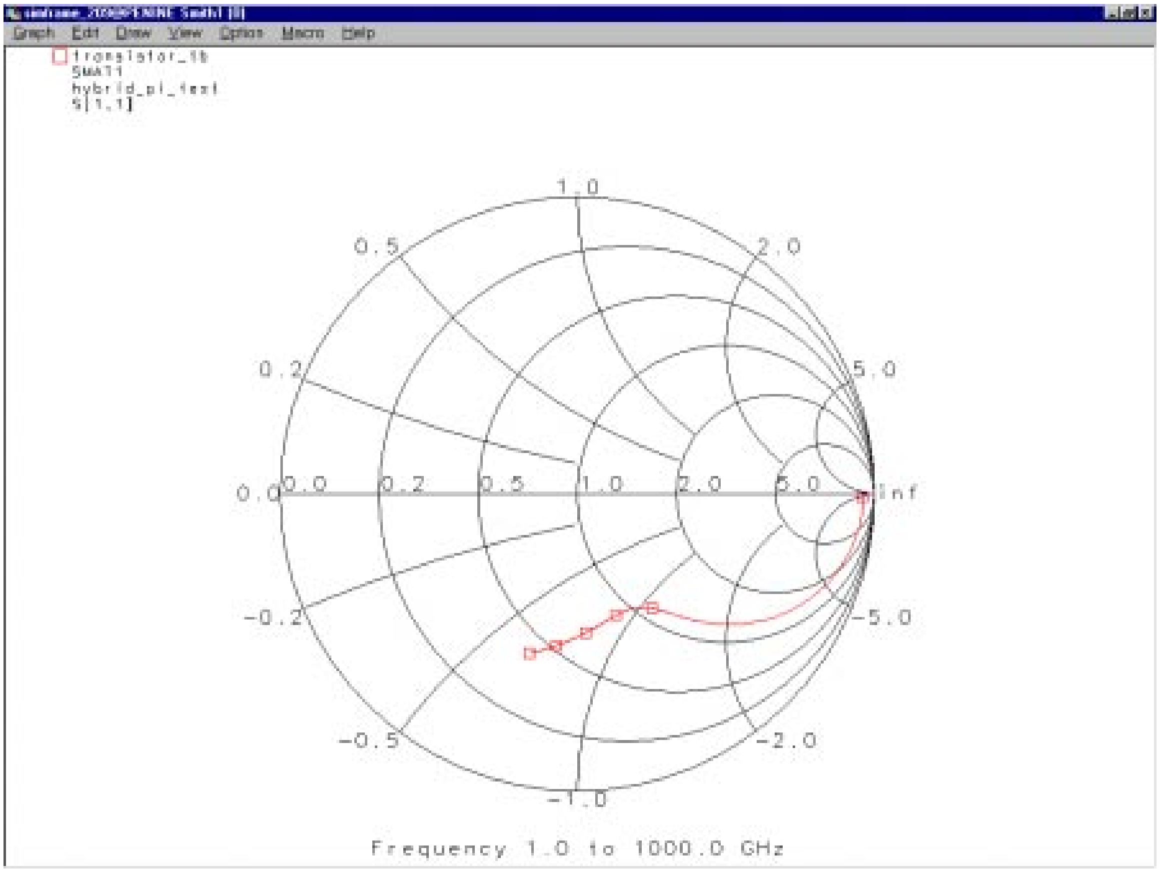
Go back to the test window, and simulate the circuit: > simulate> analyze



You can now open up a graph by going to Results > Open graph



Play with >Edit > Measurements and > Edit > sweep variables to change what is plotted and what the axes are. Play with >graph > new to work with different plot formats:

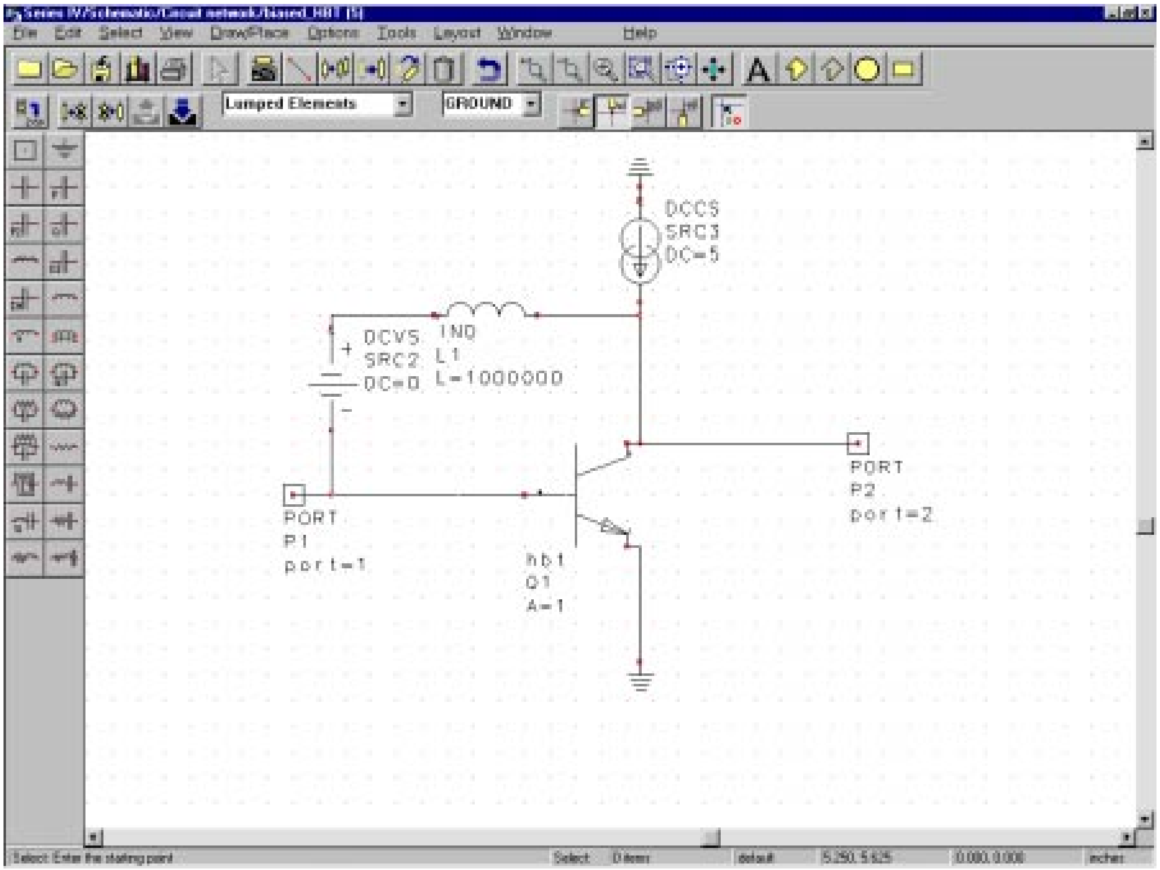


On the test bench, clicking on the "bookshelf (library)" icon brings up a bunch of things which can be placed in the test bench, including other measurements which can (after simulation) be accessed in the plot.

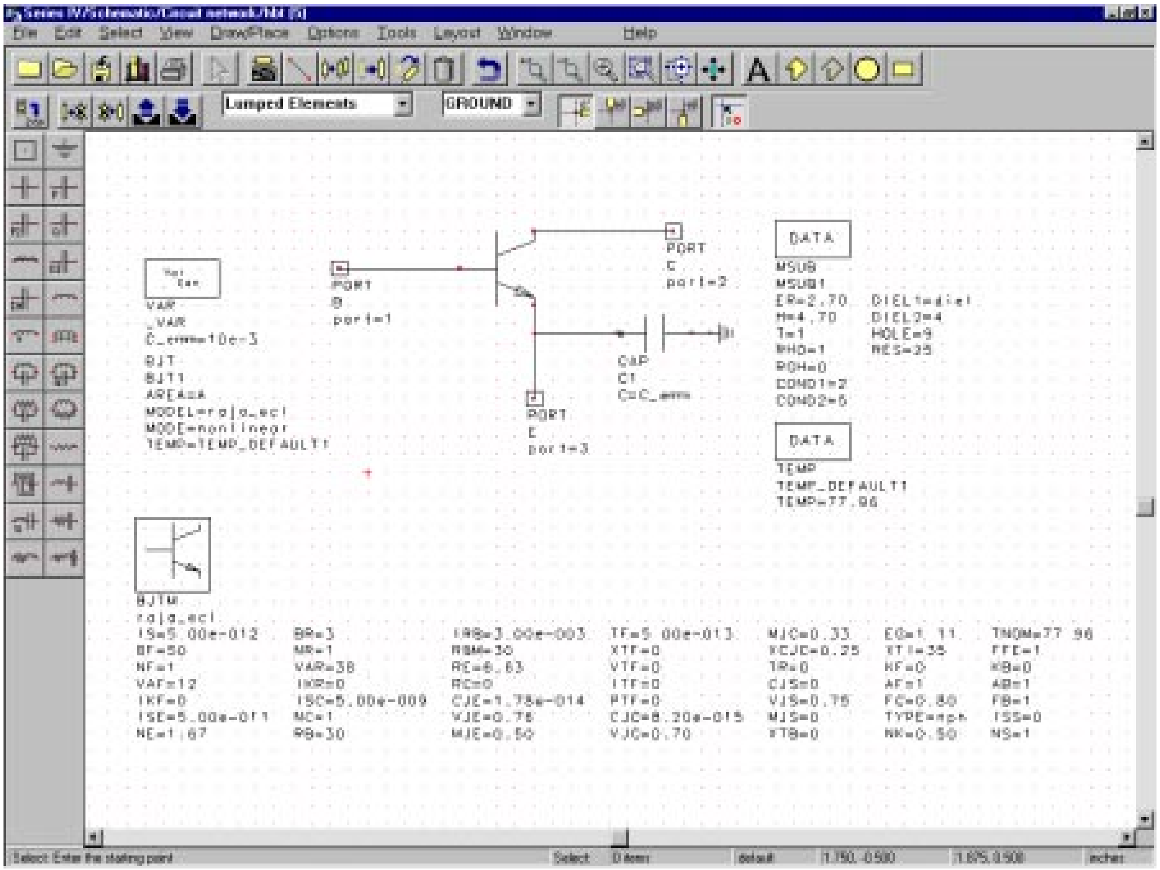
Part two

Open up the test bench "biased transistor test bench" (something like that)

The network under test will be "biased HBT"



Biased HBT looks like this, and if we push into the transistor symbol we see the following:



e.g., there is an underlying device model with a substrate capacitance C_emm. The data array below is the usual set of Gummel-Poon SPICE Model parameters.

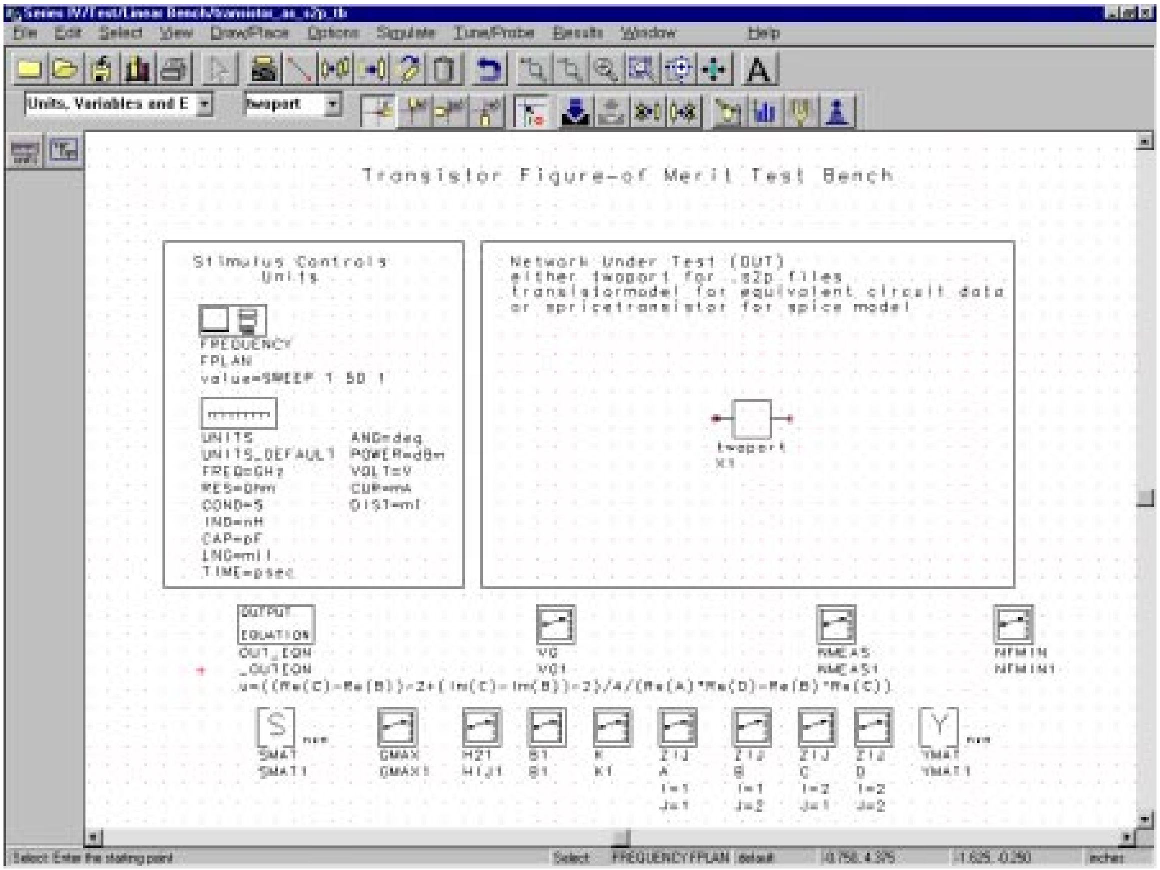
Simulate this circuit and plot the S-parameters.

This illustrates a **second way** we can define a transistor; as a Gummel-Poon (SPICE) model. This is a large-signal model, and demands that the device be biased as part of the simulation.

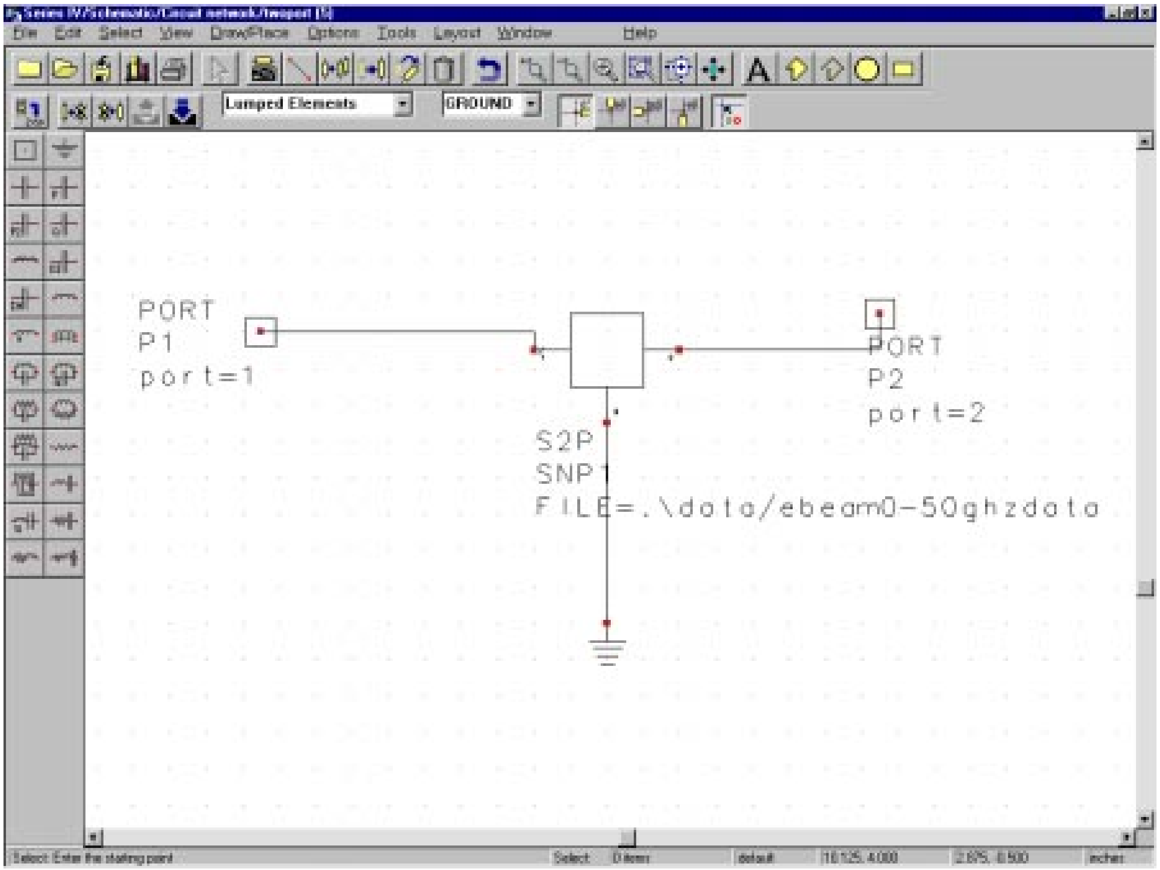
Please note: The way that the RAJA_ECL model has been defined, setting A=1 creates a device with physically 8 square microns junction area, which is best biased at currents between 1 and 8 mA. Much above 8 mA will break the device. Its breakdown is only 1.5 Volts, though the SPICE model does not reflect this.

Part Three

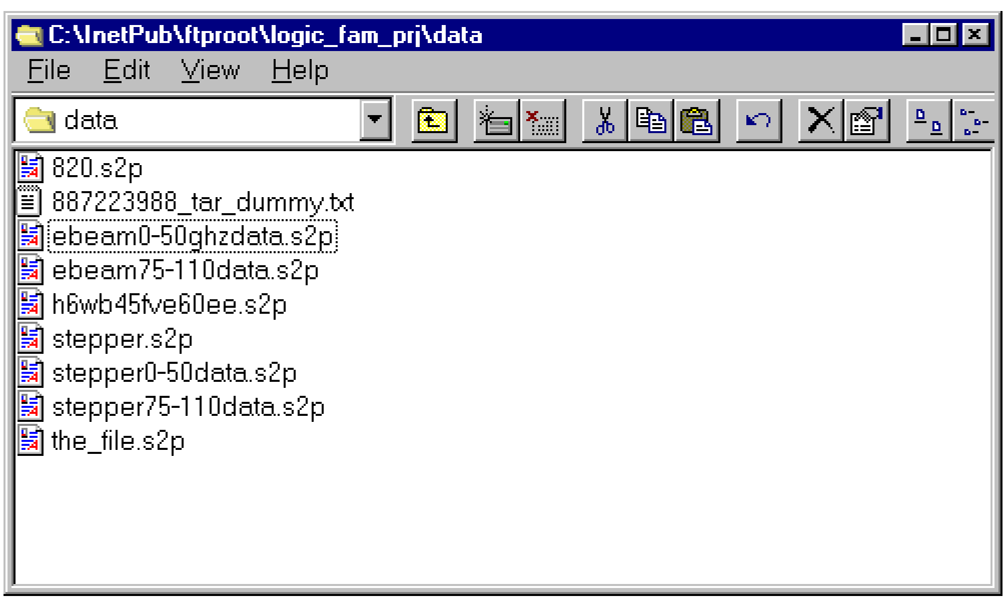
open up the test bench "transistor_as_s2p.



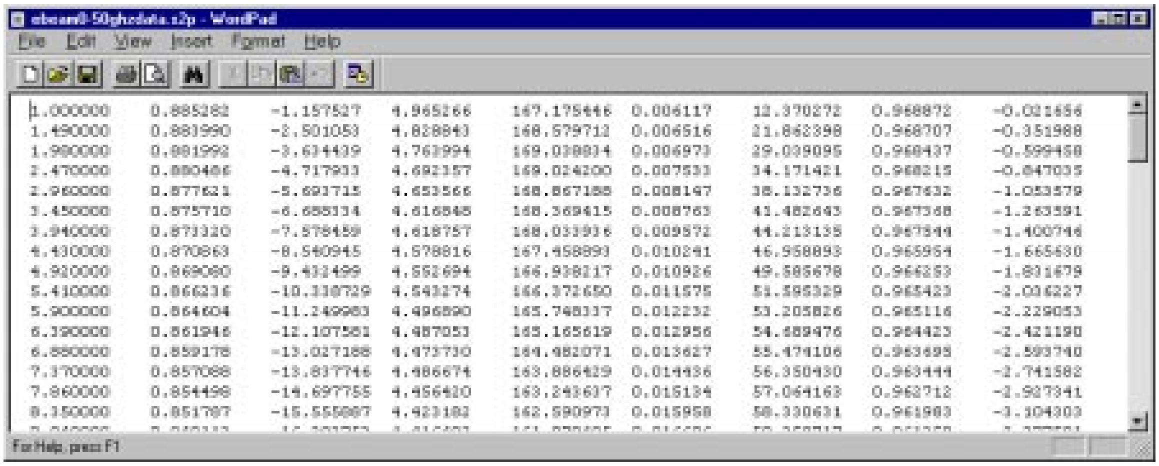
Pop into the "twoport": circuit to see:



This is invoking a data file placed in the /data directory within the project directory:



which is an tabular array of S--parameters vs. frequency, usually from a microwave network analyzer

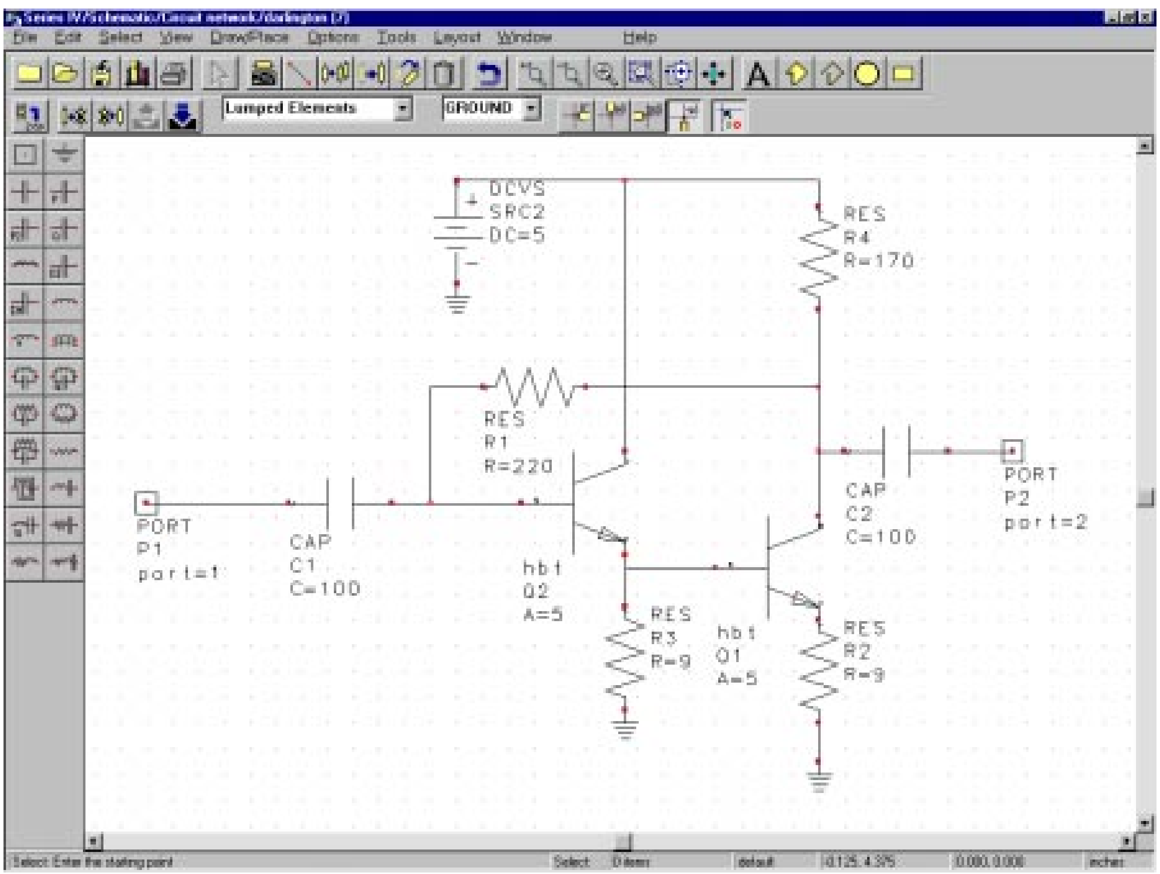


1.000000	0.885282	-1.157527	4.965266	167.175446	0.006117	12.370272	0.968872	-0.021656
1.490000	0.883990	-2.501053	4.828843	168.579712	0.006516	21.862398	0.968707	-0.351988
1.980000	0.881992	-3.634439	4.763994	169.038834	0.006973	29.039095	0.968437	-0.599458
2.470000	0.880406	-4.717933	4.692357	169.024200	0.007533	34.171421	0.968215	-0.847035
2.960000	0.877621	-5.693715	4.653566	168.867188	0.008147	38.132736	0.967632	-1.053579
3.450000	0.875710	-6.658134	4.616848	168.369415	0.008763	41.482643	0.967368	-1.263591
3.940000	0.873320	-7.578459	4.618757	168.033936	0.009572	44.213135	0.967544	-1.400746
4.430000	0.870863	-8.540945	4.578816	167.458893	0.010241	46.958893	0.965954	-1.665630
4.920000	0.869080	-9.432499	4.552694	166.938217	0.010926	49.585678	0.966253	-1.831679
5.410000	0.866236	-10.338729	4.543274	166.372650	0.011575	51.595329	0.965423	-2.036227
5.900000	0.864604	-11.249983	4.496890	165.748337	0.012232	53.205826	0.965116	-2.229053
6.390000	0.861946	-12.107581	4.487053	165.165619	0.012956	54.689476	0.964423	-2.421190
6.880000	0.859178	-13.027188	4.473730	164.482071	0.013627	55.474106	0.963695	-2.593740
7.370000	0.857088	-13.837746	4.486674	163.886429	0.014436	56.350430	0.963444	-2.741582
7.860000	0.854498	-14.697755	4.456420	163.243637	0.015134	57.064163	0.962712	-2.927341
8.350000	0.851787	-15.555087	4.423182	162.590973	0.015958	58.330631	0.961983	-3.104303

For this problem, sweep the frequency and plot the current gain H21 and the maximum available gain MAG and masons unilateral power gain U in dB vs. frequency.

Part 4:

Enter and simulate the problem circuit. Plot S-paramters vs frequency



ERROR: DANGER: Please change R3 to 40 Ohms