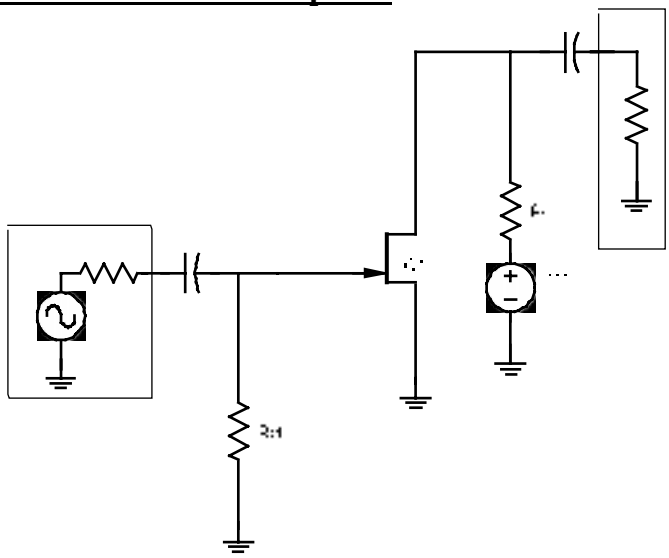
ECE202A Problem Set #2:

Device Modelling and Simple Broadband Circuits: Due Monday Nov. 1

1.FET common-source amplifier



In the circuit below, Rbb is 50 ohms, as is Rcc. Vcc is 7.5 volts. The generator and load resistances are 50 ohms. The FET Q1 has an Idss of 100 mA and a pinchoff voltage of -2 volts. Cgs=1 pF, Cgd=0.05 pF, Rg=10 ohms, Ri=0 ohms, Rds=200 ohms. Source resistance is 0 ohms. All other device parasitic parameters are negligible.

1.1

Calculate the circuit DC bias conditions, and find the drain current and the drain voltage.

1.2

Calculate element values for, and draw the device equivalent circuit. Calculate by hand approximate methods the magnitude and 3-dB bandwidth of S_{21} of the amplifier. Sketch the input reflection coefficient as a function of frequency on a Smith chart, indicating their values at 20 GHz

1.3

Enter the circuit on EESOF. Use a small signal equivalent circuit model for the transistor. Generate plots of the transistor S-parameters and G_{max} from DC-40 GHz (dB magnitude of all parameters, S_{21} & G_{max} on one graph, S_{12},S_{11},S_{22} on the other, plus smith charts of S_{11} and S_{22}). Use reasonable scales, and sufficient frequency points to adequately represent all frequency variations. Why is S_{12} not zero?

1.4

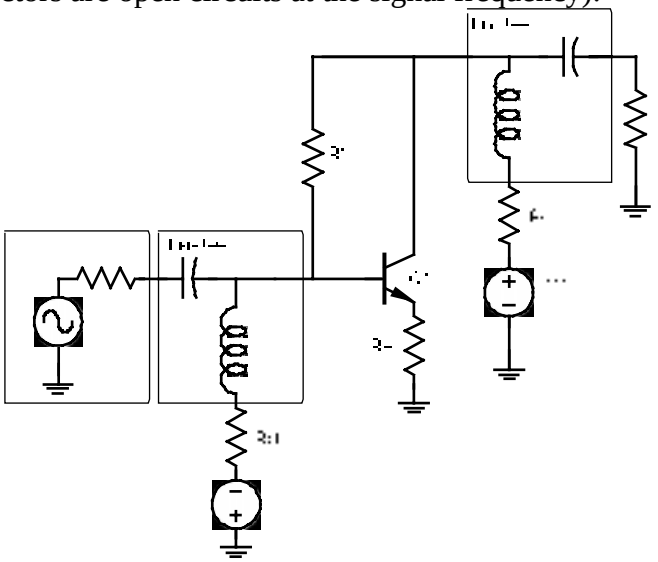
Then generate similar plots of the amplifier S-parameters, except don't bother plotting Gmax of the amplifier (it is not relevant here). Does hand analysis agree with theory?

1.5

Using the GMAX function, plot the maximum available power gain of the FET versus frequency and compare to your simulation of S_{21} of the amplifier. You should be getting flat gain over a broad frequency range, but are you using the available power gain of the transistor well?

2. BJT common-emitter feedback amplifier

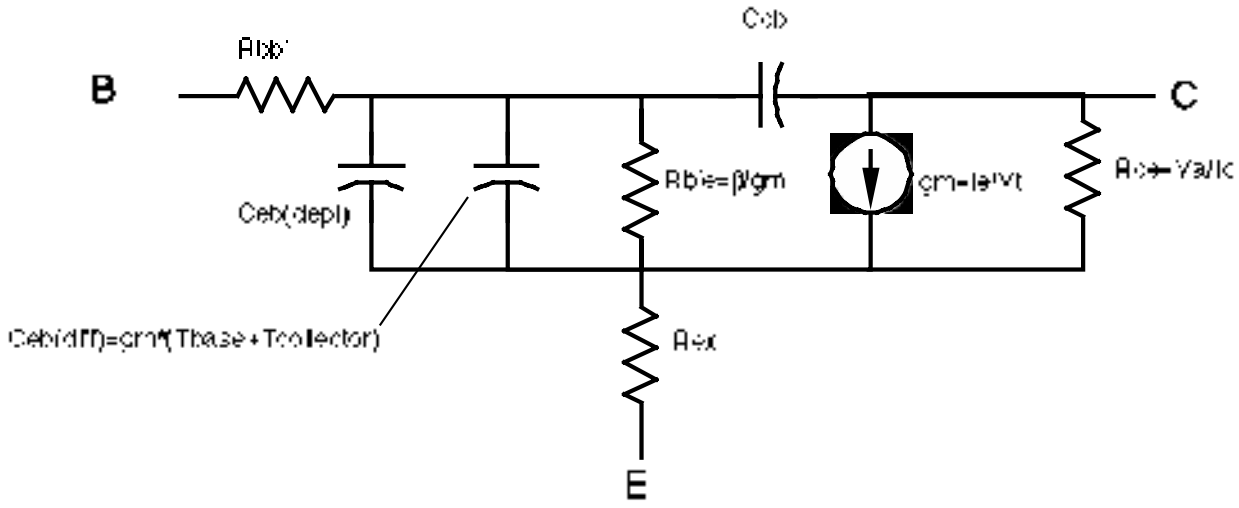
The circuit is shown below. Source impedance and load impedance are both 50 Ω, and indicated capacitors and inductors in the bias tees are "large" (i.e., the capacitors are short circuits and the inductors are open circuits at the signal frequency).



Element	Value
Re	5 Ω
Rf	208Ω
Vbb	-15 Volts
Vcc	+15 Volts
Rcc	1 kΩ
Rbb	3.33 kΩ

Transistor parameters: Use the following SPICE Model:

.MODEL INGAASHBT NPN IS=2 E-14 NF=1.0 BF=30 VAF=20 ISE=0 NE=1.17 ISC=2E-13 NC=1.0 VAR=10 RB=15.6 RC=1.6 RE=1.34 CJE=0FF VJE=0.6 MJE=0.27 FC=0.92 CJC=38FF VJC=0.07 MJC=0.1 XCJC=0.30 TF=1.5E-12



2.1

Calculate the circuit DC bias conditions, and find the emitter current and the collector voltage.

2.2

Calculate element values for the hybrid-pi model, and draw the device equivalent circuit. Calculate by hand the mid-frequency forward gain S_{21} of the amplifier and its 3 dB corner frequency. To make this hand calculation reasonable, neglect the base resistance and use the miller approximation.

2.3

Confirm your hand calculations by running EESOF from 1-20 GHz. First generate plots of the transistor dB(S_{21}) and dB(G_{max}). I would like you to both run simulations using your derived hybrid pi model, and the SPICE model

2.4

Then generate plots of the amplifier dB(S_{21}) and dB(S_{11},S_{22}, & S_{12}), and Smith Charts of S_{11} and S_{22}. Does your hand analysis agree reasonably well with simulation?

2.5

Make some observations. Does the amplifier perform as intended, as a gain stage with relatively constant gain over a wide frequency range? How does the amplifier S_{21} (in dB) compare to the transistor G_{max}? As the frequency increases, what happens to the device input and output impedances? (Look at the Smith Chart plots of S_{11} and S_{22}).