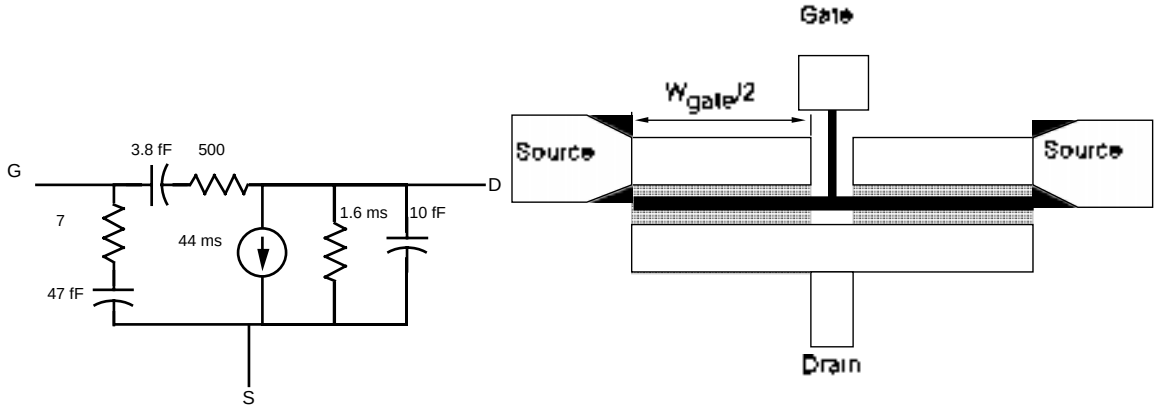
ECE202A Problem Set #4 due 11/22/99

Problem #1

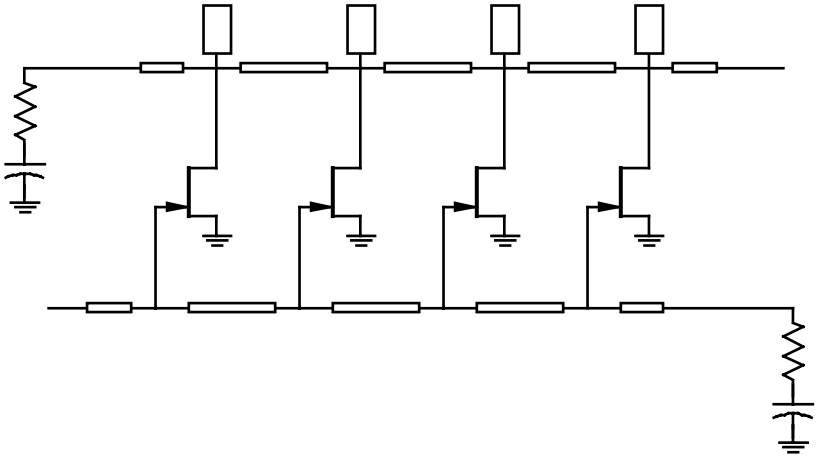
Background

You are designing a travelling-wave amplifier in a monolithic FET process. The FET has the equivalent circuit below, for a 50 µm wide device (comment: this is/was the model of a Hughes AlInAs/GaInAs/InP FET designed by Mishra, Ngyun, et. al.; later and more accurate modelling added some serious and highly detrimental parasitic inductances.)



Fet circuit elements scale in proportion to W_{gate} (if in units of admittance; things having units of impedance scale as $1/W_{gate}$). Neglect the gate-drain components (Cgd and the 500Ω resistor in series with it).

You are designing a travelling-wave amplifier for a bandwidth of about 100 GHz. Practical considerations of microstrip geometery limit you to on-wafer microstrip lines between 20Ω and 100Ω impedance. The dielectric of the transmission lines is InP which has a dielectric constant of 12.5. The substrate is 100 µm thick. Use the circuit diagram below:



Part 1

You will set the Bragg frequency of the synthetic gate and drain lines to 100 GHz, and their synthetic characteristic impedance is to be 50Ω. What gate width W_{gate} is then

required to attain this 100 GHz Bragg frequency? Draw the equivalent circuit of a FET of this width, giving all element values. Given that all series line sections are 100Ω and all shunt lines are 20Ω, find the required electrical lengths of all line sections in the above circuit diagram.

Part 2

Now examine the issue of frequency-dependent loss on the gate line. Using the distributed approximations discussed in class, how much attenuation is there as a function of frequency at each of the gates of the 4-FET TWA above? On the drain line, what is the attuation from the output of each FET to the TWA output?

Part 3

Trying to optimize the amplifier for 100 GHz operation: how many FETs should we use? We no longer have to use 4 fets. Setting the attenuation at the last FET to (Mark's somewhat arbitrary constraint) exp{-1/2} at the amplifier bandwidth, how many FETs should be used? What resulting attenuation do you predict on the drain line? What will be the low-frequency gain?

What is F_{max} of the FET? What is the transistor maximum available power gain vs frequency? How does this compare to the gain-frequency characteristics you predict for your amplifier?

Part 4

Now consider the issue of gate/drain phase matching: Due to the usual process variations, the FET gate length increases 33% from 0.15 μm to 0.2 μm, C_{gs} then increases by 33% and g_m decreases 33% (assume that other parameters remain relatively unchanged). Neglecting losses on gate and drain line for the moment, and using the number of FETs you have found above, how much gain rolloff would occur at 100 GHz relative to DC (give answer in dB) would occur from the resulting gate/drain phase mismatch? How about if we had the nominal FETs, but someone removed the drain shunt stubs?

Part 5

Sketch a layout for your amplifier, as a monolithic microwave IC, giving all dimensions. **You will find almost immediately that the 20Ω stubs are much too wide (approaching λ/4 @100 GHz)**. So, instead use Touchstone to find the dimensions of a microstrip radial stub having the capacitance you need. LINECALC should be used to find the required physical dimensions of your microstrip elements. Draw locations where the FET sources are connected to the wafer backside ground plane using via holes through the substrate. The vias are 25μm diameter circular holes. It is ok to use 90° microstrip bevelled bends .

Part 6

Simulate your final circuit design on Touchstone, and generate 2 plots: one of dB magnitude of S_{21}, and the other of dB magnitude of S_{11},S_{12}, and S_{22}. Simulate also otherwise identical TWAs, one having one more FET than your design, and the other having two more, just plotting S_{21}. Comment on the observed variations in gain and bandwidth.

Option:
I am also VERY interested in seeing how well a capacitive-division TWA would work with a really good HBT. If you are interested in doing this instead of the HEMT TWA design above, please come see me. As a similar comment, please feel free to consider capacitive division for the HEMT TWA listed above.