ECE 145B / 218B, notes set 10: Oscillators, Part 2.

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Two-Port Oscillator Theory

Why ?

Selection of oscillator topology seems ad - hoc.

Is there any reason to pick a particular topology?

Many standard oscillators will not oscillate at $f_{\max}$!

Is "maximum frequency of oscillation" an oxymoron ?

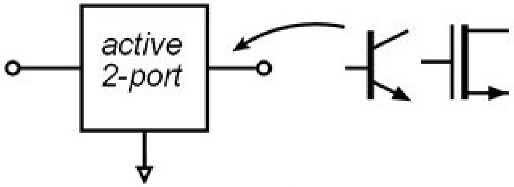
Or are we not desiging our oscillators well ?

Two - port theory will answer this.

Two-Port Oscillator Theory

Take an active 2-port (transistor, etc)

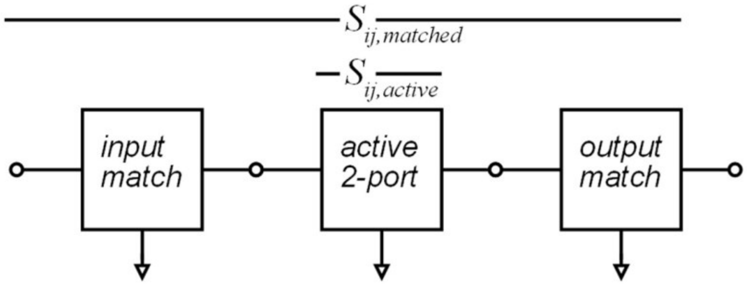
It has power gain for $0 < f < f_{\max}$.



Now impedance-match on input and output.

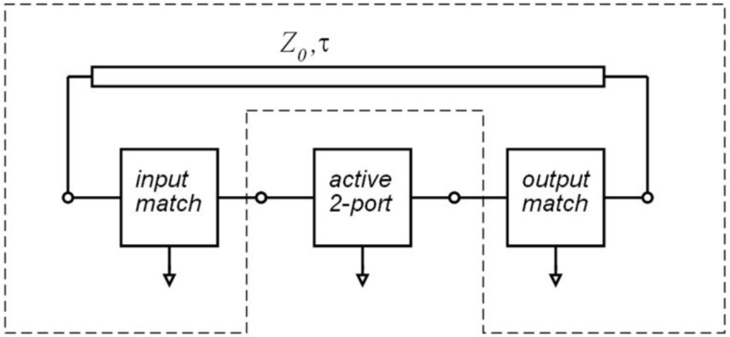
If $f < f_{\max}$, then $S_{11,matched} = S_{22,matched} = 0$ and

$S_{21,matched} = \| S_{21,matched} \| e^{j\phi}$ with $\| S_{21,matched} \| > 1$

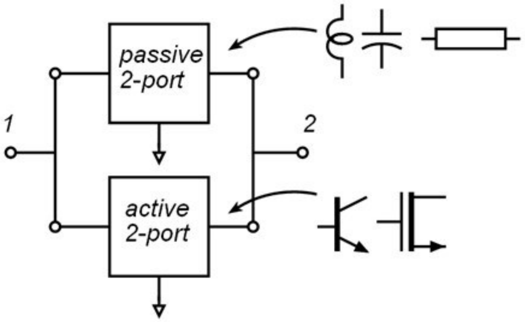


Add a transmission line of time delay τ hence phase shift $-j\omega\tau$, such that $\phi - j\omega\tau = n2\pi = n(360^o)$.

The feedback loop has loop transmisson $T = \| T \| e^{j\theta_T}$ with $\theta_T = 0$ and $\| T \| > 1$, hence the circuit will oscillate.



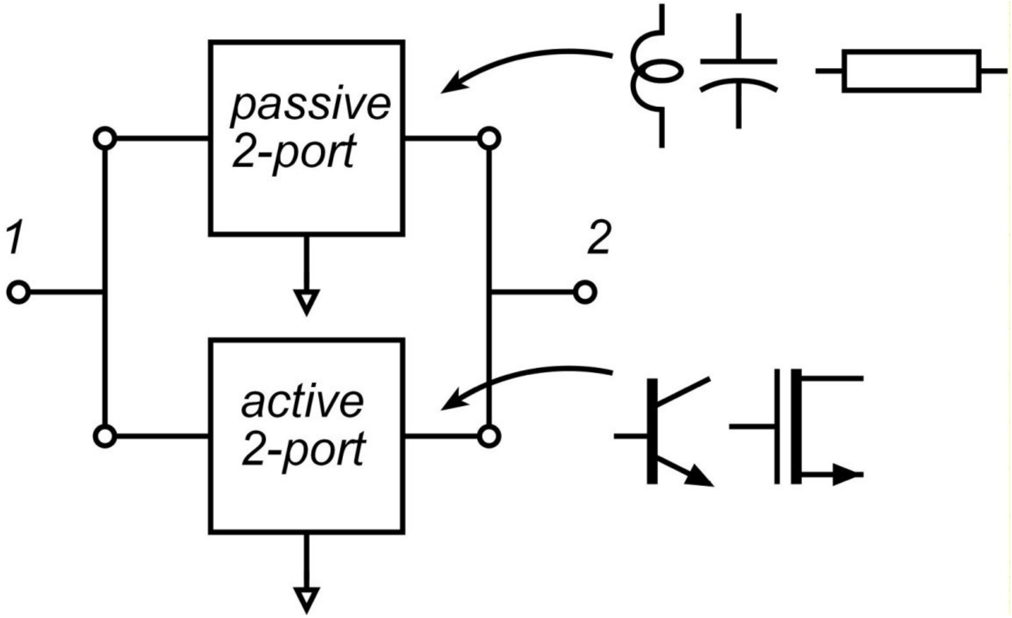
The combination of the 2 matching networks and the transmission-line is simply a 2-port network. Hence, for $f < f_{\max}$, a transistor will oscillate if connected to the appropriate 2-port network



Two-Port Oscillator Theory

Take an active 2 - port
(transistor, etc)

..and add feedback with
a passive 2 - port.



The passive 2 - port should clearly be lossless

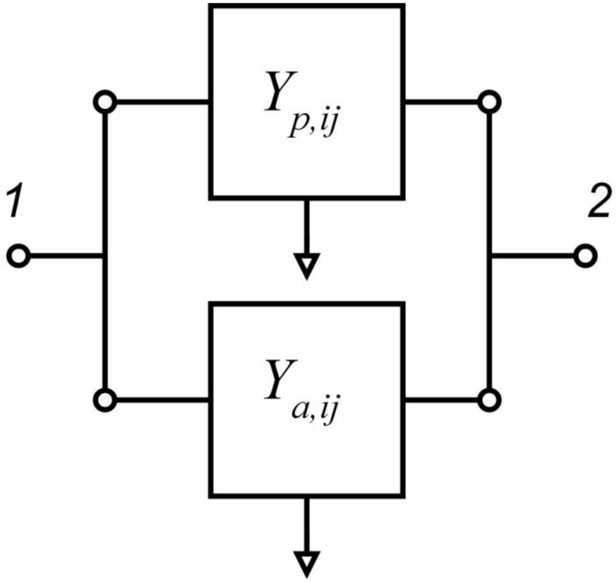
The feedback is completely general.

We are analyzing all possible 1 - transistor oscillators

Two-Port Oscillator Theory

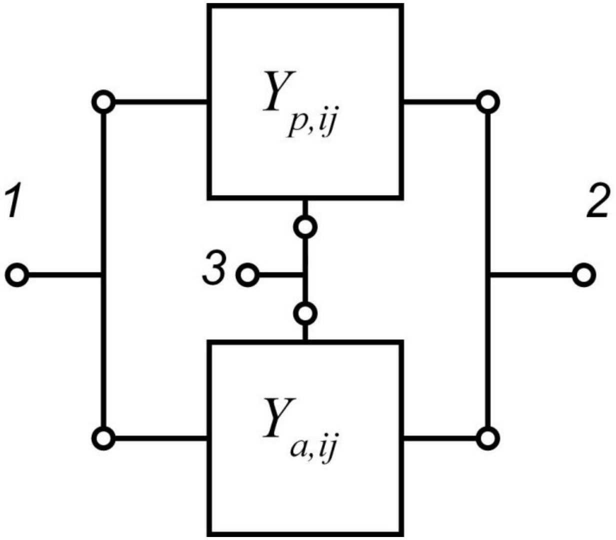
Passive network : $Y_{p,ij}$; this is reciprocal.

Active network : $Y_{a,ij}$; possibly not reciprocal



Note that the ground connection can be placed at nodes 1, 2, or 3.

This transforms oscillator from common - base to common - emitter, etc.



The feedback network

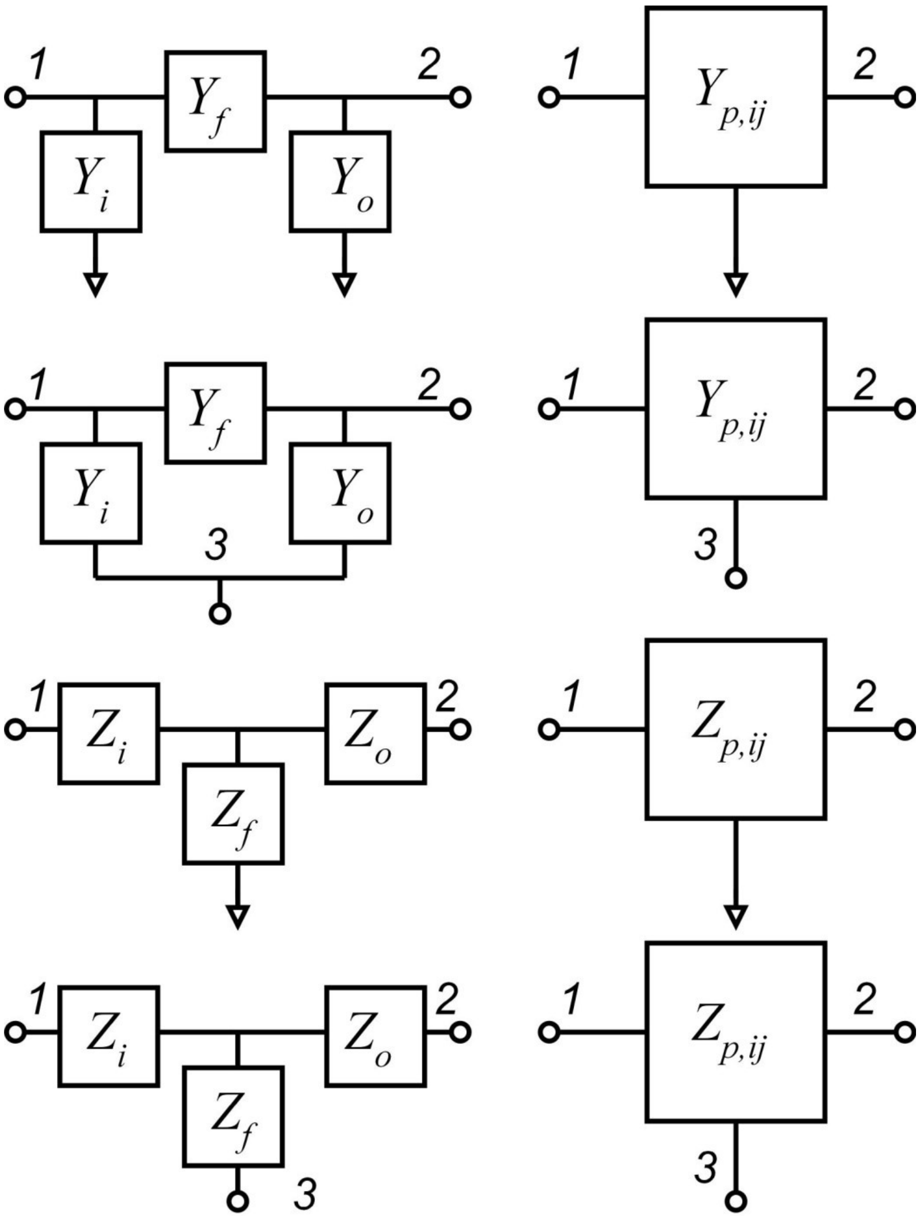
The feedback network can be represented by either $Y_{p,ij}$ or $Z_{p,ij}$.

It can be composed of either a T or a Pi network.

The Pi network is also known as a Delta network

More complex networks can be used, but are equivalent.

Note that the feedback impedances and admittances are purely imaginary.



The feedback network

$$\left[Y_{ij,p}\right]=\begin{bmatrix} Y_i+Y_f & -Y_f \\ -Y_f & Y_o+Y_f \end{bmatrix}$$

$$Y_f=-Y_{p,12}$$

$$Y_i=Y_{p,11}-Y_{p,12}$$

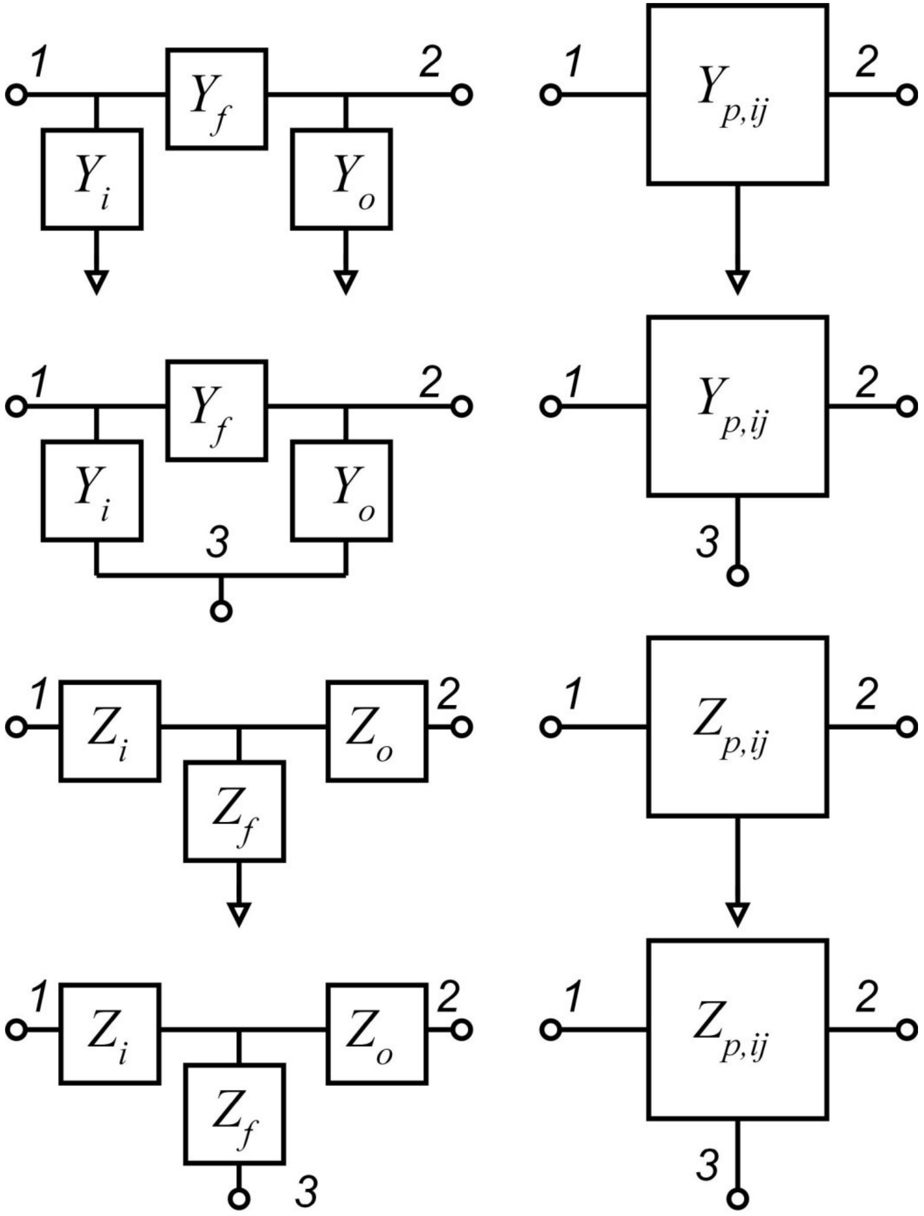
$$Y_o=Y_{p,22}-Y_{p,12}$$

$$\left[Z_{ij,p}\right]=\begin{bmatrix} Z_i+Z_f & -Z_f \\ -Z_f & Z_o+Z_f \end{bmatrix}$$

$$Z_f=-Z_{p,12}$$

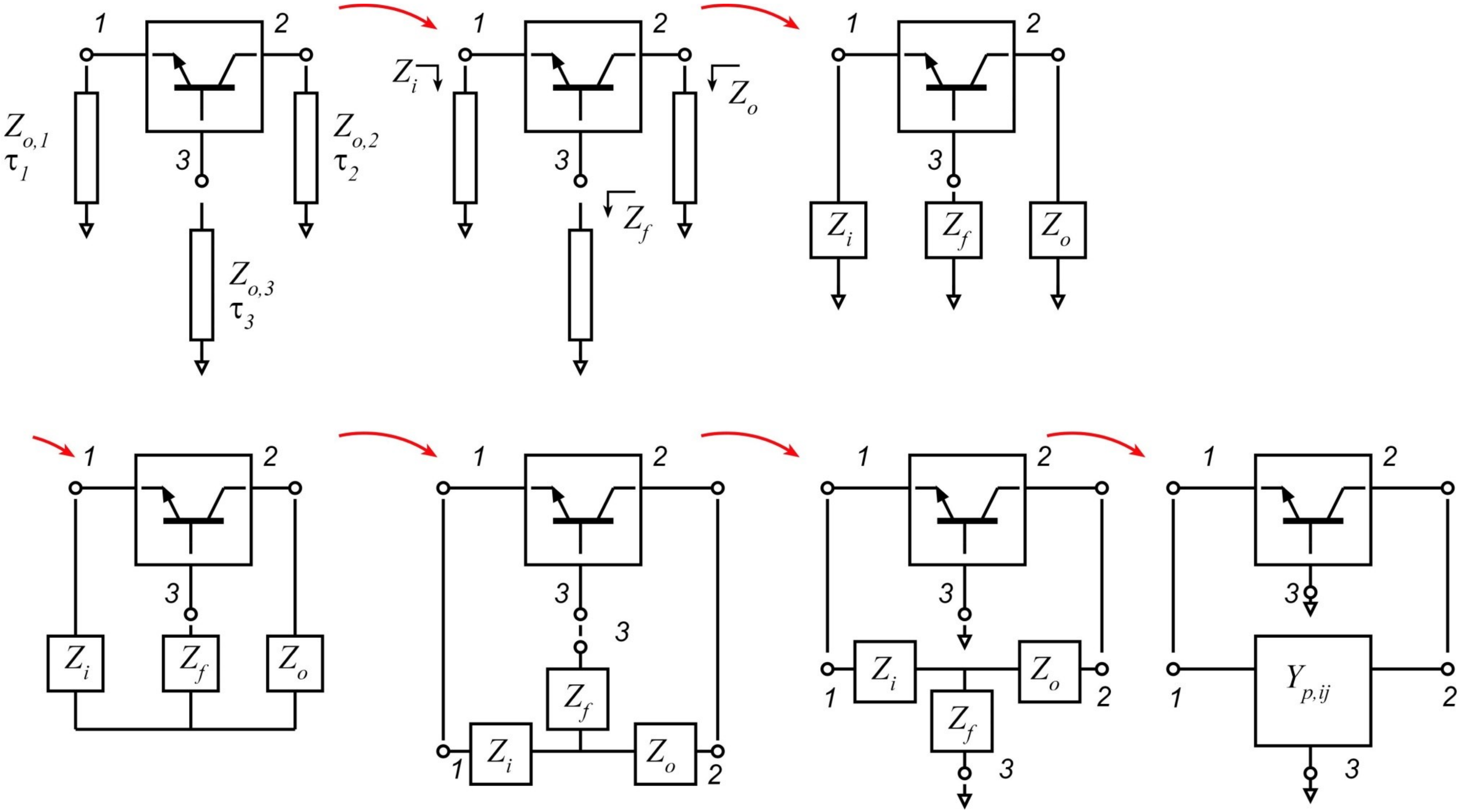
$$Z_i=Z_{p,11}-Z_{p,12}$$

$$Z_o=Z_{p,22}-Z_{p,12}$$

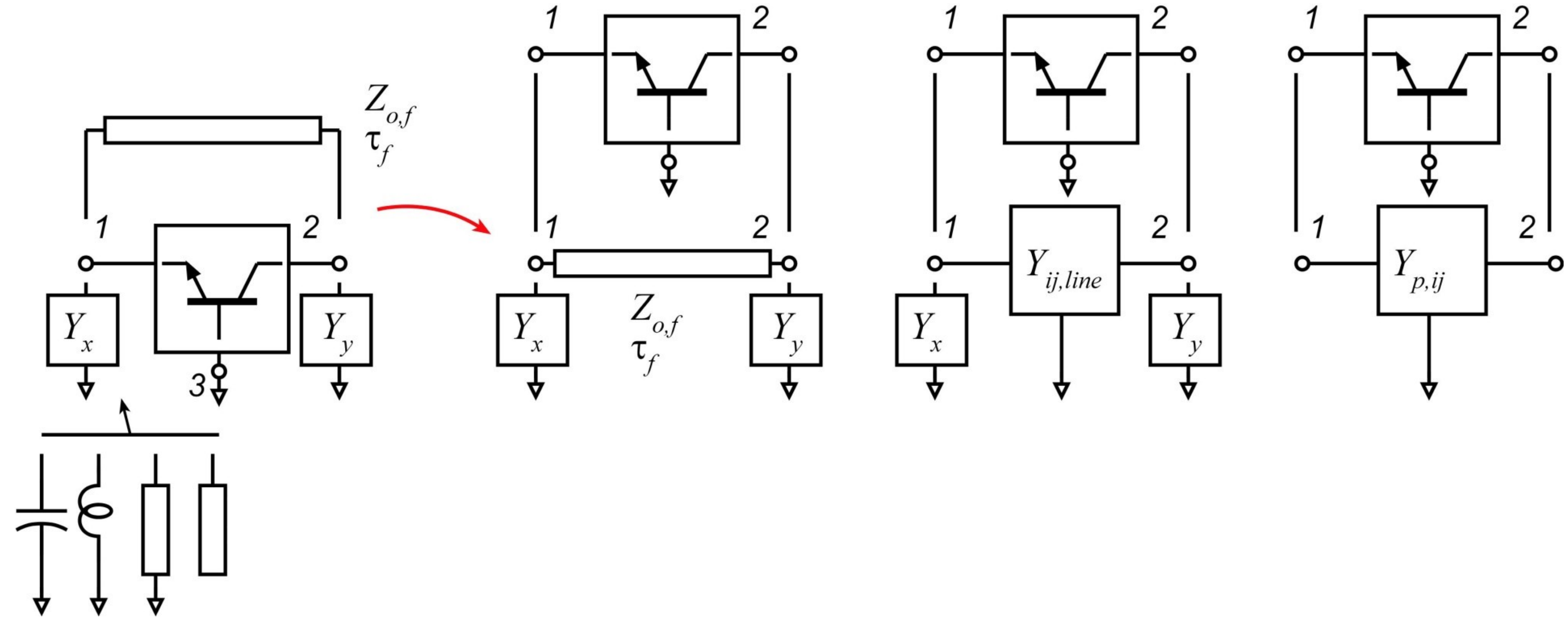


Note that the feedback impedances and admittances are purely imaginary.

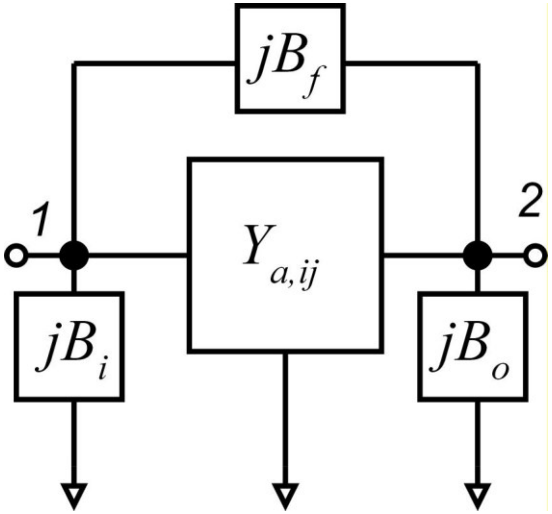
Series-Line-Tuned Oscillator



Shunt-Line-Tuned Oscillator



The Oscillator



Active device

$$[Y_{a,ij}]=\begin{bmatrix} G_{a,11}+jB_{a,11} & G_{a,12}+jB_{a,12} \\ G_{a,21}+jB_{a,21} & G_{a,22}+jB_{a,22} \end{bmatrix}$$

Oscillator

$$[Y_{osc,ij}]=\begin{bmatrix} G_{a,11}+jB_{a,11}+jB_i+jB_f & G_{a,12}+jB_{a,12}-jB_f \\ G_{a,21}+jB_{a,21}-jB_f & G_{a,22}+jB_{a,22}+jB_o+jB_f \end{bmatrix}=\begin{bmatrix} Y_{osc,11} & Y_{osc,12} \\ Y_{osc,21} & Y_{osc,22} \end{bmatrix}$$

Simplify : write this as

$$[Y_{osc,ij}]=\begin{bmatrix} G_{a,11}+jB_{11} & G_{a,12}+jB_{a,12}-jB_f \\ G_{a,21}+jB_{a,21}-jB_f & G_{a,22}+jB_{22} \end{bmatrix}$$

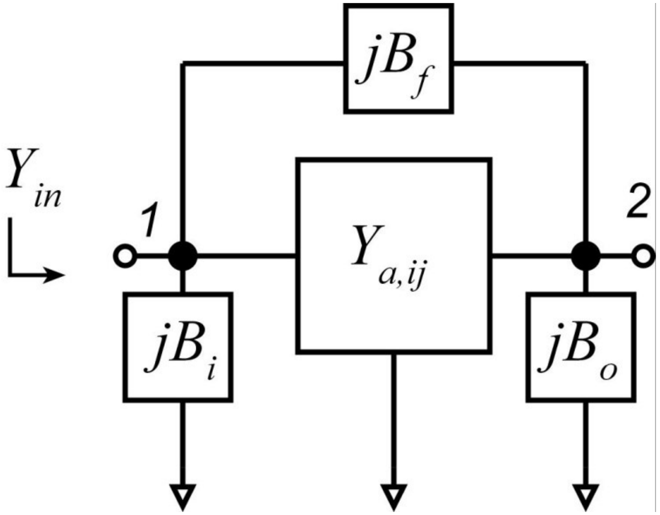
By adjusting the feedback network, we can set B_{11} , B_{22} , and B_f to any value we desire.

Oscillator Input Admittance

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{osc,11} & Y_{osc,12} \\ Y_{osc,21} & Y_{osc,22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$I_2 = 0 \rightarrow V_2 = -(Y_{osc,21} / Y_{osc,22}) V_1$$

$$\rightarrow Y_{in} = Y_{osc,11} - (Y_{osc,12} Y_{osc,21} / Y_{osc,22})$$



$$\left[Y_{osc,ij}\right] = \left[Y_{osc,ij}\right] = \begin{bmatrix} G_{a,11} + jB_{11} & G_{a,12} + jB_{a,12} - jB_f \\ G_{a,21} + jB_{a,21} - jB_f & G_{a,22} + jB_{22} \end{bmatrix}$$

$$Y_{in} = G_{a,11} + jB_{11} - \frac{\left(G_{a,12} + jB_{a,12} - jB_f\right)\left(G_{a,21} + jB_{a,21} - jB_f\right)}{\left(G_{a,22} + jB_{22}\right)} = G_{in} + jB_{in}$$

We want $B_{in} = 0$, and to make G_{in} as negative as possible.

Input Conductance

$$
\begin{aligned}
Y_{in} &= G_{a,11} + jB_{11} - \frac{\left(G_{a,12} + j(B_{a,12} - B_f)\right)\left(G_{a,21} + j(B_{a,21} - B_f)\right)}{\left(G_{a,22} + jB_{22}\right)} \\
Y_{in} &= G_{a,11} + jB_{11} - \frac{\left(\left(G_{a,12}G_{a,21} - (B_{a,12} - B_f)(B_{a,21} - B_f)\right) + j\left(G_{a,21}(B_{a,12} - B_f) + G_{a,12}(B_{a,21} - B_f)\right)\right)\left(G_{a,22} - jB_{22}\right)}{\left(G_{a,22}^2 + B_{22}^2\right)} \\
G_{in} &= G_{a,11} - \frac{\left(G_{a,12}G_{a,21} - (B_{a,12} - B_f)(B_{a,21} - B_f)\right)G_{a,22} + \left(G_{a,21}(B_{a,12} - B_f) + G_{a,12}(B_{a,21} - B_f)\right)B_{22}}{\left(G_{a,22}^2 + B_{22}^2\right)} \\
B_{in} &= B_{11} + \frac{\left(G_{a,21}(B_{a,12} - B_f) + G_{a,12}(B_{a,21} - B_f)\right)G_{a,22} - \left(G_{a,12}G_{a,21} - (B_{a,12} - B_f)(B_{a,21} - B_f)\right)B_{22}}{\left(G_{a,22}^2 + B_{22}^2\right)}
\end{aligned}
$$

$$
\begin{aligned}
G_{in} = G_{a,11} &- \frac{\left(G_{a,12}G_{a,21} - (B_{a,12} - B_f)(B_{a,21} - B_f)\right)G_{a,22}}{\left(G_{a,22}^2 + B_{22}^2\right)} \\
&- \frac{\left(G_{a,21}(B_{a,12} - B_f) + G_{a,12}(B_{a,21} - B_f)\right)B_{22}}{\left(G_{a,22}^2 + B_{22}^2\right)}
\end{aligned}
$$

We should pick B_f and B_{22} and to obtain a large negative G_{in}.

Unfortunately, I've been unable to derive these*.

B_f and B_{22} can also be tuned manually to maximize the negative input conductance.

This is shown on the next slides.

* Optimum feedback elements given in

D.F. Page, A. R. Boothroyd, "Instability in Two-Port Active Networks"

IRE Transactions on Circuit Theory, Vol. CT-5, pp. 133-139, June 1958.

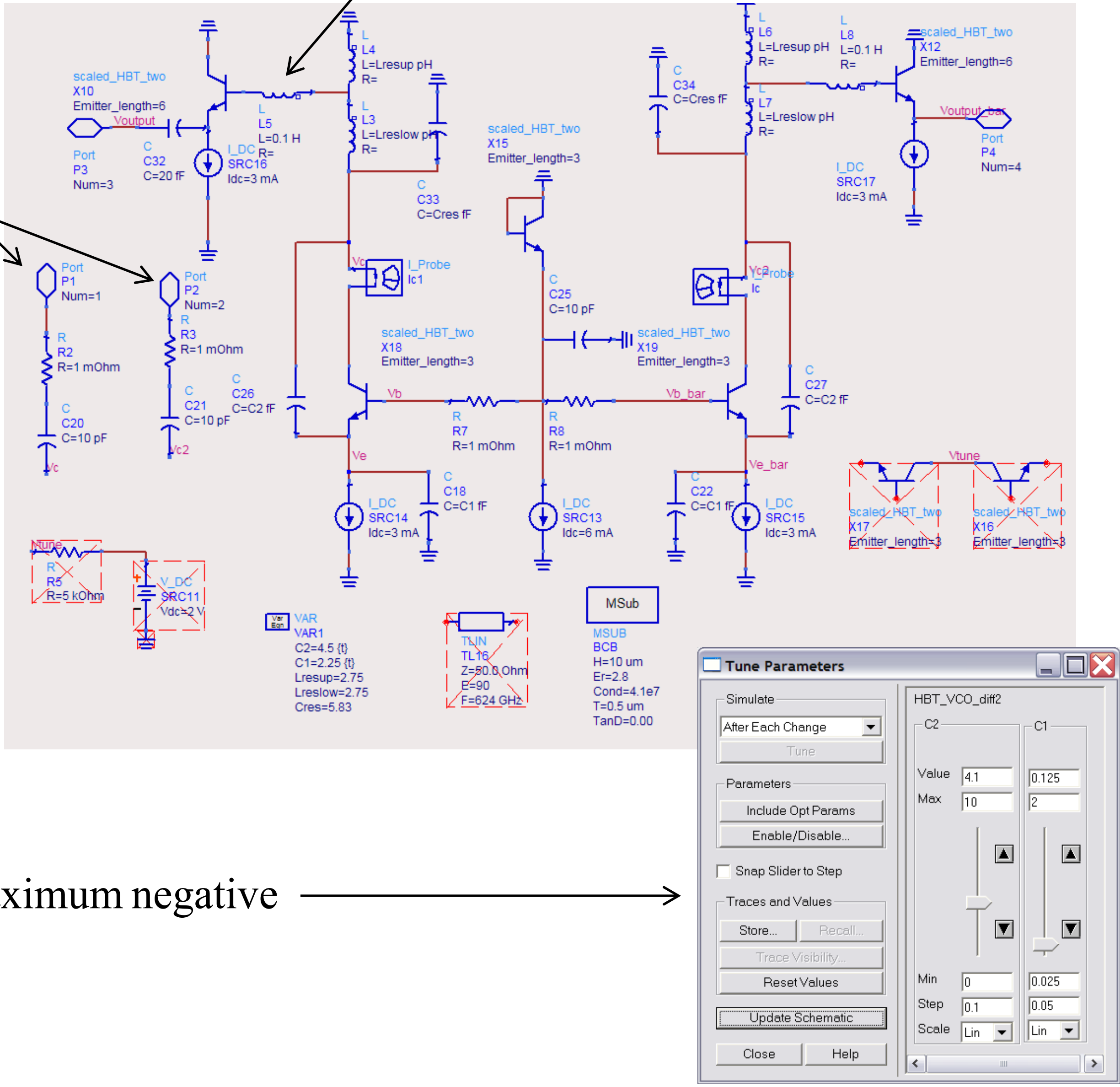
Design Example (1): Topology, Negative G Tuning.

620 GHz Common - Base Colpitts

with ~ 800 GHz $f_{\max}$ HBT

initially set large to disconnect buffer, removing its loading.

Test port connected to transistor collectors



Simulate: After Each Change

☐ Snap Slider to Step

HBT_VCO_diff2

	C2	C1
Value	4.1	0.125
Max	10	2
Min	0	0.025
Step	0.1	0.05
Scale	Lin	Lin

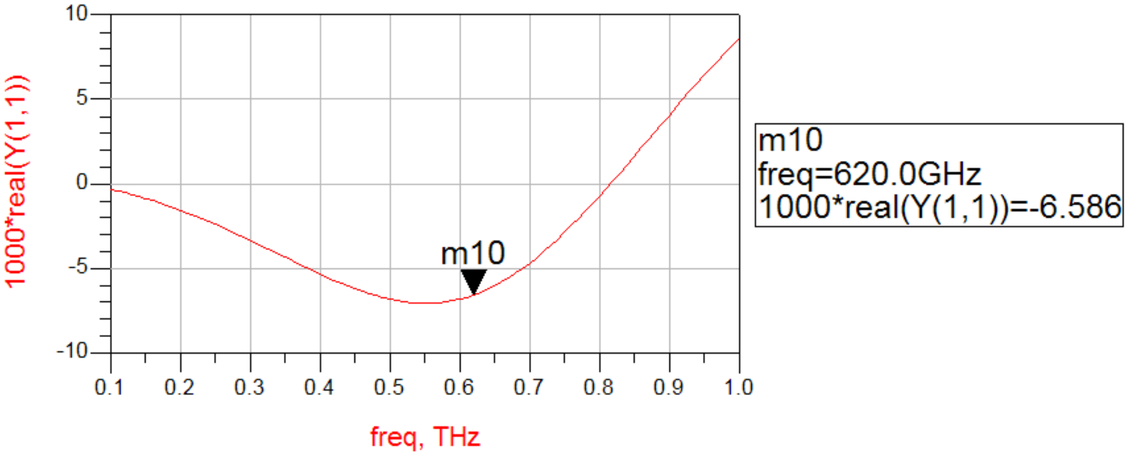
C_1 and C_2 are tuned to produce maximum negative conductance at the collectors :

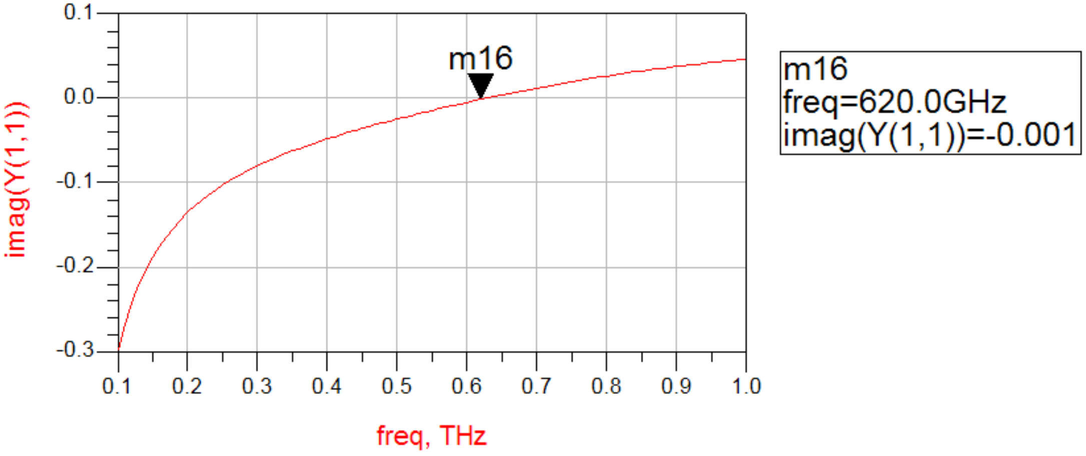
Design Example (2): Resonator Admittance

Port admittance observed at the collectors.

C_1 and C_2 have been tuned for maximum negative G_{11}.

The resonator inductance has been tuned for zero B_{11}.

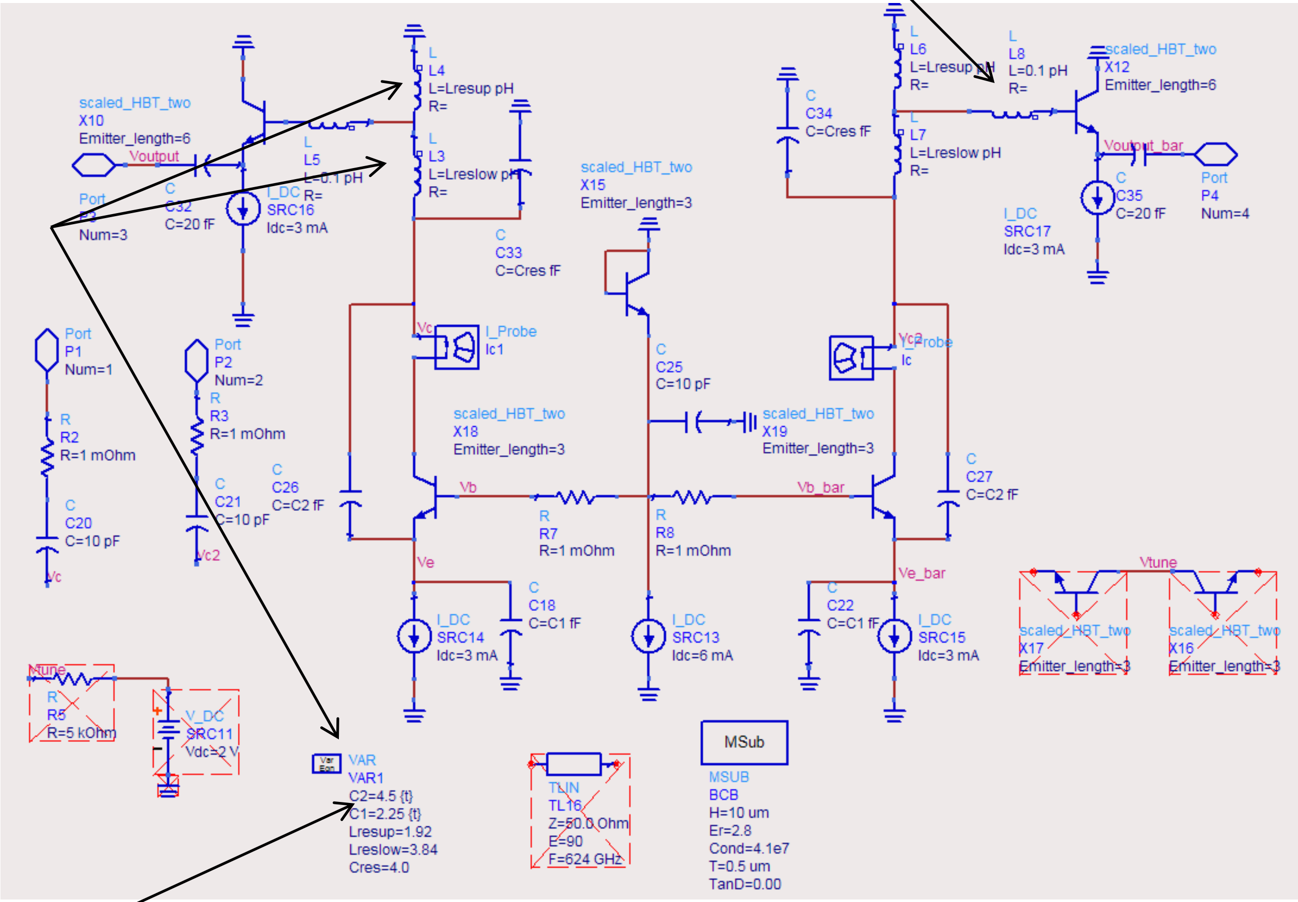




Design Example (3): Connection of Buffer

L is now small; buffer is connected.

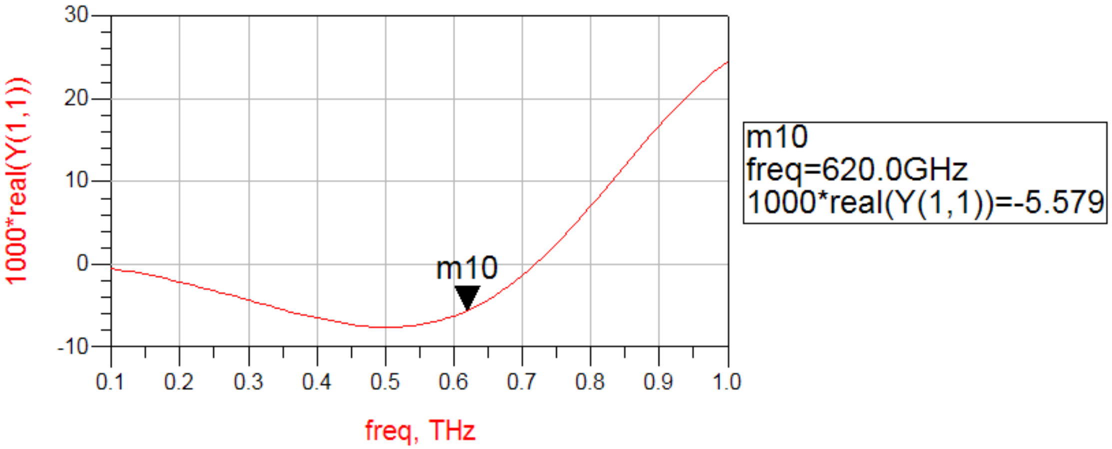
3 : 1 inductor step - down ratio reduces loading of buffer on oscillator core.



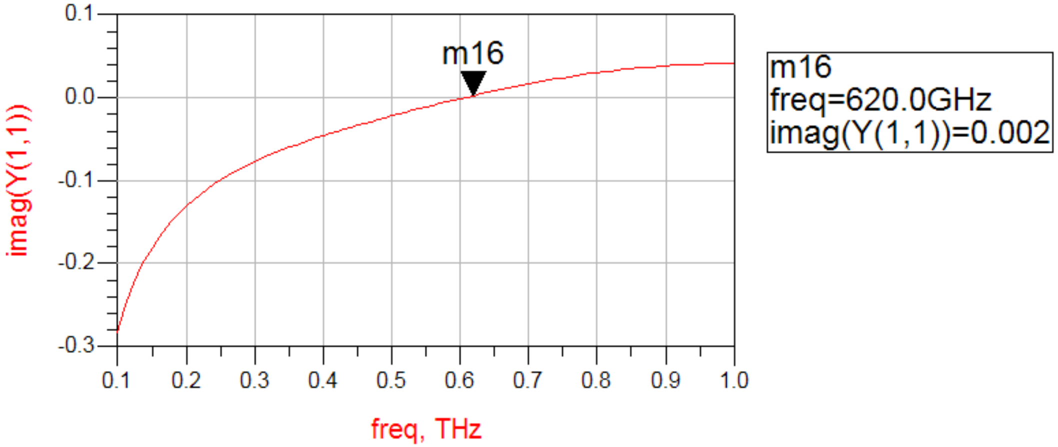
The feedback elements must be re - tuned

Design Example (4): Negative G given Buffer

Note that the negative conductance has been somewhat suppressed by the output loading.



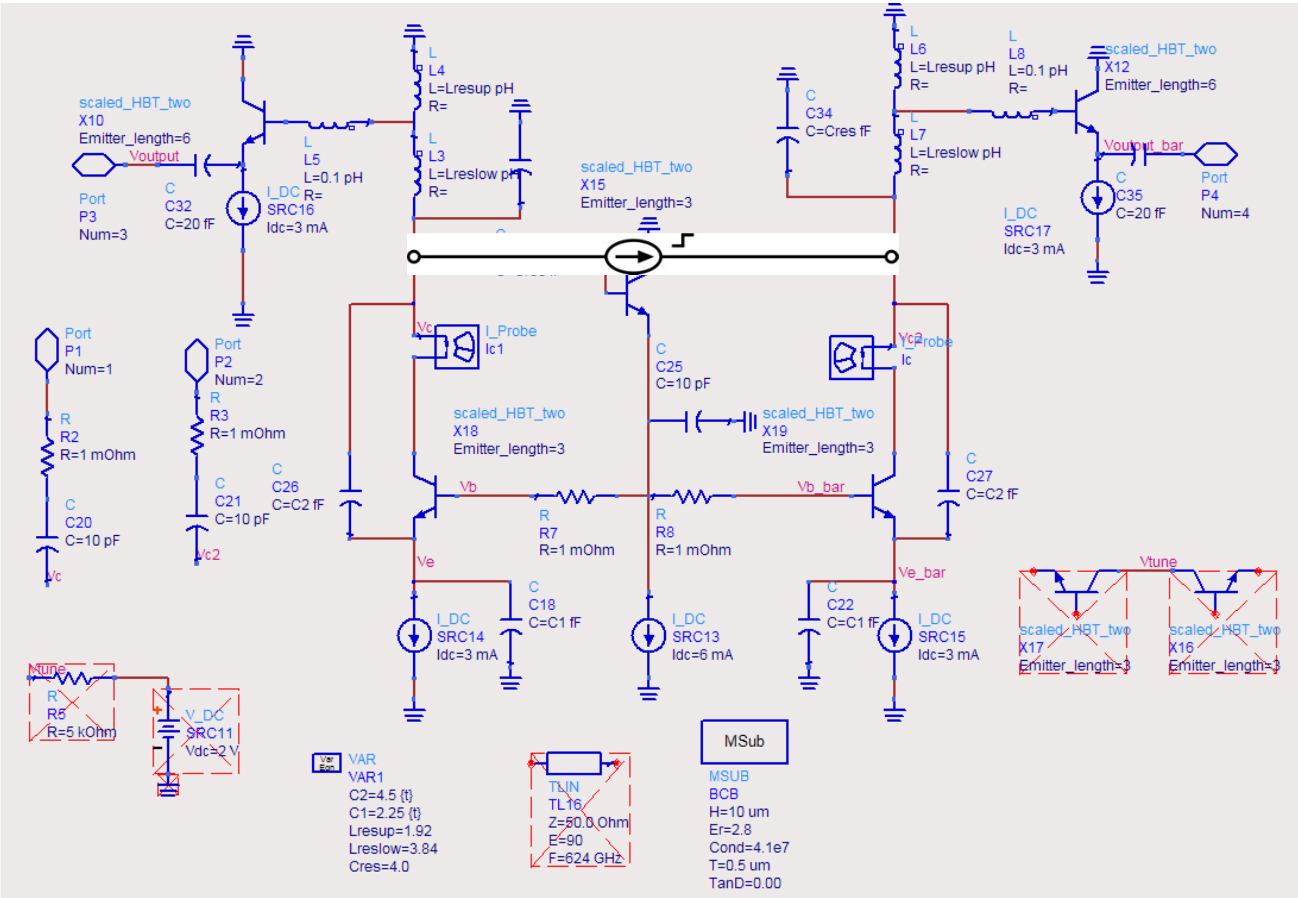
m10
freq=620.0GHz
1000*real(Y(1,1))=-5.579



m16
freq=620.0GHz
imag(Y(1,1))=0.002

Design Example (5): Transient Simulation

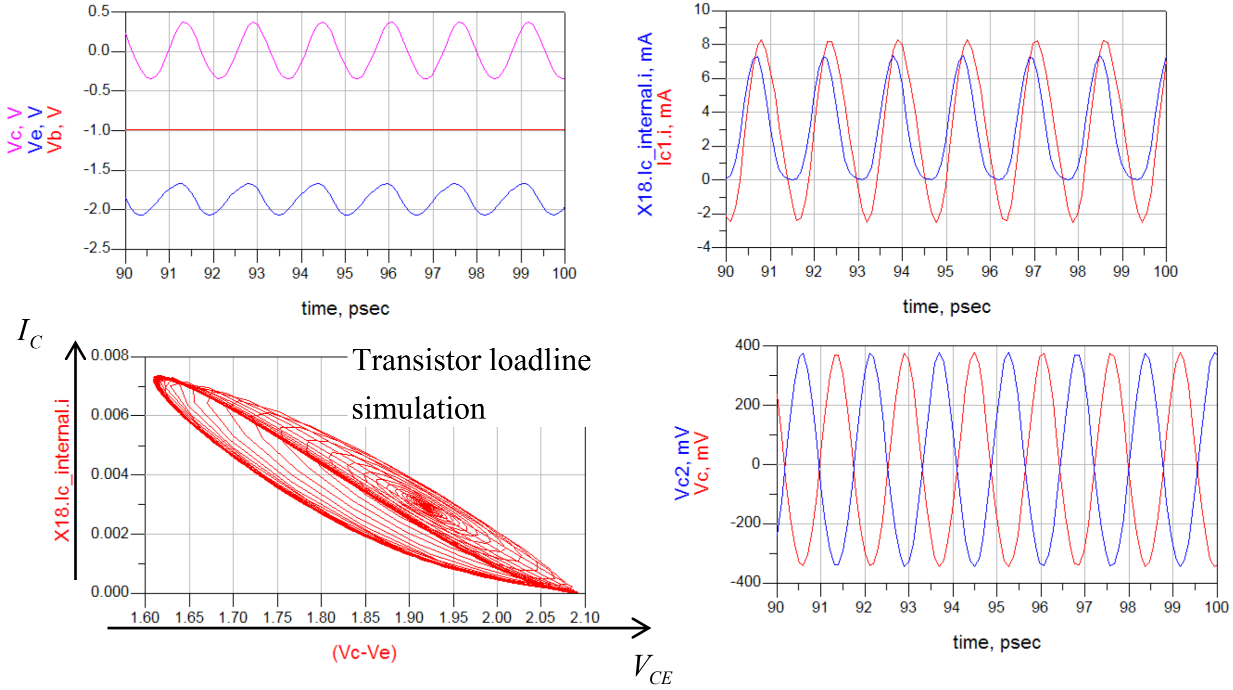
Transient simulation : a small $(\sim 10\mu\text{A})$ current pulse is injected into the resonator and the circuit is simulated.



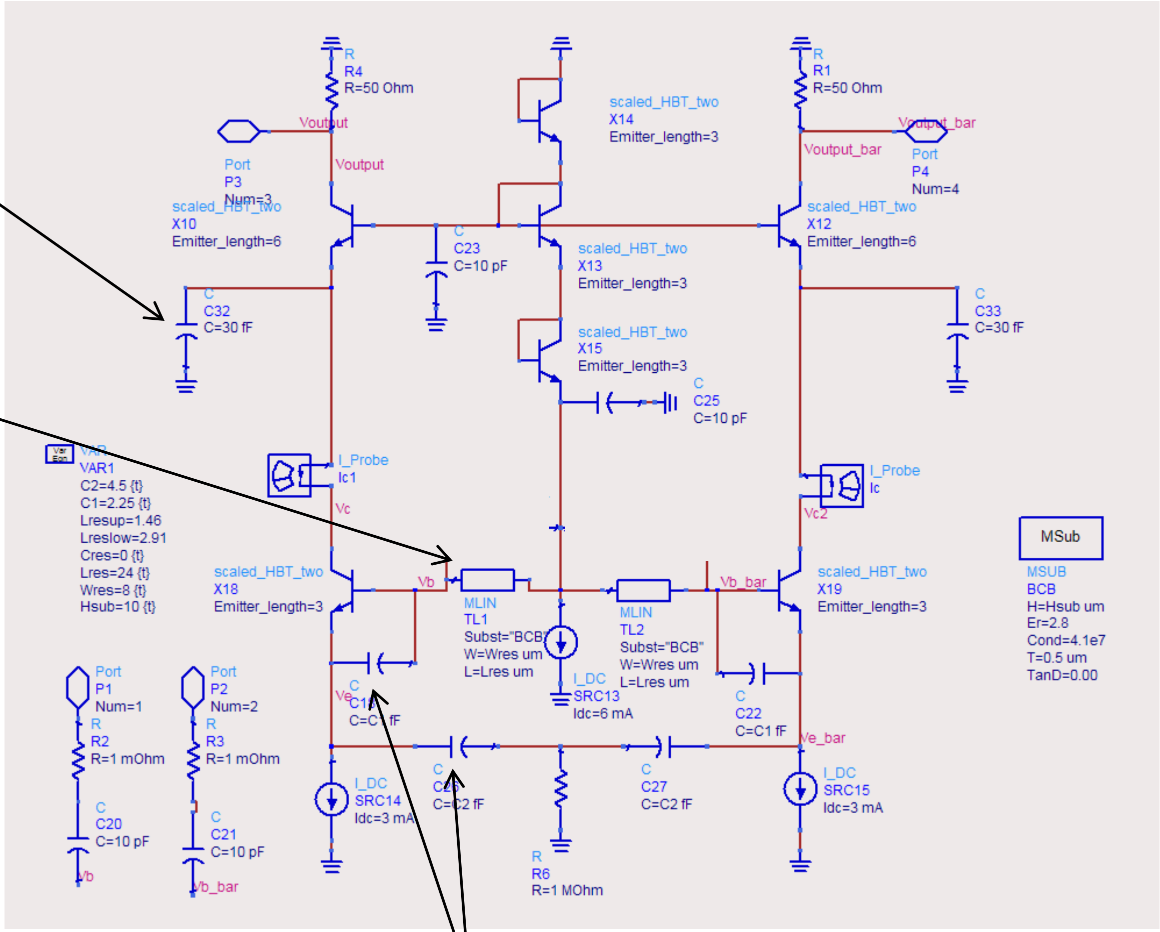
Design Example (5): Transient Simulation

Build - up of oscillation is not shown here.

Note that the time axis starts at 90 ps.



2nd Example : Common-Collector Colpitts



Capacitor reduces loading of oscillator by common - base output buffer

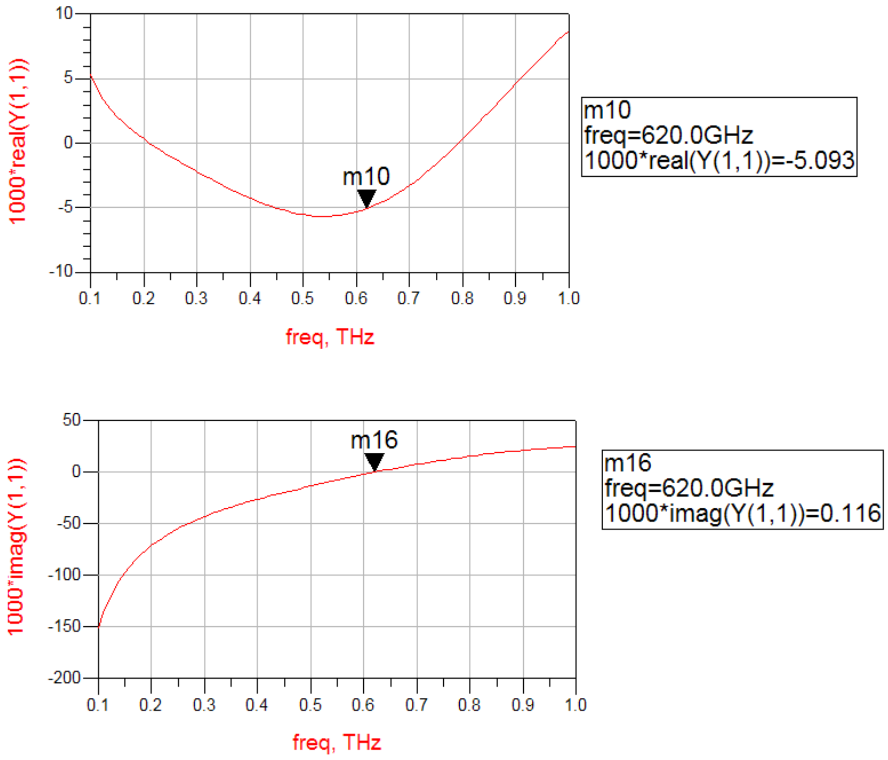
resonator inductor

feedback network

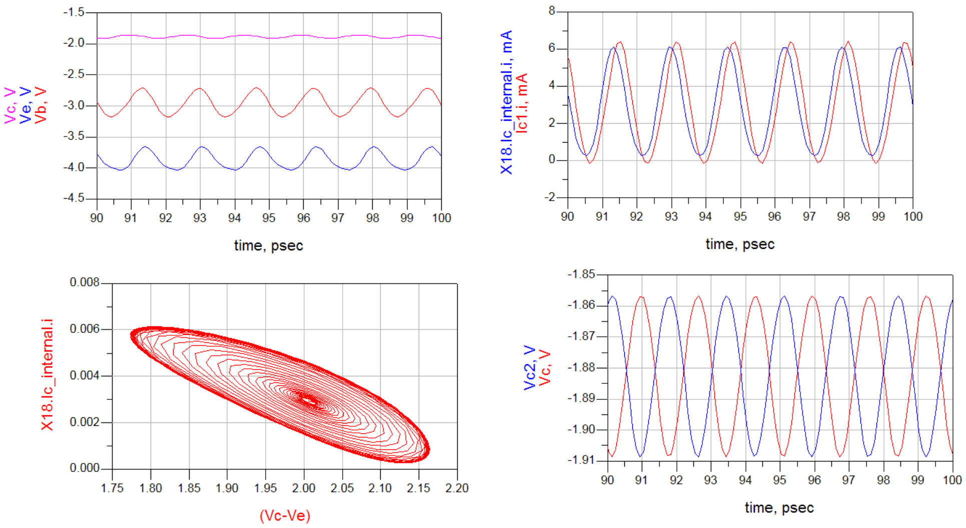
Common - collector Colpitts with common - base output buffer.

2nd Example : Common-Collector Colpitts

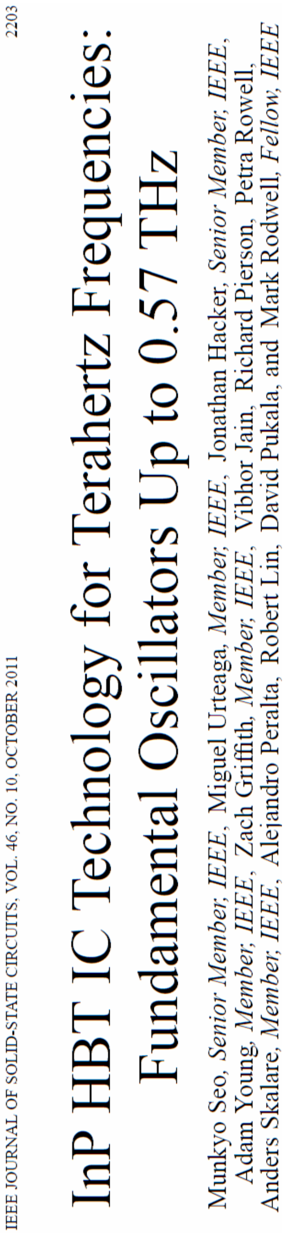
Port admittance



Transient Simulation



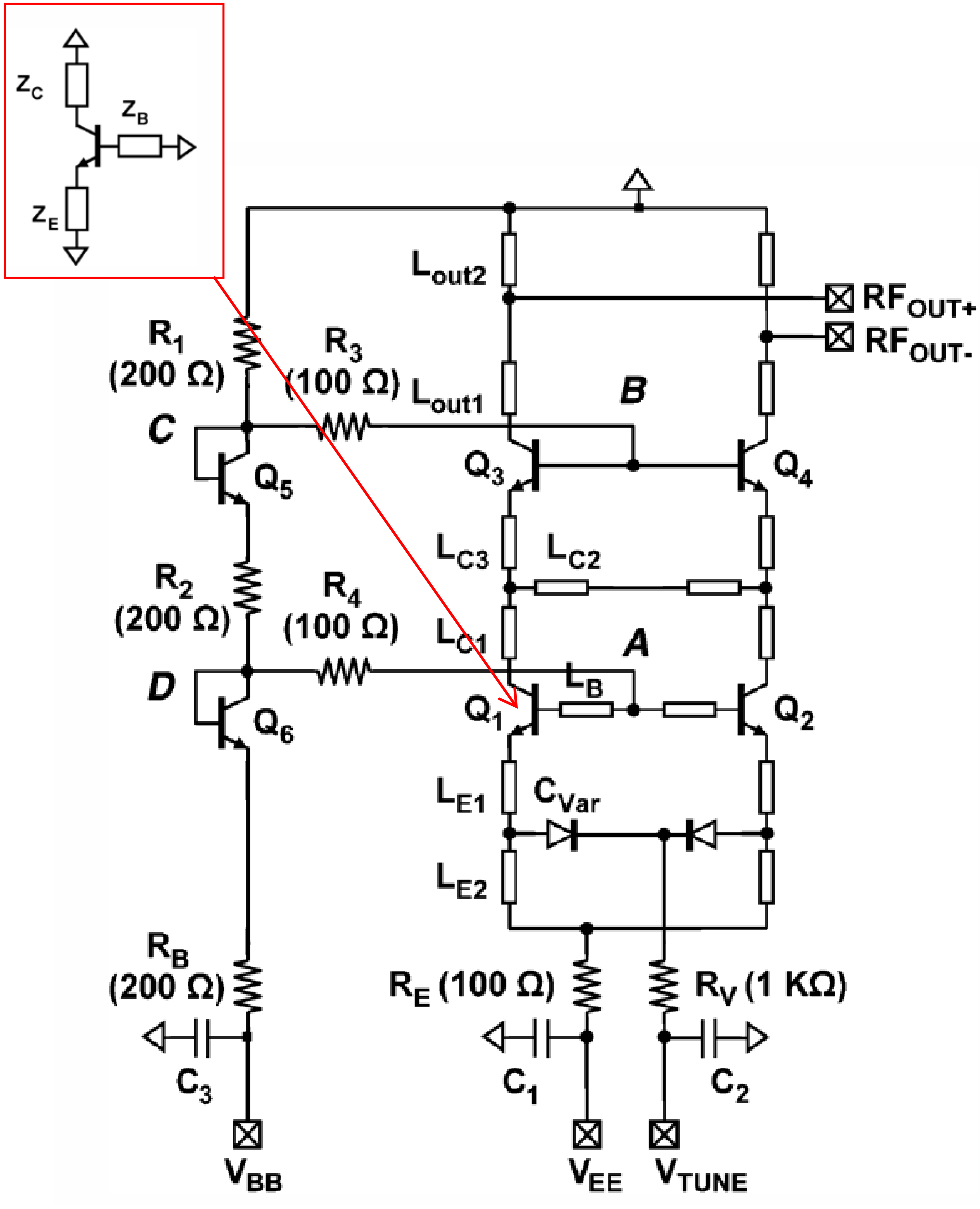
3nd Example : The Real Design



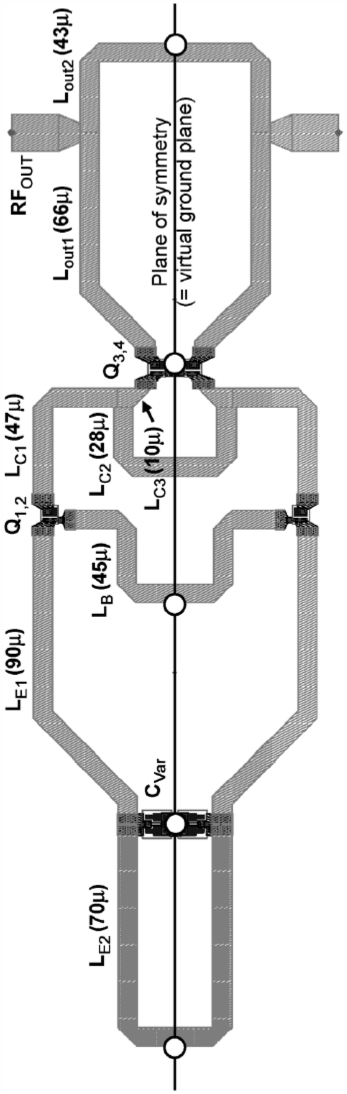
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 46, NO. 10, OCTOBER 2011 2203

InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz

Munkyo Seo, *Senior Member, IEEE*, Miguel Urteaga, *Member, IEEE*, Jonathan Hacker, *Senior Member, IEEE*, Adam Young, *Member, IEEE*, Zach Griffith, *Member, IEEE*, Vibhor Jain, Richard Pierson, Petra Rowell, Anders Skalare, *Member, IEEE*, Alejandro Peralta, Robert Lin, David Pukala, and Mark Rodwell, *Fellow, IEEE*



300 GHz layout



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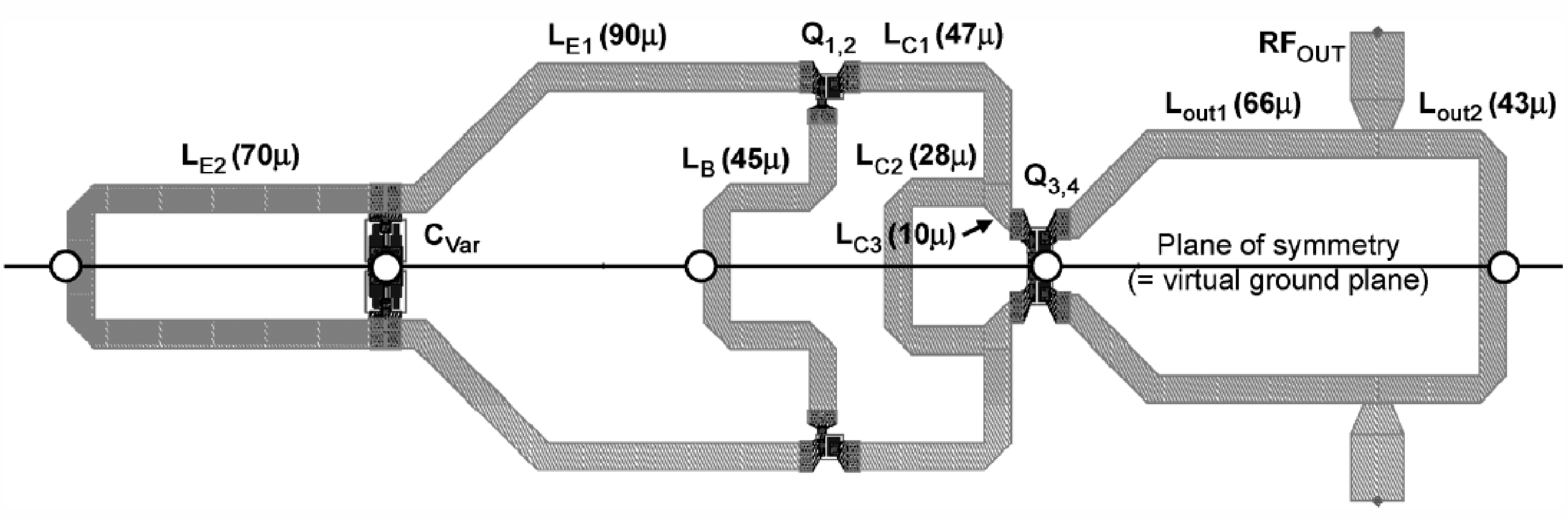
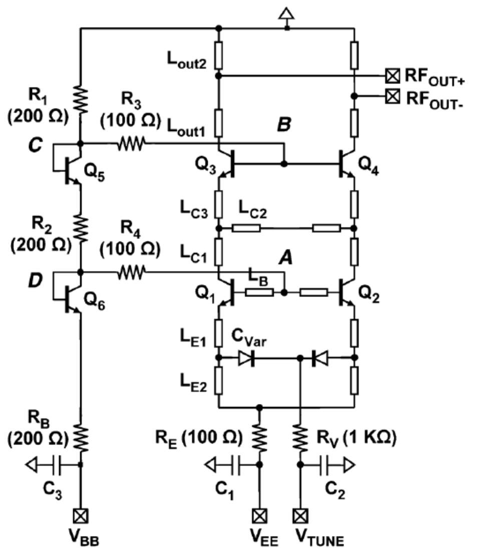
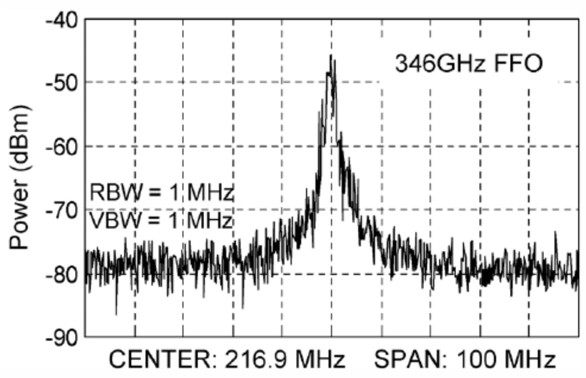
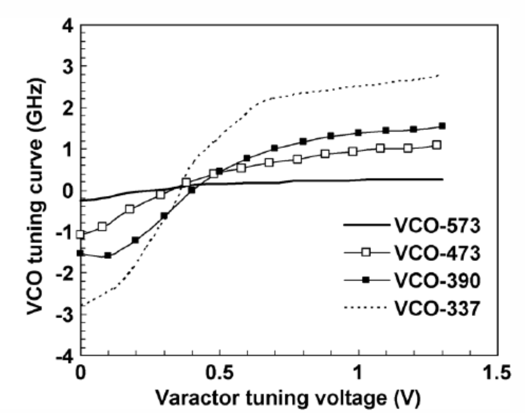
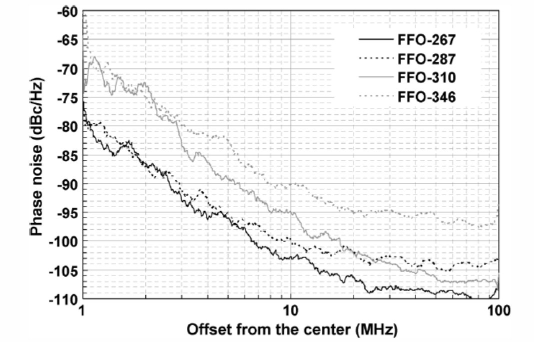


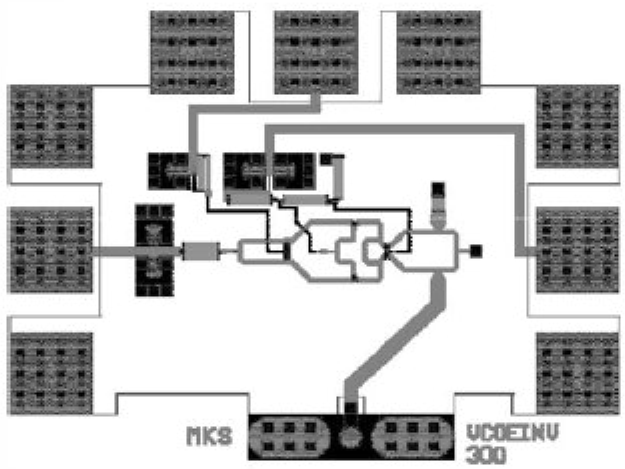


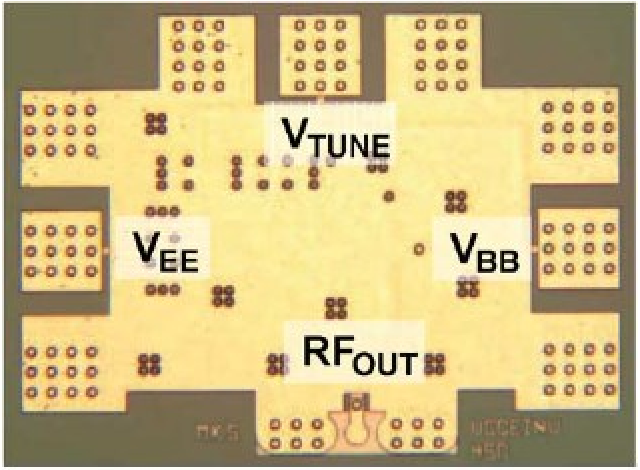
3nd Example : The Real Design

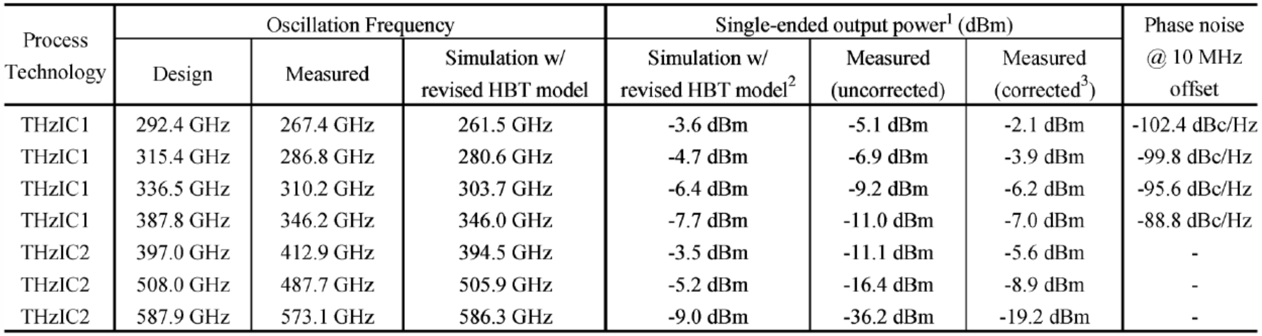












Process Technology	Oscillation Frequency			Single-ended output power[1] (dBm)			Phase noise @ 10 MHz offset
	Design	Measured	Simulation w/ revised HBT model	Simulation w/ revised HBT model[2]	Measured (uncorrected)	Measured (corrected[3])	
THzIC1	292.4 GHz	267.4 GHz	261.5 GHz	-3.6 dBm	-5.1 dBm	-2.1 dBm	-102.4 dBc/Hz
THzIC1	315.4 GHz	286.8 GHz	280.6 GHz	-4.7 dBm	-6.9 dBm	-3.9 dBm	-99.8 dBc/Hz
THzIC1	336.5 GHz	310.2 GHz	303.7 GHz	-6.4 dBm	-9.2 dBm	-6.2 dBm	-95.6 dBc/Hz
THzIC1	387.8 GHz	346.2 GHz	346.0 GHz	-7.7 dBm	-11.0 dBm	-7.0 dBm	-88.8 dBc/Hz
THzIC2	397.0 GHz	412.9 GHz	394.5 GHz	-3.5 dBm	-11.1 dBm	-5.6 dBm	-
THzIC2	508.0 GHz	487.7 GHz	505.9 GHz	-5.2 dBm	-16.4 dBm	-8.9 dBm	-
THzIC2	587.9 GHz	573.1 GHz	586.3 GHz	-9.0 dBm	-36.2 dBm	-19.2 dBm	-