SUBMICRON TRANSFERRED-SUBSTRATE HETEROJUNCTION BIPOLAR TRANSISTORS WITH GREATER THAN 800 GHz \( f_{max} \)

Department of ECE, University of California, Santa Barbara, CA 93106, USA
Tel: 805-893-8044, Fax: 805-893-3262, michelle@vsat.ece.ucsb.edu
* Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, CA 91109, USA

Abstract— We report submicron transferred-substrate AlInAs/GaInAs heterojunction bipolar transistors. Devices with 0.4 \( \mu m \) emitter and 0.4 \( \mu m \) collector widths have 17.5 dB unilateral gain at 110 GHz. Extrapolating at -20 dB/decade, the power gain cut-off frequency \( f_{max} \) is 820 GHz.

I. INTRODUCTION

VERY wide bandwidth heterojunction bipolar transistors (HBTs) [1], [2] will enable microwave analog-digital converters, microwave direct digital frequency synthesis, fiber-optic transmission at \( > 40 \) Gb/s, and wireless data networks at frequencies above 100 GHz.

Such ICs will demand very high transistor current gain cutoff frequency \( f_r \) and power gain cutoff frequency \( f_{max} \). Increases in \( f_r \) are obtained by thinning the collector, and by thinning and grading the base. Unfortunately, thinning the base and collector epitaxial layers increases the base-collector capacitance \( C_{cb} \) and the base resistance \( R_b \), decreasing \( f_{max} \sim \sqrt{f_r/8\pi RC_{cb}} \) where \( C_{cb} \) is the fraction of \( C_{cb} \) charged through the base resistance \( R_b \). Using substrate-transfer processes [3], HBTs can be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. Reducing the emitter and collector widths progressively reduces \( R_b C_{cb} \), and hence \( f_{max} \) increase rapidly with scaling. Subsequently thinning the base and collector epitaxial films will increase \( f_r \) at the expense of \( f_{max} \), and high values of both \( f_r \) and \( f_{max} \) are thus obtained.

We had earlier reported transferred-substrate heterojunction bipolar transistors with 0.8 \( \mu m \) collector junction width and \( > 400 \) GHz \( f_{max} \) [3]. Here we report submicron devices fabricated using electron-beam lithography and (for dimensional control) combined reactive-ion and wet-chemical etches. Devices with 0.4 \( \mu m \) emitter and 0.4 \( \mu m \) collector width obtained DC current gain \( \beta = 50 \) and 17.5 dB unilateral power gain at 110 GHz. Extrapolating at -20 dB/dec results in an estimated 820 GHz \( f_{max} \), the highest reported for any transistor.

II. DEVICE DESIGN AND FABRICATION

The MBE epitaxial layer structure used in this work is similar to [3]. The base is 400 \( \AA \) thick, and is Be-doped at \( 5 \times 10^{17} / \text{cm}^3 \). \( 50 \) meV base bandgap grading, introduced by varying the Ga:In ratio, reduces the base transit time. The collector is 3000 \( \AA \) thick.

The fabrication process is similar to that described in [3]. Emitter contact metal is defined by E-beam litho-
phy at 0.3 μm and 0.5 μm linewidth. The emitter-base junction is formed by CH_4/Ar/H_2 reactive-ion-etching with subsequent selective (acetic/HBr/HCl) and non-selective citric-based wet etches. The etch undercuts 0.05 μm, producing 0.2 μm and 0.4 μm emitter widths (figure 1). Subsequent steps include self-aligned base Ohmic contact deposition, base mesa isolation, polyimide passivation and planarization, and interconnect metal evaporation. The substrate transfer process includes Benzocyclobutene (BCB) deposition, etching and plating to form vias and ground planes, bonding to a transfer substrate with an In_{0.4}P_{0.6} solder, and InP host substrate removal in HCl. Collector metal, with a “T” cross-section, is then defined by E-beam lithography at 0.5, 0.7, and 1.1 μm contact widths. An isotropic collector recess etch to 0.05 μm depth forms collector-base junctions with a tapered profile, reducing C_{cb} while maintaining latitude for emitter-collector misalignment. After etching collector junction widths are 0.4, 0.6, and 1.0 μm. A device schematic cross-section is shown in figure 2.

III. RESULTS

Devices with 0.2 x 6 μm² emitter and 0.4 x 10 μm² collector exhibit DC current gain β = 24, while devices with 0.2 x 6 μm² emitter and 0.6 x 10 μm² collector exhibit β = 42.

The devices were characterized by HP8510 on-wafer network analysis from 0 to 50 GHz and 75-110 GHz using (GGB Inc.) waveguide-coupled microwave wafer probes. To avoid measurement errors (in S_{12}, hence U) arising from microwave probe-probe coupling, the HBTs are separated from the probe pads by 230-μm-length on-wafer microstrip lines. On wafer calibration standards were used to de-embed the transistor S-parameters. The standard Line-reflect-line (LRL) technique was used, with microstrip through line, extended lines for 20-50 GHz and 75-110 GHz calibration, and offset shorts and opens for the reflect standard and for verification. Biasing at V_{ce} = 1.2 volts and I_c = 5.0 mA, devices with 0.4 μm emitter and 0.4 μm collector widths obtained 3.2 dB current gain and 17.5 dB unilateral power gain at 110 GHz (figure 3). Extrapolating at -20 dB/decade, the current gain cut-off frequency f_r is 162 GHz and the power gain cut-off frequency f_{max} is a record 820 GHz. We have used unilateral gain U for extrapolating the power gain cut-off frequency f_{max} because of its characteristic -20 dB/decade slope, its independence of the transistor configuration (common-base vs. common-emitter), and its independence of inductive and capacitive pad parasitics. The common-emitter (figure 3) and common-base (not shown) maximum stable gains are 12.2 dB and 16.0 dB at 110 GHz.

Figure 4 shows a small-signal hybrid-π model for a device with a 0.4 x 6 μm² emitter and a 0.4 x 10 μm² collector biased at I_c = 5 mA and V_{ce} = 1.2 V. Base
Fig. 5. Measured device S-parameters at $V_{cc} = 1.2$ V and $I_c = 5$ mA. The solid line represents S-parameters of the equivalent circuit model.

The measured S-parameters (figure 5), $h_{21}$ and $U$ show good correlation to that of the hybrid-π model. Figure 6 and 7 show the variation of $f_r$ and $f_{max}$ with bias. The drop of $f_{max}$ at high current density and at low $V_{ce}$ is due to the Kirk effect.

![Graph showing variation of $f_r$ and $f_{max}$ with collector-emitter voltage $V_{ce}$](image)

![Graph showing variation of $f_r$ and $f_{max}$ with emitter current density $J_e$](image)

IV. CONCLUSIONS

We have demonstrated submicron transferred-substrate heterojunction bipolar transistors. Devices with $0.4 \times 6 \mu m^2$ emitters and $0.4 \times 10 \mu m^2$ collectors obtained an extrapolated $f_r$ of 162 GHz and $f_{max}$ of 820 GHz. With further scaling, HBTs with $> 1000$ GHz $f_{max}$ should be feasible, permitting ICs operating above 300 GHz [7].

ACKNOWLEDGMENTS

This work was supported by the ONR under grant no. N00014-99-23063 and N00014-98-0068. JPL work performed at the Center for Space Microelectronics Technology, JPL, Caltech, and sponsored by the NASA Office of Space Science.
REFERENCES


