InP/InGaAs/InP DOUBLE HETEROJUNCTION BIPOLAR TRANSISTORS WITH 300 GHz $f_{\text{max}}$

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ABSTRACT

We report InP/InGaAs/InP Double Heterojunction Transistors (DHBTs) with high breakdown voltages in a substrate transfer process. A device with a 400 Å thick graded base, a 500 Å chirped superlattice base-collector grade and a 2500 Å thick InP collector exhibits $f_c = 165$ GHz and $f_{\text{max}} = 300$ GHz with breakdown voltage $BV_{CEO} = 6$ V at a current density, $J_c = 1 \times 10^5$ A/cm$^2$. A device with a 400 Å thick graded base, a 500 Å chirped superlattice base-collector grade and a 1500 Å thick InP collector exhibits $f_c = 215$ GHz and $f_{\text{max}} = 210$ GHz with breakdown voltage $BV_{CEO} = 4$ V at a current density, $J_c = 1 \times 10^4$ A/cm$^2$.

INTRODUCTION

Advances in device technology for heterojunction bipolar transistors (HBTs) are necessary to further improve the performance of associated high speed analogue and digital circuits. The substrate transfer process has yielded InP based single heterojunction bipolar transistors (SHBTs) with outstanding cutoff frequencies [1]. However, SHBTs have low breakdown voltage and high output conductance limiting their use in high voltage and precision analog circuits. Higher breakdown voltages can be achieved by using a wide bandgap material such as InP as the collector. Efforts in this direction have resulted in impressive high frequency performance [2, 3].

Here, we report DHBTs fabricated in the substrate transfer process, a process that allows HBTs to be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer.

<table>
<thead>
<tr>
<th>Material</th>
<th>Doping/(cm$^{-3}$)</th>
<th>Thickness/(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>nInGaAs</td>
<td>$1 \times 10^{19}$</td>
<td>100</td>
</tr>
<tr>
<td>nInGaAlAs</td>
<td>$1 \times 10^{19}$</td>
<td>20</td>
</tr>
<tr>
<td>nInP</td>
<td>$1 \times 10^{19}$</td>
<td>90</td>
</tr>
<tr>
<td>nInAlAs</td>
<td>$8 \times 10^{17}$</td>
<td>30</td>
</tr>
<tr>
<td>nInGaAlAs</td>
<td>$8 \times 10^{17}$</td>
<td>23.3</td>
</tr>
<tr>
<td>nInAlAs</td>
<td>$2 \times 10^{18}$</td>
<td>6.6</td>
</tr>
<tr>
<td>pInGaAs</td>
<td>$4 \times 10^{19}$</td>
<td>40</td>
</tr>
<tr>
<td>nInAlGaAs</td>
<td>$1 \times 10^{26}$</td>
<td>48</td>
</tr>
<tr>
<td>nInAlAs</td>
<td>$2 \times 10^{18}$</td>
<td>2</td>
</tr>
<tr>
<td>nInP</td>
<td>$1 \times 10^{19}$</td>
<td>250</td>
</tr>
<tr>
<td>nInGaAs</td>
<td>$1 \times 10^{19}$</td>
<td>75</td>
</tr>
<tr>
<td>nInAlAs</td>
<td>$UD$</td>
<td>250</td>
</tr>
</tbody>
</table>

The period of the superlattice for the base-collector grade is 1.5 nm. From a material growth perspective, the InP/InGaAs CSL is much more difficult to grow than the InAlAs/InGaAs CSL due to the interfacial strain that builds up as a result of the inter-mixing of group V elements at the interface.

LAYER STRUCTURE AND FABRICATION

The wafers were grown on Fe-doped semi-insulating (100) InP substrates at IQE, Inc. The layer structure is as shown in Table . The conduction band edge discontinuity ($\Delta E_c$) at the base-collector heterointerface is removed by providing a linear bandgap variation for the interfacial region [4] by using a chirped super lattice (CSL). Delta-doped layers are used at the ends of the base-collector grade to create a dipole that cancels the band offset.

Fig. 1: Band diagram, under bias, of a typical device
So, all-arsenide(InAlAs/InGaAs) CSLs have been used to grade all the heterointerfaces.

The emitter and base layers are grown at a lower temperature to reduce Beryllium outdiffusion during and after the growth of the base. Base grading is accomplished by increasing the temperature of the gallium cell after each 50 Å step of base growth to give a progressively wider bandgap In_xGa_1-xAs composition. The composition of InGaAs in the base-emitter grade is the same as that at the base emitter edge. The base layer and the base-emitter grade are therefore strained. The band diagram for a typical device with this layer structure is shown in Fig. 1.

After the emitters are defined, selective wet etch processes are used to define the base-emitter junction and the base mesa [5]. The active junction is then passivated and planarized using polyimide. The substrate transfer process commences with deposition of the PECVD SiN_x insulator layer and the benzocyclobutene(BCB) transmission-line dielectric. Thermal and electrical vias are etched in the BCB. The wafer is electroplated to metalize the vias and to form the ground plane. Subsequently, the wafer is indium-bonded to a GaAs carrier substrate and the InP substrate removed in HCl. InGaAs stop-etch layers are used to prevent the substrate etch from removing the InP collector. Schottky collectors are then deposited, completing the process.

Fig. 2: Scanning Electron Micrograph of a completed transistor

A substrate transfer process of this nature allows HBTs to be fabricated with narrow emitter/base and collector/base junctions on opposing sides of the base epitaxial layer. Reducing the emitter and collector widths progressively reduces \( R_{BA} \), resulting in a rapid increase in \( f_{max} \) with scaling. The layers can subsequently be thinned to obtain high values of both \( f_T \) and \( f_{max} \). Fig. 2 shows the Scanning Electron Micrograph of a completed transistor with a \( 1 \times 8 \mu m^2 \) emitter contact and a \( 1.6 \mu m^2 \) collector contact.

RESULTS AND DISCUSSION

DC performance

Fig. 3 shows typical common-emitter characteristics for a \( 1 \times 8 \mu m^2 \) emitter contact device with a 2000 Å collector depletion layer thickness at low current densities. The transistors demonstrate a common-emitter current gain \( \beta = 40 \) with a breakdown voltage, \( BV_{CEO} > 6V \). The DC offset voltage is \( \sim 0.3 \text{ V} \) and is due to the barrier in the schottky contact. Transistors fabricated with ohmic collectors exhibited a lower offset voltage of \( \sim 0.15 \text{ V} \). Transistors with a 3000 Å thick collector depletion layer thickness demonstrate similar current gain with a breakdown voltage, \( BV_{CEO} > 9 \text{ V} \).

Fig. 3: \( I_C - V_{ce} \) characteristics at low current densities, \( I_B \) is in steps of 15mA

Fig. 4 shows the DC I-V characteristics at higher current densities. The maximum power density, before device failure, is found to be \( 4 \times 10^5 \text{W/cm}^2 \). For devices with 3000 Å collector depletion layer thickness, the maximum power density before device failure is found to be \( 6 \times 10^5 \text{W/cm}^2 \).

Fig. 4: \( J_C - V_{ce} \) characteristics at high current densities, \( I_B \) is in steps of 50mA
Microwave performance

The devices were characterised by measuring the S-parameters on wafer using a 75-110 GHz network analyzer. The current gain (h21) and the power (U) gain are extrapolated at -20 dB/decade to obtain the two figures of merit, f_T, the current gain cutoff frequency and f_max, the maximum frequency of oscillation.

![Graph of Gain vs. Frequency](image)

Fig. 5: RF gains for a DHBT with a 1 x 8 \( \mu \text{m}^2 \) emitter contact. This device has a 400 \( \AA \) thick graded base and a 3000 \( \AA \) thick collector depletion region.

![Graph of Gain vs. Frequency](image)

Fig. 6: RF gains for a DHBT with a 1 x 8 \( \mu \text{m}^2 \) emitter contact. This device has a 400 \( \AA \) thick graded base and a 2000 \( \AA \) thick collector depletion region.

![Graph of Current vs. Voltage](image)

Fig. 7: Variation of f_T and f_max with bias; \( V_{CE} = 2.5V \)

![Graph of Current vs. Voltage](image)

Fig. 8: Variation of f_T and f_max with bias; \( J_e = 6 \cdot 10^4 \text{A/cm}^2 \)

CONCLUSIONS

InP/InGaAs/InP DHBTs have been demonstrated in a substrate transfer process. A peak f_max of 300 GHz was obtained for a device with 1 x 8 \( \mu \text{m}^2 \) emitter contact dimensions, a 400 \( \AA \) thick graded base and a 3000 \( \AA \) thick collector depletion region. The breakdown voltage, \( V_{CEO} \) was found to be \( \sim 6 \text{V} \) at a current density, \( J_e = 1 \cdot 10^8 \text{A/cm}^2 \). A device with a 400 \( \AA \) thick graded base and a 2000 \( \AA \) thick collector depletion region exhibits an f_T = 215 GHz and f_max = 211 GHz. The breakdown voltage, \( V_{CEO} \) was found to be \( \sim 4 \text{V} \) at a current density, \( J_e = 1 \cdot 10^8 \text{A/cm}^2 \). With further scaling, higher values of f_T and f_max should be possible. The Kirk threshold density is found to be low and can be improved by increasing the collector doping. Experiments in this regard are in progress.

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REFERENCES


