InP-based HBTs: Devices and GHz mixed-signal ICs

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Applications:
Applications: optical fiber transceivers at 40 Gb/s and higher

Key advantages for:
TIA, LIA, Modulator driver

Closer competition with SiGe:
MUX/CMU, DMUX/CDR
lower power
problems with integration scale

"40 Gb" is often 44, 48, or 52…
increases InP leverage over SiGe

80 & 160 Gb may come in time
world may not need capacity for some time
WDM might be better use of fiber bandwidth
Applications: military mixed-signal ICs

Radar/Comms transmitter electronics
- direct digital frequency synthesis
- accumulator, sine ROM, DAC

Radar/Comms receiver electronics
- high resolution ADC

Technology requirements
- 3,000 to 30,000 transistors
- Few GHz IF (operating) bandwidths
- ~160 dB/Hz dynamic range
- high resolution drives technology
- speed far beyond signal bandwidth
- 50-100 GHz clock rate digital technologies sought
Applications: wireless / RF

Present Wireless/RF ICs
GaAs HBTs at lower frequencies
InGaAs PHEMTs in higher bands

Opportunities for InP
33 GHz LMDS and 60 GHz metropolitan area networks (IEEE 802.16)
cheap GaAs HBT processes → cheap InP HBT processes
   200 GHz $f_t$ and $f_{\text{max}}$, 8 V BVCEO
quick migration to 6" wafers enabled by metamorphic growth on GaAs

Longer-term opportunities for InP
wider range of RF/wireless applications
…IF SiGe-like integration scales can be reached.
**mmWave Transmission**

Atmospheric attenuation is LOW (~4 dB/km) at bands of interest
60-80 GHz, 120-160 GHz, 220-300 GHz

(Weather permitting)

Geometric path losses are LOW due to short wavelengths.

55 mW transmitter power sufficient for 10 Gb/s transmission over 500 meters range.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit rate</td>
<td>1.00E+10</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>1.50E+11</td>
</tr>
<tr>
<td>F</td>
<td>10 dB</td>
</tr>
<tr>
<td>Distance</td>
<td>5.00E+02</td>
</tr>
<tr>
<td>Atmospheric loss</td>
<td>4.00E-03</td>
</tr>
<tr>
<td>Dant, trans</td>
<td>0.1 m</td>
</tr>
<tr>
<td>Dant, rcvr</td>
<td>0.1 m</td>
</tr>
<tr>
<td>bits/symbol</td>
<td>1</td>
</tr>
<tr>
<td>kT</td>
<td>-173.83 dBm (1Hz)</td>
</tr>
<tr>
<td>Prec</td>
<td>-48.27 dBm</td>
</tr>
<tr>
<td>Δf</td>
<td>1.00E+10 Hz</td>
</tr>
<tr>
<td>transmission</td>
<td>-63.68 dB</td>
</tr>
<tr>
<td>atmospheric loss</td>
<td>2 dB</td>
</tr>
<tr>
<td>P transmitter</td>
<td>55.1 mW</td>
</tr>
</tbody>
</table>
Transistor
Figures of Merit
Short-circuit current gain cutoff frequency

short-circuit current gain:
drive input, short output,
measure $H_{21} = \frac{I_{\text{out}}}{I_{\text{in}}}$

$$H_{21}(f) \approx \frac{1}{\left(\frac{1}{\beta} + (jf / f_\tau)\right)}$$

![Circuit diagram with labels: $V_{\text{gen}}$, $R_{\text{gen}}$, $I_{\text{in}}$, $I_{\text{out}}$, $V_{\text{be}}$, $R_x = 433 \Omega$, $C_{\text{ch}} = 2.3 \text{ fF}$, $C_{\text{ch}} = 6.9 \text{ fF}$, $r_{\text{ch}} = 7000 \Omega$, $C_{\text{diff}} = 172 \text{ fF}$, $C_{\text{je}} = 34 \text{ fF}$, $g_m = g_{\text{mos}} \exp(-j\omega\tau_c)$, $g_m V_{\text{be}}$, $R_c = 4.7 \Omega$, $g_{\text{mos}}$, $\tau_c$]
Current-gain cutoff frequency in HBTs

\[
\frac{1}{2\pi f_\tau} = \tau_{base} + \tau_{collector} + C_{je} \frac{kT}{qI_E} + C_{bc} \left( \frac{kT}{qI_E} + R_{ex} + R_{coll} \right)
\]

\[
\tau_{base} \approx T_b^2 / 2D_n \quad \tau_{collector} \approx T_c / 2\nu_{sat}
\]

RC terms are quite important for > 200 GHz \( f_\tau \) devices
\( f_\tau \) is a questionable metric for high speed digital logic
…where capacitance charging has proportionally larger role
Measurement of power gains and $f_{\text{max}}$

**Maximum Available Gain**
Simultaneously match input and output of device

$$\text{MAG} = \frac{|S_{21}|}{|S_{12}|} \left( K - \sqrt{K^2 - 1} \right)$$

$K = \text{Rollet stability factor}$

Transistor must be unconditionally stable or MAG does not exist

**Maximum Stable Gain**
Stabilize transistor and simultaneously match input and output of device

$$\text{MSG} = \frac{|S_{21}|}{|S_{12}|} = \frac{|Y_{21}|}{|Y_{12}|} \approx \frac{1}{\omega C_{eb} \left( R_{ex} + \frac{kT}{qI_c} \right)}$$

Approximate value for hybrid-$\pi$ model

To first order MSG does not depend on $f_\tau$ or $R_{bb}$

For Hybrid-$\pi$ model, MSG rolls off at 10 dB/decade, MAG has no fixed slope. So, NEITHER can be used to accurately extrapolate $f_{\text{max}}$

MSG/MAG is however of direct relevance in tuned RF amplifier design
Mason’s Unilateral Power Gain

Use lossless reactive feedback to cancel device feedback and stabilize the device, then match input/output.

\[
U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}
\]

U is not changed by pad reactances

For Hybrid-\(\pi\) model, U rolls off at 20 dB/decade

ALL Power Gains must be unity at \(f_{\text{max}}\)

Monolithic amplifiers not easily made unilateral, so U of only historical relevance to IC design. U is usually valuable for \(f_{\text{max}}\) extrapolation
Excess Collector Capacitance, \( f_{\text{max}} \), and Device Utility

The partitioning between \( C_{\text{cbi}} \) and \( C_{\text{cbx}} \) will be discussed later. 

\( C_{\text{cbx}} \) has no effect upon \( f_{\text{max}} \) or \( U \).

\( C_{\text{cbx}} \) has a large impact upon common - emitter MSG,  

hence has large impact on usable gain in mm - wave circuits.

\( C_{\text{cbx}} \) has a large impact upon digital logic speed.

*high \( f_{\text{max}} \) does not mean low \( C_{\text{cb}} \) or fast logic*
What do we need: $f_\tau$, $f_{\text{max}}$, or ...?

Tuned ICs (MIMICs, RF):
- $f_{\text{max}}$ sets gain, and max frequency, not $f_t$.
- Low $f_t/f_{\text{max}}$ ratio makes tuning design hard (high Q)
- High $C_{cbx}$ reduces MSG

Lumped analog circuits
- Need high & comparable $f_t$ and $f_{\text{max}}$.
- $C_{cb}/I_c$ has major impact upon bandwidth

Distributed Amplifiers
- In principle, $f_{\text{max}}$-limited, $f_t$ not relevant....
- (Low $f_t$ makes design hard)

digital ICs will be discussed in detail later
transistor
layer structures
SHBT layer structure

<table>
<thead>
<tr>
<th>Layer</th>
<th>Material</th>
<th>Doping</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter cap</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>$2 \times 10^{19}$ cm$^{-3}$: Si</td>
<td>300</td>
</tr>
<tr>
<td>N$^+$ emitter</td>
<td>InP</td>
<td>$2 \times 10^{19}$ cm$^{-3}$: Si</td>
<td>700</td>
</tr>
<tr>
<td>N$^-$ emitter</td>
<td>InP</td>
<td>$8 \times 10^{17}$ cm$^{-3}$: Si</td>
<td>500</td>
</tr>
<tr>
<td>Emitter-base grade</td>
<td>In$<em>{0.55}$Ga$</em>{0.26}$Al$<em>{0.21}$As to In$</em>{0.455}$Ga$_{0.545}$As</td>
<td>P: $4 \times 10^{17}$ cm$^{-3}$: Si, N: $8 \times 10^{17}$ cm$^{-3}$: C</td>
<td>233, 47</td>
</tr>
<tr>
<td>Base</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>N: $4 \times 10^{19}$ cm$^{-3}$: C</td>
<td>400</td>
</tr>
<tr>
<td>Collector</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>N: $2 \times 10^{16}$ cm$^{-3}$: Si</td>
<td>2000</td>
</tr>
<tr>
<td>Subcollector</td>
<td>InP</td>
<td>N: $1 \times 10^{19}$ cm$^{-3}$: Si</td>
<td>$\sim$1000 Å</td>
</tr>
</tbody>
</table>

**very low breakdown:**
scaling beyond $\sim$75 GHz
digital clock rate very difficult

**high collector-base leakage**
particularly at elevated temperatures.
Serious difficulties in real applications

**very high thermal resistance**
InGaAs collector and subcollector
DHBT Layer structure

B-C grade design is critical

InGaAs or GaAsSb bases
GaAsSb more easily passivated
otherwise comparable

high breakdown
important for microwave power
important for logic

low thermal resistance
essential for high power density
important for microwave power
important for logic

Performance
ft and fmax good or better than SHBTs

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</tr>
<tr>
<td>Base</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>N: 4 × 10$^{19}$ cm$^{-3}$. C</td>
<td>400</td>
</tr>
<tr>
<td>Base-collector grade</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As to In$<em>{0.53}$Ga$</em>{0.26}$Al$_{0.21}$As</td>
<td>N: 2 × 10$^{16}$ cm$^{-3}$. Si</td>
<td>240</td>
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<tr>
<td>Pulse doping</td>
<td>InP</td>
<td>5.6 × 10$^{18}$ cm$^{-3}$. Si</td>
<td>30</td>
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<tr>
<td>Collector</td>
<td>InP</td>
<td>N: 2 × 10$^{16}$ cm$^{-3}$. Si</td>
<td>1,630</td>
</tr>
<tr>
<td>Subcollector</td>
<td>InP</td>
<td>N: 1 × 10$^{19}$ cm$^{-3}$. Si</td>
<td>~1000 Å</td>
</tr>
</tbody>
</table>
Alternative InP DHBT base-collector junction designs

Several layer alternatives exist for DHBTs with:
- high $f_t$
- high current density
- negligible current blocking
- low base sheet and contact resistivity

UCSB: InGaAs base, MBE

Mattias Dahlstrom

InAlAs/InGaAs superlattice

InP collector

InGaAs setback

InGaAs base

InP/GaAsSb/InP DOUBLE HETEROJUNCTION Bipolar TRANSISTORS WITH HIGH cut-off FREQUENCIES and BREAKDOWN VOLTAGES

N. Main, M. W. Dvorak, X. G. Xu, S. P. Watkins, and C. R. Bolognesi

InP/InGaAs DHBTs with 341-GHz $f_t$ at high current density of over 800 kA/cm²

Minoru Iida, Kenji Kurishima, Noriyuki Watanabe, and Takatomo Enoki

IEDM 2001
transistor
process flow
(research-lab-like)
1) emitter metal liftoff

scale: 1x1 um
2) base recess etch

scale: 1x1 um
3) **base metal deposition**

*scale: 1x1 um*
4) collector mesa etch

dimension: 1x1 um
5) *etch through base to subcollector, collector Ohmics*
6) liftoff base-collector vias

scale: 1x1 um
7) **planarize**: spin on BCB or polyimide & etch back
8) deposit interconnect metal
Problems with mesa process flow

Large Parasitic Collector Junction, Large Excess Ccb
resembles Si bipolar processes of 1960's!
parasitic collector junction lies under base contacts
base contacts must be nonzero size: nonzero resistivity
base contacts must be nonzero size: lithographic impact on yield

Self-aligned emitter-base process flow
base-emitter short-circuits
problems with wet-etch undercut control
problems with dry-etch reproducibility

Nonplanar process
loss of yield in back-end process
**Problems with mesa process flow**

- Emitter-base junction is 3 μm$^2$
- Collector-base junction is 12 μm$^2$
- Collector/emitter area ratio
- Even worse in non-self-aligned processes...

While research-lab processes have moderate Ccb, processes aimed at high yield at >3000 HBTs have very large collector junctions.

Ccb then the dominant circuit parasitic, regardless of impact on $f_\tau$ & $f_{\text{max}}$. 
transistor
key parasitics
and model
Emitter Resistance

Emitter resistance: one limiting factor in scaling for speed high speed devices: high $J \rightarrow$ low $\left(\frac{C_{cb}}{I_c}\right)$ but high $J \rightarrow$ excessive $\left(I_E R_{ex}\right)$ voltage drop

evidence of edge depletion or damage

\[
R_{ex} = \frac{\rho_c}{L_E (W_E - \Delta W)}
\]

\[
\frac{1}{R_{ex}} = \left(\frac{L_E}{\rho_c}\right)(W_E - \Delta W)
\]

Dino Mensa
Current Gain: surface leakage

Surface Conduction:
InGaAs has low surface recombination velocity.
InGaAs has surface pinning near conduction band.
→ weak surface inversion layer on base, surface conduction to base contact
Problem aggravated by InP emitter, as this also pins near conduction band

\[
\frac{1}{\beta} = \frac{I_b}{I_c} = \frac{I_{\text{surface}}}{I_c} + \frac{I_{\text{bulk}}}{I_c} = \frac{P_E(k_1 qn_po)}{A_E(qn_po D_n / W_b)} + \frac{1}{\beta_{\text{bulk}}}
\]

evidence of surface conduction

Be: InGaAs
4E19/cm³ doping
Current Gain: Auger recombination

Carbon base doping: above $10^{20} / \text{cm}^2$ feasible

Bulk recombination dominated by Auger

$$\tau_{\text{Auger}} \propto 1/N_A^2$$

Since $$\tau_{\text{base}} \propto 1/T_B^2$$

$$\beta \propto 1/(N_A T_B)^2 \propto 1/\rho_{\text{sheet}}^2$$

This constrains $\rho_{\text{sheet}}$ reduction through high base doping

But, high base doping + thin base

$\Rightarrow$ low base contact resistivity, low transit time
Base Transit Time

Assumes:

\[ D_N = 40 \text{ cm}^2 / \text{V - sec} \]
\[ v_{exit} = 3 \cdot 10^7 \text{ cm/s} \]

Base Thickness (Angstroms)

\[ \tau_b = \frac{W_b L_g}{D_n} \left( L_g^2 / D_n - L_g / v_{sat} \right) \left( 1 - e^{-W_b/L_g} \right) \]

where \( L_g \) is the grading length:

\[ L_g = W_b \left( kT / \Delta E_g \right) \]

Drift - diffusion model correct if

\[ \tau_b \gg \tau_m \approx D_n m^* / kT \approx 35 \text{ fs} \]
Base Bandgap vs. Doping Grading

Objective: introduce a 52 meV potential drop across base.

Case 1: base bandgap grading.
Vary In : Ga ratio: $\text{In}_{0.455}\text{Ga}_{0.545}\text{As} \leftrightarrow \text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (strained)

Case 2: base doping grading, non-degenerate base
Base doping near emitter side constrained by growth/reliability
Reduce doping at collector side of base by $e^{-2} : 1 = 0.12 : 1$
⇒ greatly increased base sheet resistance
⇒ Contact resistance increased: contacts land somewhere in middle of base

Case 3: base doping grading, degenerate base
Degenerate doping statistics: small doping change induces big field
With heavy doping, Auger-induced $\beta$ collapse sets maximum $\int_0^{T_b} p(x)dx$
Can introduce built-in field without degrading sheet resistance.
Collector Transit Time

From elementary electrostatics (refer to sketch)

\[ \tau_c = \int_0^{T_c} \frac{1 - x / T_c}{v(x)} dx \equiv \frac{T_c}{2v_{eff}} \]

\( \tau_c \) is more sensitive to velocity near base.

Fortuitous, as initial velocity is high, then decreases due to \( \Gamma - L \) scattering.
Collector Transit Time

...from best fit to RF data

Velocities in InGaAs collectors

\[3 - 5 \cdot 10^7 \text{ cm/s for } \sim 2000 \text{ Å layers}\]

Velocities in InP collectors

also \[3 - 5 \cdot 10^7 \text{ cm/s for } \sim 2000 \text{ Å layers}\]
Current-induced Collector Velocity Overshoot (?)

Effect predicted by Ishibashi

\[ \tau_{ec} \] data *does* show predicted trend.

**BUT**: \( \tau_{ec} \) variation may also be due to modulation in emitter ideality factor with bias current \( \left( \frac{1}{g_m} \right. \) often does not vary as \( R_{ex} + \frac{kT}{qI_E} \). \( C_{je} \) also varies with bias.
This "mesh model" can be entered into a microwave circuit simulator (e.g. Agilent ADS) to predict $f_{\text{max}}$, etc.
Components of $R_{bb}$ and $C_{cb}$

\[ R_{horiz} = \frac{\rho_s W_{bc}}{2L_E} \]

\[ R_{cont} = \sqrt{\frac{\rho_s \rho_v}{2L_e}} \]

\[ R_{gap} = \frac{\rho_s W_{eb}}{2L_e} \]

\[ R_{spread} = \frac{\rho_s W_e}{12L_e} \]

\[ C_{cb,ext} = 2\epsilon_LW_{cb}/T_c \]

\[ C_{cb,\text{gap}} = 2\epsilon_LW_{eb}/T_c \]

\[ C_{cb,e} = \epsilon L_e W_e / T_c \]

\[ R_x = R_{horiz} + R_{vert} \parallel R_{cont} = R_{cont} ! \]
Components of base spreading resistance

With submicron emitters (or with ~1E20 base doping) \( R_{bb} \) is dominated by \( R_{\text{contact}} \) and \( R_{\text{gap}} \).

Given that emitter area \( A_E = L_E W_E \) is fixed:
- decreased emitter width \( W_E \)
- results in increased emitter length \( L_E \).

\[ R_{bb} = R_{\text{cont}} + R_{\text{gap}} + R_{\text{spread}} \]
\[ R_{\text{cont}} = \sqrt{\rho_s \rho_v / 2 L_E} \]
\[ R_{\text{gap}} = \rho_s W_{eb} / 2 L_E \]
\[ R_{\text{spread}} = \rho_s W_e / 12 L_E. \]
## Typical base parameters

<table>
<thead>
<tr>
<th>Type</th>
<th>Carrier Density</th>
<th>Energy Level</th>
<th>Thickness</th>
<th>Sheet Resistance</th>
<th>Carrier Mobility</th>
<th>Lifetime</th>
<th>Diffusion Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 \cdot 10^{19} / cm^3 Be-doped InGaAs base</td>
<td>10^{19} cm^{-3}</td>
<td>52 meV grading</td>
<td>400 Å thick</td>
<td>750 Ohms/square</td>
<td>10 Ohm - \mu m^2</td>
<td>170 fs</td>
<td>40 cm^2 / s</td>
</tr>
<tr>
<td>7 \cdot 10^{19} / cm^3 C-doped InGaAs base</td>
<td>10^{19} cm^{-3}</td>
<td>52 meV (doping) grading</td>
<td>300 Å thick</td>
<td>700 Ohms/square</td>
<td>&lt;10 Ohm - \mu m^2</td>
<td>100 fs</td>
<td>40 cm^2 / s</td>
</tr>
<tr>
<td>8 \cdot 10^{19} / cm^3 C-doped GaAsSb base</td>
<td>10^{19} cm^{-3}</td>
<td>?? meV grading</td>
<td>250 Å thick</td>
<td>1000 Ohms/square</td>
<td>\approx 20 Ohm - \mu m^2</td>
<td>\approx 150 – 200 fs</td>
<td>\approx 20 cm^2 / s</td>
</tr>
</tbody>
</table>

(Dvorak)
Pulfrey / Vaidyanathan f_{max} model

Note that the external capacitance \( C_{cb,ext} \) is charged through a relatively low resistance, less than \( R_{vert} \).

\[
C_{cb,ext} \left( R_{cont} \parallel R_{vert} \right) < C_{cb,ext} R_{vert}
\]

\[
= \frac{\varepsilon}{T_c} \frac{1}{\rho_{contact}}
\]

...the associated charging time is relatively small

\( C_{cb,ext} \) has moderate effect upon \( f_{\text{max}} \), but big impact upon digital and analog speed
C\textsubscript{cb} Cancellation by Collector Space-Charge

$$\delta V_{cb} = \frac{\partial Q_{base}}{\partial V_{cb}} = \frac{\varepsilon A}{T_c} - \frac{\partial}{\partial V_{cb}} \left( \frac{I_c T_c}{2 V_{sat}} \right)$$

$$\Rightarrow C_{cb} = \frac{\varepsilon A}{T_c} - I_c \frac{\partial \tau_c}{\partial V_{cb}}$$

Collector space charge screens field,
Increasing voltage decreases velocity,
→ modulates collector space-charge
→ offsets modulation of base charge
→ C\textsubscript{cb} is reduced

\begin{itemize}
  \item \textit{Even if you don't care about fmax, the effect can confuse HBT model extraction}
\end{itemize}

\textbf{measured 0.64 fF decrease}
equivalent circuit model
Transistor Hybrid-Pi equivalent circuit model

\[ g_{m0} = \frac{qI_E}{kT} \]
\[ g_m = g_{m0} e^{-j\omega(\gamma \tau_b + \tau_c)} \]
\[ C_{be} = C_{je} + g_m (\tau_b + \tau_c) \]
Comments regarding the Hybrid-Pi model

The common-base (T) model directly models frequency-dependent transport.

The hybrid-pi model results from a fit to the T to first order in \( \omega \).

The capacitance \( C_{be,diff} \) models the effect of \( (\tau_b + \tau_c) \) on input impedance.

The \( g_m \) generator nevertheless also requires an associated \( \sim (0.2 \cdot \tau_b + \tau_c) \) delay (important in fast IC design).

\( R_{bb}C_{cbi} \) and \( C_{cbx} \) represent fits to the distributed RC base-collector network.
Collector field-screening (Kirk Effect)
Kirk effect in DHBTs: not base pushout, but current-blocking

\[
\frac{d^2 \phi}{dx^2} = \rho = \frac{qN_d - J}{\varepsilon}
\]

Bandbending under high \( J \) and low \( V_{ce} \) results in current blocking

\( \Rightarrow \) decrease in \( \beta \) and \( f_\tau \)

\[
V_{ce} = 0.7 \text{ V}, \ J_e = 0 \text{ kA/cm}^2, \ v_{sat,eff} = 4 \cdot 10^7 \text{ cm/s}
\]

\[
V_{ce} = 0.7 \text{ V}, \ J_e = 1000 \text{ kA/cm}^2, \ v_{sat,eff} = 4 \cdot 10^7 \text{ cm/s}
\]

\[
V_{ce} = 1.2 \text{ V}, \ J_e = 1000 \text{ kA/cm}^2, \ v_{sat,eff} = 4 \cdot 10^7 \text{ cm/s}
\]
Kirk effect in DHBTs

Decrease in $f_\tau$ and $f_{\text{max}}$ at lower $J$
Kirk-effect threshold increases with increased $V_{ce}$

$$J_{\text{max}} = 2\varepsilon V_{sat} (V_{cb} + V_{cb,\text{min}} + 2\phi) / T_c^2$$

$$\approx 2\varepsilon V_{sat} (V_{ce} + V_{ce,\text{min}}) / T_c^2$$

Increase in $V_{ce,\text{sat}}$ with increased $J$

$$\frac{dV_{ce}}{dI_c} = R_{\text{space-charge}} = \frac{T_c^2}{2\varepsilon V_{sat} A_{\text{effective}}}$$

where the effective collector current flux area is

$$A_{\text{effective}} \approx L_E (W_E + 2T_C)$$
Kirk effect in SHBTs: base pushout, increased $C_{cb}$

Base pushes out.
Holes compensate electrons
$C_{cb}$ increases.

$V_{ce} = 0.7$ V, $J_e = 500$ kA/cm$^2$, $v_{sat,eff} = 3 \cdot 10^7$ cm/s

$C_{cb}$ increases

Base pushes out
Kirk effect with Nonuniform Collector Electron Velocity

From transit time analysis,

\[ \tau_c = \frac{T_c}{v(x)} \int_0^T \left(1 - \frac{x}{T_c}\right) dx \equiv \frac{T_c}{2v_{\text{eff}}} \]

\( \tau_c \) and \( v_{\text{eff}} \) are more sensitive to velocity near base.

Kirk effect with uniform collector velocity:

\[ J_{\text{max}} = \frac{2 \varepsilon v_{\text{sat}} (V_{cb} + V_{cb, \text{min}} + 2\phi)}{T_c^2} \]

\[ \equiv \frac{2 \varepsilon v_{\text{sat}} (V_{ce} + V_{ce, \text{min}})}{T_c^2} \]

Kirk effect with NONuniform collector velocity:

\[ J_{\text{max}} = \frac{2 \varepsilon v_{\text{eff}} (V_{cb} + V_{cb, \text{min}} + 2\phi)}{T_c^2} \]

\[ \equiv \frac{2 \varepsilon v_{\text{eff}} (V_{ce} + V_{ce, \text{min}})}{T_c^2} \]

Nonuniform collector electron velocity doesn't profoundly change Kirk effect…
transistor scaling theory
**HBT scaling: layer thicknesses**

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, \( \tau \)'s

- Reduce \( T_b \) by \( \sqrt{2}:1 \)
  \[ \rightarrow \tau_b \text{ improved } 2:1 \]

- Reduce \( T_c \) by 2:1
  \[ \rightarrow \tau_c \text{ improved } 2:1 \]

Note that \( C_{cb} \) has been **doubled**

Assume \( W_C \sim W_E \)

\[
\tau_b \approx \frac{T_b^2}{2D_n} \\
\tau_b \approx \frac{T_c}{2v_{sat}}
\]
HBT scaling: lithographic dimensions

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ 's

Base Resistance $R_{bb}$ must remain constant
→ $L_e$ must remain ~ constant

$R_{bb} = R_{gap} + R_{spread} + R_{contact}$
≈ $R_{contact}$

$= \sqrt{\rho_{sheet} \rho_{c,vertical}} / 2L_E$

$Ccb/Area$ has been **doubled**
..we had wanted it 2:1 smaller
...must make area=$L_e W_e$ 4:1 smaller
→ must make $W_e$ & $W_c$ 4:1 smaller

reduce collector width 4:1
reduce emitter width 4:1
keep emitter length constant

Assume $W_C \sim W_E$
HBT scaling: emitter resistivity, current density

2:1 improved device speed: keep G's, R's, I's, V's constant, reduce 2:1 all C's, τ's

Emitter Resistance $R_{ex}$ must remain constant but emitter area $L_e W_e$ is 4:1 smaller resistance per unit area must be 4:1 smaller

Collector current must remain constant but emitter area $L_e W_e$ is 4:1 smaller and collector area $L_c W_c$ is 4:1 smaller current density must be 4:1 larger

increase current density 4:1 reduce emitter resistivity 4:1

Assume $W_C \sim W_E$
**Scaling Laws, Collector Current Density, $C_{cb}$ charging time**

**Collector Field Collapse (Kirk Effect)**

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

**Collector Depletion Layer Collapse**

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow J_{\max} = 2\varepsilon v_{sat} (V_{cb} + V_{cb,\min} + 2\phi) / T_c^2$$

Note that $V_{be} \equiv \phi$, hence $(V_{cb} + \phi) \equiv V_{ce}$

$$C_{cb} \Delta V_{LOGIC} / I_C = (\varepsilon A_{\text{collector}} / T_c)(\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{V_{CE} + V_{CE,\min}} \left(\frac{A_{\text{collector}}}{A_{\text{emitter}}}\right) \left(\frac{T_C}{2v_{sat}}\right)$$

Collector capacitance charging time is reduced by **thinning the collector** while increasing current.
### Scaling Laws for fast HBTs

for x 2 improvement of *all* parasitics:
- $f_t$, $f_{\text{max}}$, logic speed...
- base $\sqrt{2}$: 1 thinner
- collector 2:1 thinner
- emitter, collector junctions 4:1 narrower
- current density 4:1 higher
- emitter Ohmic 4:1 less resistive

### Challenges with Scaling:

**Collector**
- mesa HBT: collector under base Ohmics.
- Base Ohmics must be one transfer length
- sets minimum size for collector

**Emitter Ohmic**:  
hard to improve...how?

**Current Density**:  
dissipation, reliability

**Loss of breakdown**  
avanche $V_{br}$ never less than collector $E_{gap}$  
(1.12 V for Si, 1.4 V for InP)
- ....sufficient for logic, insufficient for power
digital circuit speed
Logic Speed: III-V vs. Silicon

Divider Frequency (GHz)

Benchmark: master-slave flip-flop configured as 2:1 static frequency divider

Source: M Sokolich, HRL, Rodwell, UCSB
75 GHz HBT master-slave latch connected as Static frequency divider

technology:
400 Å base, 2000 Å collector HBT
0.7 um mask (0.6 um junction) x 12 um emitters
1.5 um mask (1.4 um junction) x 14 um collectors

transistor performance:
1.8x10^5 A/cm^2 operation, 180 GHz ft, 260 GHz fmax
collector/ emitter junction area ratio: 2.7:1 (low)
Ccbl/Ic: 0.9 ps/V
Rex*I=54 mV

simulations: 95 GHz clock rate in SPICE

Vout (Volts)

Time (ps)

fin=75GHz, fout=37.5GHz

Vout (Volts)

Time (ps)

fin=69GHz, fout=34.5GHz

modulation is synthesizer 6 GHz subharmonic

~3.5 dBm input power

3.92 V, 224 mA, 0.88 W
What do we need for fast logic?

Gate Delay Determined by:

1. Depletion capacitance charging through the logic swing
   \[ \left( \frac{\Delta V_{\text{LOGIC}}}{I_C} \right) \left( C_{cb} + C_{be,\text{depletion}} \right) \]

2. Depletion capacitance charging through the base resistance
   \[ R_{bb} \left( C_{cb} + C_{be,\text{depletion}} \right) \]

3. Supplying base + collector stored charge through the base resistance
   \[ R_{bb} \left( \tau_b + \tau_c \right) \left( \frac{I_C}{\Delta V_{\text{LOGIC}}} \right) \]

The logic swing must be at least
\[ \Delta V_{\text{LOGIC}} > 6 \left( \frac{kT}{q} + R_{ex} I_c \right) \]

Neither \( f_{\tau} \) nor \( f_{\max} \) predicts digital speed

\( C_{cb} \Delta V_{\text{logic}} / I_c \) is very important

\[ \rightarrow \text{collector capacitance reduction is critical} \]
\[ \rightarrow \text{increased III-V current density is critical} \]

\( R_{ex} \) must be very low for low \( \Delta V_{\text{logic}} \) at high \( J_c \)

InP: \( R_{bb} \), \( (\tau_b + \tau_c) \), are already low, must remain so
# What HBT parameters determine logic speed?

<table>
<thead>
<tr>
<th></th>
<th>Cje</th>
<th>Ccbx</th>
<th>Ccbi</th>
<th>(τ_b+τ_c) (VΔV)</th>
<th>total</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔV/ I</td>
<td>33.5%</td>
<td>6.7%</td>
<td>27.8%</td>
<td></td>
<td>68.4%</td>
</tr>
<tr>
<td>ΔV/ I</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>12.3%</td>
</tr>
<tr>
<td>(kT/q) I</td>
<td>1.4%</td>
<td>0.1%</td>
<td>0.4%</td>
<td>0.5%</td>
<td>2.5%</td>
</tr>
<tr>
<td>Rex</td>
<td>-1.3%</td>
<td>0.1%</td>
<td>0.3%</td>
<td>0.9%</td>
<td>0.1%</td>
</tr>
<tr>
<td>Rbb</td>
<td>10.2%</td>
<td>2.8%</td>
<td>3.7%</td>
<td></td>
<td>16.7%</td>
</tr>
<tr>
<td>total</td>
<td>43.8%</td>
<td>6.8%</td>
<td>31.3%</td>
<td>17.5%</td>
<td>100.0%</td>
</tr>
</tbody>
</table>

**Sorting Delays by capacitances:**

- 44% charging $C_{je}$, 38% charging $C_{cb}$, only 18% charging $C_{diff}$ (e.g. $\tau_b + \tau_c$)

**Sorting Delays by resistances and transit times:**

- 68% from $\Delta V_{logic} / I_c$, 12% from $(\tau_b + \tau_c)$, 17% from $R_{bb}$
- $R_{ex}$ has very strong indirect effect, as $\Delta V_{logic} > 6 \cdot (kT / q + I_c R_{ex})$

**Caveats:**

- Assumes a specific UCSB InP HBT (0.7 um emitter, 1.2 um collector 2kÅ thick, 400 Å base, 1.5E5 A/cm²)
- Ignores interconnect capacitance and delay, which is very significant

---

Yoram Betser, Raja Pullela
## Logic Speed

<table>
<thead>
<tr>
<th></th>
<th>$c_{je}$</th>
<th>$c_{cbx}$</th>
<th>$c_{cbi}$</th>
<th>$\tau_f J / \Delta V_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_L / J$</td>
<td>1</td>
<td>6</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>$kT / qJ$</td>
<td>0.5</td>
<td>1</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>$\rho_e$</td>
<td>-0.25</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>$r_{bb}$</td>
<td>0.5</td>
<td>0</td>
<td>1</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Approximate delay coefficients $a_{ij}$ for an ECL master-slave flip-flop, found by hand analysis. Gate delay is of the form $T_{gate} = 1/2 f_{clock, max} = \Sigma a_{ij} r_i c_j$, where $f_{clock}$ is the maximum clock frequency. The minimum logic voltage swing is $\Delta V_{LOGIC} > 6(kT / q + J\rho_{ex})$

Caveat: ignores interconnect capacitance and delay, which is very significant
### Logic Speed: definition of terms

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$c_{je}$</td>
<td>emitter base depletion capacitance per unit emitter area</td>
</tr>
<tr>
<td>$c_{cbi}$</td>
<td>intrinsic collector base capacitance per unit emitter area</td>
</tr>
<tr>
<td>$c_{cbx}$</td>
<td>extrinsic collector base capacitance per unit emitter area</td>
</tr>
<tr>
<td>$\tau_f$</td>
<td>sum of base and collector transit times</td>
</tr>
<tr>
<td>$J$</td>
<td>emitter current per unit emitter area</td>
</tr>
<tr>
<td>$\Delta V_{LOGIC}$</td>
<td>logic voltage swing</td>
</tr>
<tr>
<td>$r_{bb}$</td>
<td>base resistance times emitter area (e.g. &quot;per - area&quot; $R_{bb}$)</td>
</tr>
<tr>
<td>$\rho_{ex}$</td>
<td>emitter resistance times emitter area (e.g. &quot;per - area&quot; $R_{ex}$)</td>
</tr>
</tbody>
</table>
**Why isn't base+collector transit time so important?**

Under Small - Signal Operation:

\[ \Delta Q_{\text{base}} = (\tau_b + \tau_c) \Delta I_C = (\tau_b + \tau_c) \frac{dI_C}{dV_{be}} \Delta V_{be} = \frac{(\tau_b + \tau_c)I_C}{kT/q} \Delta V_{be} \]

Under Large - Signal Operation:

\[ \Delta Q_{\text{base}} = (\tau_b + \tau_c)I_C = \frac{(\tau_b + \tau_c)I_{dc}}{\Delta V_{LOGIC}} \Delta V_{LOGIC} \]

Large - signal diffusion capacitance reduced by ratio of \[ \left( \frac{\Delta V_{LOGIC}}{kT/q} \right) \], which is \( \sim 10 : 1 \)

Depletion capacitances see no such reduction
roadmap
# Technology Roadmaps for 40 / 80 / 160 Gb/s

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Transferred-Substrate HBT</th>
<th>Mesa HBT Generation 1</th>
<th>Mesa HBT Generation 2</th>
<th>Mesa HBT Generation 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Predicted MS-DFF speed (no interconnects)</td>
<td>93 GHz</td>
<td>62 GHz</td>
<td>125 GHz</td>
<td>237 GHz</td>
</tr>
<tr>
<td>Observed speed</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Emitter Junction Width</td>
<td>0.6 μm</td>
<td>1 μm</td>
<td>0.8 μm</td>
<td>0.2 μm</td>
</tr>
<tr>
<td>Parasitic Resistivity</td>
<td>30 Ω-μm²</td>
<td>50 Ω-μm²</td>
<td>20 Ω-μm²</td>
<td>5 Ω-μm²</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>400 Å</td>
<td>400 Å</td>
<td>300 Å</td>
<td>250 Å</td>
</tr>
<tr>
<td>Doping</td>
<td>4×10¹⁹/cm²</td>
<td>5×10¹⁹/cm²</td>
<td>5×10¹⁹/cm²</td>
<td>5×10¹⁹/cm²</td>
</tr>
<tr>
<td>Sheet resistance</td>
<td>750 Ω</td>
<td>750 Ω</td>
<td>700 Ω</td>
<td>700 Ω</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>150 Ω-μm²</td>
<td>150 Ω-μm²</td>
<td>20 Ω-μm²</td>
<td>10 Ω-μm²</td>
</tr>
<tr>
<td>Collector Width</td>
<td>1.5 μm</td>
<td>3 μm</td>
<td>1.6 μm</td>
<td>0.4 μm</td>
</tr>
<tr>
<td>Collector Thickness</td>
<td>2000 Å</td>
<td>3000 Å</td>
<td>2000 Å</td>
<td>1000 Å</td>
</tr>
<tr>
<td>Current Density</td>
<td>1.8 mA/μm²</td>
<td>1 mA/μm²</td>
<td>2.3 mA/μm²</td>
<td>9.3 mA/μm²</td>
</tr>
<tr>
<td>( \frac{A_{\text{collector}}}{A_{\text{emitter}}} )</td>
<td>2.5</td>
<td>4.55</td>
<td>2.6</td>
<td>2.6</td>
</tr>
<tr>
<td>( f_r )</td>
<td>180</td>
<td>170</td>
<td>260</td>
<td>500</td>
</tr>
<tr>
<td>( f_{\text{max}} )</td>
<td>220</td>
<td>170</td>
<td>440</td>
<td>1000</td>
</tr>
<tr>
<td>( C'_{cb} / I_c )</td>
<td>0.8 ps/V</td>
<td>1.7 ps/V</td>
<td>0.63 ps/V</td>
<td>0.31 ps/V</td>
</tr>
<tr>
<td>( C'<em>{cb\Delta V</em>{\text{logic}}}/I_c )</td>
<td>0.24 ps</td>
<td>0.5 ps</td>
<td>0.19 ps</td>
<td>0.093 ps</td>
</tr>
<tr>
<td>( R_{bb}/(\Delta V_{\text{logic}}/I_c) )</td>
<td>0.9</td>
<td>0.8</td>
<td>0.65</td>
<td>0.52</td>
</tr>
<tr>
<td>( C'<em>{je}/(\Delta V</em>{\text{logic}}/I_C) )</td>
<td>0.9 ps</td>
<td>1.7 ps</td>
<td>0.72 ps</td>
<td>0.18 ps</td>
</tr>
<tr>
<td>( R_{ex}/(\Delta V_{\text{logic}}/I_c) )</td>
<td>0.12</td>
<td>0.1</td>
<td>0.15</td>
<td>0.15</td>
</tr>
</tbody>
</table>
80 Gb/s technology node:
Change from 40 Gb/s does not fully follow scaling laws. Why?
Lithographic scaling eased by carbon base doping.
Current density scaling eased by reduced excess collector area.

160 Gb/s technology node:
Direct application of scaling laws.
Aggressive current density and lithographic scaling required.
If further improved base contact resistance $\rightarrow$ relax lithographic scaling
Further reduce $A_{\text{collector}} / A_{\text{emitter}}$ ratio $\rightarrow$ relax current density scaling
...note that $A_{\text{collector}} / A_{\text{emitter}} < 2.5$ looks hard at deep submicron.
device structures
InP mesa HBT

- Collector
- Emitter
- BCB
Narrow-Mesa HBTs: high $f_\tau$ & $f_{\text{max}}$ if high base doping

0.5 $\mu$m emitter,
0.25 $\mu$m base contacts
Low Ccb HBT structures

**transferred-substrate**
- Extremely high demonstrated fmax
- 75 GHz (record) static frequency dividers
- Too low yield for manufacturing (?)

**undercut-collector**
- Pursued by several research groups
- Also has uncertain yield at submicron geometries

**Narrow-mesa with ~1E20 carbon-doped base**
- The conservative device structure
- Yet, I assert that even this device is not viable of mass manufacturing if > 3000 transistors per IC are sought
yield and fabrication
**InP HBT limits to yield: non-planar process**

Emitter contact:
- Emitter
- Base
- Sub collector
- S.I. substrate

Etch to base:
- Base
- Sub collector
- S.I. substrate

Liftoff base metal:
- Emitter contact
- Base contact
- Base
- Sub collector
- S.I. substrate

Emitter planarization, interconnects:
- Base
- Sub collector
- S.I. substrate

Failure modes:
- Liftoff failure: emitter-base short-circuit
- Excessive emitter undercut
- Planarization failure: interconnect breaks

Yield degrades as emitters are scaled to submicron dimensions.
<table>
<thead>
<tr>
<th>Material</th>
<th>Front and side views</th>
<th>Smaller emitters → lower yield. Need better fabrication process</th>
</tr>
</thead>
<tbody>
<tr>
<td>InP</td>
<td>![InP image]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.7 um</td>
<td></td>
</tr>
<tr>
<td>InAlAs</td>
<td>![InAlAs image]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>~0.4 um junction</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Metal</th>
<th>Junction</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 um</td>
<td>~0.4 um</td>
</tr>
<tr>
<td>0.6 um</td>
<td>~0.4 um</td>
</tr>
</tbody>
</table>
**InP vs. SiGe**

**Digital**
InP has slightly higher speed, much less power
InP can't meet integration scales of many complex fast ICs

**Analog:**
Combined InP speed and breakdown are key advantages

mm-wave wireless / RF (60 GHz, etc)
No significant market yet
InP HBT could be strong contender (fast and cheap)

*Fast, high-yield InP HBT IC processes are critically needed*
# InP vs. SiGe

**III-V literature, III-V research community:**
Large inherent advantages in transport parameters over Si
Research focused on transport physics, poorly tied to circuit design
→ **devices not well-tuned for circuits, poor parasitic reduction**
→ **university-like fabrication, low yield, low scales of integration**

**Silicon research community**
Focused on **SCALING**, closely tied to **circuit** design, focus on **YIELD**
Strong **extrinsic parasitic reduction**
Result: very good SiGe HBT digital circuit speed, large fast ICs

InP HBT has fundamental advantages which will allow it to scale beyond SiGe HBT scaling limits, but must address:

**yield**: Silicon-like planar implanted / regrowth processes
**speed**: device scaling informed by understanding of circuit design
**InP vs. Si/SiGe HBTs: materials vs. scaling advantages**

**Good:**
- Narrow emitter: 0.18 um
- High current density: 10 mA/um²
- Large emitter contact: low resistance
- Polysilicon base contact: low resistance
- SiO₂ trenches: small collector capacitance
- Planar device: high yield

**Bad:**
- High base sheet resistance,
- Low electron velocity, low breakdown limits scaling.

**Equal speed at 5x smaller scaling.**
**Loss of breakdown may soon slow scaling**

**Good:**
- 20x lower base sheet resistance,
- 5x higher electron velocity,
- 4x higher breakdown-at same ft.

**Bad:**
- Presently only scaled to ~ 1 um
- Archaic mesa fabrication process:
  - large emitters, poor emitter contact:
  - low current density: 2 mA/um²
  - high collector capacitance
  - nonplanar device: low yield
SiGe HBTs high yield: **regrown emitter, planar process, VLSI interconnects**

0.2 um emitters are **regrown**, not etched

Transistor is planar, interconnects are standard for VLSI (W/ Al with SiO₂)

InAlAs/InGaAs/InP DHBT with polycrystalline extrinsic emitter regrowth.
thermal resistance and thermal runaway
Thermal resistance and effect of subcollector

\[ \theta_{JA} \approx \frac{T_{InP,c}}{2 K_{InP} W_E L_E} + \frac{T_{InGaAs}}{K_{InGaAs} W_B L_B} + \frac{1}{\pi K_{InP} L_B} \ln\left( \frac{L_B}{W_B} \right) + \frac{1}{\pi K_{InP} L_B} \]

**Approximation:**
InGaAs dominates thermal resistance → heat flows through InGaAs in area equal base mesa (excluding pad)

\( \Delta T, \text{2000 Å InGaAs} \)

\( \Delta T, \text{200 Å InGaAs} \)

\( W_B \)

\( L_B \)

\( \text{Emitter} \)

\( \text{Collector} \)

\( \text{InGaAs subcollector} \)

\( W_E = 0.5 \, \mu m, \ L_E = 3 \, \mu m, \ W_B = 0.7 \, \mu m, \ L_B = 3.25 \, \mu m, \)

\( J_E = 4 \, mA/\mu m^2, \ V_{CE} = 1.2 \, V \)

\( K_{InGaAs} = 5 \, W/k \cdot m \quad K_{InP} = 68 \, W/k \cdot m \)

Poor performance observed in multi-finger DHBT

8 finger common emitter DHBT
Emitter size: 16 µm x 1 µm
Ballast resistor (design): 9 Ohm/finger

Current hogging observed
fmax also low due to high base feed resistance

Restrictions on DHBT sizing: distributed base feed resistance

Self-aligned base contact thickness = 0.08 \( \mu m \)
Leads to feed sheet resistance:
\( \rho = 0.3 \ \Omega/\square \)
restricts emitter length to \( \sim 15 \ \mu m \)

Excess Rbb, hence reduced \( f_{max} \)
(big HBT has big \( C_{cb} \), small \( R_{bb} \), hence even small excess \( R_{bb} \) reduces \( f_{max} \))
DHBT thermal stability: multiple emitter fingers

Assume initial temperature difference $\delta T$ between 2 fingers

$$\frac{dV_{be}}{dT} = -1.1 \text{ mV/K at constant } I_c$$

$$\delta T \Rightarrow \delta V_{be} = \frac{dV_{be}}{dT} \delta T \Rightarrow \delta I_c = \frac{1}{R_{ex} + R_{\text{ballast}} + kT/qI_E} \delta V_{be}$$

$$\Rightarrow \delta P = V_{CE} \delta I_c \Rightarrow \delta T = \theta_{JA} \delta P$$

Unstable unless

$$K_{\text{thermal stability}} = \left| \frac{dV_{be}}{dT} \right| \frac{V_{CE} \theta_{JA}}{R_{ex} + R_{\text{ballast}} + kT/qI_E} < 1$$

With long emitter finger, current-crowding can occur within finger

- Long finger: temperature can vary along length of emitter finger
  loss of strong thermal coupling
- Temperature gradients along finger results in nonuniform current distribution
  center of stripe gets hotter → carries more current → gets hotter → …
  Premature Kirk-effect-induced collapse in $f_t$. 
Current hogging observation: multi-finger DHBT

Measuring DHBT thermal resistance

\[ \delta V_{be} \bigg|_{\text{fixed } I_c} = \frac{dV_{be}}{dT} \frac{dT}{dP} \frac{dP}{dV_{CE}} \delta V_{CE} = (-1.1 \text{ mV/K}) \cdot \theta_{JA} I_C \delta V_{CE} \]

\[ \Rightarrow \theta_{JA} = \left. \frac{dV_{be}}{dV_{CE}} \right|_{\text{fixed } I_c} \times \frac{1}{I_C (-1.1 \text{ mV/K})} \]

Large current high breakdown voltage broadband InP DHBT

Objectives: $f_{\text{max}}>300$ GHz, $BV_{CEO}>6$ V, $J_{\text{max}}\approx 1\times 10^5$ A/cm$^2$

Approach: transferred-substrate multi-finger InP DHBTs, HBT thermal analysis

Simulations: large signal HBT spice model

Accomplishments:
$f_{\text{max}}>330$ GHz, $BV_{CE}>7$ V, $J_{\text{max}}\approx 1\times 10^5$ A/cm$^2$

128 μm$^2$ common base DHBT
On-wafer characterization of HBTs
accurate and otherwise
Ultra-high $f_{\text{max}}$ Submicron HBTs

- Electron beam lithography used to define submicron emitters and collectors
- Minimum feature sizes
  - $\Rightarrow 0.2 \, \mu\text{m}$ emitter stripe widths
  - $\Rightarrow 0.3 \, \mu\text{m}$ collector stripe widths
- Improved collector-to-emitter alignment using local alignment marks
- Aggressive scaling of transistor dimensions predicts progressive improvement of $f_{\text{max}}$

As we scale HBT to $<0.4$ um, $f_{\text{max}}$ keeps increasing, measurements become very difficult.
140-220 GHz On-Wafer Network Analysis

- HP8510C VNA, *Oleson Microwave Lab* mm-wave Extenders

- *GGB Industries* coplanar wafer probes

- Connection via short length of WR-5 waveguide

- Internal bias Tee’s in probes for biasing active devices

- 75-110 GHz set-up is similar

UCSB 140-220 GHz VNA Measurement Set-up
Accurate Transistor Measurements Are Not Easy

- Submicron HBTs have very low $C_{cb}$ ($< 3 \, \text{fF}$)
- Characterization requires accurate measure of very small $S_{12}$
- Standard 12-term VNA calibrations do not correct $S_{12}$ background error due to probe-to-probe coupling

Solution
Embed transistors in sufficient length of transmission line to reduce coupling
Place calibration reference planes at transistor terminals

Line-Reflect-Line Calibration
Standards easily realized on-wafer
Does not require accurate characterization of reflect standards
Characteristics of Line Standards are well controlled in transferred-substrate microstrip wiring environment

Corrupted 75-110 GHz measurements due to excessive probe-to-probe coupling
Can we trust the calibration?

75-110 GHz calibration looks **Great**

- **S11 of short**
- **S11 of through**
- **S11 of open**

**Probe-Probe coupling is better than -45 dB**

140-220 GHz calibration looks OK

- **S11 of open**
  - About -40 dB
- **S11 of through**
  - About -40 dB

**S11 of through**

**S21 of through line is off by less than 0.05 dB**
140-220 GHz Calibration Verification: Measurement of Thru Line after Calibration

1. **Magnitude S21 (dB)**
   - Graph showing the magnitude of S21 in dB across frequencies.

2. **Phase S21 (degrees)**
   - Graph showing the phase of S21 in degrees across frequencies.

3. **S11, S22 (dB)**
   - Graphs showing the S11 and S22 values in dB across frequencies.
transistor
results
Ultra-high $f_{\text{max}}$ Transferred-Substrate HBTs

- Substrate transfer provides access to both sides of device epitaxy
- Permits simultaneous scaling of emitter and collector widths
- Maximum frequency of oscillation
  $$f_{\text{max}} \approx \sqrt{f_v / 8\pi R_{bb} C_{cb}}$$
- Sub-micron scaling of emitter and collector widths has resulted in record values of extrapolated $f_{\text{max}}$
- Extrapolation begins where measurements end
- New 140-220 GHz Vector Network Analyzer (VNA) extends device measurement range

**Gains, dB vs. Frequency, GHz**

- Mason's gain, $U$
- $f_{\tau}$ = 204 GHz
- $f_{\text{max}} = 1.1 \text{ THz} \ ?$
- 3000 Å collector
- 400 Å base with 52 meV grading
- AlInAs / GaInAs / GaInAs HBT

Emitter, 0.4 x 6 µm²
Collector, 0.7 x 6 µm²
$I_c = 6 \text{ mA}, V_{ce} = 1.2 \text{ V}$

Michelle Lee
Submicron InAlAs/InGaAs HBTs: Unbounded Unilateral power gain 45-170 GHz

- Collector: 3000 Å thickness, $10^{16}$/cm$^3$ doping
- Collector pulse doping: 50 Å thickness, $10^{17}$/cm$^3$ doping, 250 Å from base

$V_{ce} = 1.1$ V, $I_c = 5$ mA

- 0.3 µm x 18 µm emitter,
- 0.7 µm x 18.6 µm collector,
Negative Unilateral Power Gain ???

Can U be Negative?

YES, if denominator is negative

This may occur for device with a negative output conductance \( G_{22} \) or some positive feedback \( G_{12} \)

What Does Negative U Mean?

Device with negative U will have infinite Unilateral Power Gain with the addition of a proper source or load impedance

AFTER Unilateralization

- Network would have negative output resistance
- Can support one-port oscillation
- Can provide infinite two-port power gain

\[
U = \frac{|Y_{21} - Y_{12}|^2}{4(G_{11}G_{22} - G_{21}G_{12})}
\]

Select \( G_L \) such that denominator is zero:
\[
U = \infty
\]

Simple Hybrid- \( \pi \) HBT model will NOT show negative U
DC-200 GHz parameters of 0.3 µm Emitter / 0.7 µm Collector HBTs:

No evidence whatsoever of the postulated base pushout phenomenon of Jäckel et al (this theory also uses an erroneous hole mobility, error due to calculus derivatives chain rule error)

Miguel Urteaga
transferred-substrate DHBTs

\[ f_{\text{max}} = 425 \text{ GHz}, \quad f_t = 139 \text{ GHz} \]

0.4 µm x 8 µm emitter
1.2 µm x 8.75 µm collector
I_c = 4.5 mA, V_{ce} = 1.9 V

\[ V_{ce(\text{sat})} \sim 1 \text{ V at 1.8 mA/µm}^2 \]

\[ BV_{CEO} = 8 \text{ V at } J_E = 0.4 \text{ mA/µm}^2 \]

much wider bandwidth devices coming soon (we hope...)
We have obtained high $f_t$ and very high $f_{max}$ in mesa DHBTs with C-doped InGaAs bases.

Devices have very narrow base mesas and extremely low base contact resistivity.

Unlike transferred-substrate HBTs, which have very low $C_{cbx}$, these devices have significant extrinsic collector-base junction areas.

→ further effort needed in excess Ccb reduction for >100 GHz digital ICs.

Results to be presented soon.
Comparing High-$f_{\text{max}}$ HBTs

**Transferred-Substrate HBT:**

- **Low Rbb**

0.3 um x 18 um emitter, 0.7 um x 19 um collector. 130 GHz ft, $f_{\text{max}}$ very high

- **Low Ccb**

1-45, 75-110, 140-220 GHz

**Transferred-Substrate HBT:**

- **Very low Ccb**

0.4 um x 6 um emitter, 0.7 um x 6.4 um collector. 130 GHz ft, $f_{\text{max}}$ very high

- **Very low Ccb**

0.4 um x 6 um emitter, 0.7 um x 6.4 um collector. 130 GHz ft, $f_{\text{max}}$ very high

**Good (not record) mesa HBT**

- **High Rbb**

0.5 um x 7 um emitter, 2.7 um x 12 um collector. 200 GHz ft, 200 GHz $f_{\text{max}}$

- **High Ccb**

**Fast C-doped-base mesa HBT**

- **Low Rbb**

0.5 um x 7 um emitter, ~1.6 um x 12 um collector. >250 GHz ft, high $f_{\text{max}}$

- **High Ccb**

PK Sundararajan

Mattias Dahlstrom
**InP/InGaAs/InP Metamorphic DHBT on GaAs substrate**

**Growth:**
- 400 Å base, 2000 Å collector
- GaAs substrate
- InP metamorphic buffer layer
  (high thermal conductivity)

**Processing**
- conventional mesa HBT
- narrow 2 um base mesa, 0.4 um emitter

**Results**
- 207 GHz \(f_t\), 140 GHz \(f_{max}\),
- >6 Volt BVCEO, \(\beta=76\)
IC results
75 GHz HBT master-slave latch connected as Static frequency divider

technology:
- 400 Å base, 2000 Å collector HBT
- 0.7 um mask (0.6 um junction) x 12 um emitters
- 1.5 um mask (1.4 um junction) x 14 um collectors
- $1.8 \times 10^5$ A/cm² operation, 180 GHz ft, 260 GHz fmax

simulations: 95 GHz clock rate in SPICE

test data to date:
- tested, works over full 26-40 and 50-75 GHz bands

$3.92 \text{ V, } 224 \text{ mA, } 0.88 \text{ W}$

$\text{modulation is synthesizer } 6 \text{ GHz subharmonic}$
18 GHz $\Sigma - \Delta$ ADC

**Design**
- comparator is 75 GHz flip flop
- DC bias provided through 1 kΩ resistors
- Integration obtained with 3 pF capacitors
- RTZ gated DAC

**Integrated Circuit**
- 150 HBTs, 1.2 x 1.5 mm, 1.5 W
High Speed Amplifiers

18 dB, DC--50+ GHz

>397 GHz
gain x bandwidth from 2 HBTs

8.2 dB, DC-80 GHz

Gain x bandwidth from 2 HBTs
AFOSR

HBT distributed amplifier

11 dB, DC-87 GHz

PK Sundararajan

TWA with internal ft-doubler cells
175 GHz Single-Stage Amplifier

6.3 dB gain at 175 GHz
40 mW, W-band InP DHBT power amplifiers

**Objectives:** W band, $P_{1\text{dB}}>9$ dBm, $P_{\text{sat}}>12$ dBm

**Approach:** transferred-substrate InP DHBTs, microwave amplifier design

**Simulations:** S-parameter and harmonic simulation in ADS

**Accomplishments:**
- $f_0=85$ GHz, $BW_{3\text{dB}}=28$ GHz,
- $G_T=8.5$ dB, $P_{1\text{dB}}=14.5$ dBm, $P_{\text{sat}}=16$ dBm

**Common base PA**

- $0.5\text{mm} \times 0.4\text{mm}$, $A_E=128 \mu\text{m}^2$

**Graphs:**
- S11, S21, S22 vs. frequency, GHz
- $P_{\text{out}},$ $G_T$ vs. $P_{\text{in}},$ dBm

**UCSB**

Yun Wei