Ultra Low Resistance Ohmic Contacts to InGaAs/InP

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Outline

• Motivation

• Previous Work

• Approach

• Results

• Conclusion
Device bandwidth scaling laws

\[
\frac{1}{2\pi f_\tau} = \tau_{\text{base}} + \tau_{\text{collector}} + C_{je} \frac{kT}{qI_E} + C_{bc} \frac{kT}{qI_E} + R_{ex} C_{bc} + R_{coll} C_{bc}
\]

\[
f_{\max} = \sqrt{\frac{f_\tau}{8 \cdot \pi \cdot (R_{bb} \cdot C_{cb})_{\text{eff}}}}
\]

Goal: Double transistor bandwidth
- Reduce transit delay
- Reduce RC delay

Vertical Scaling

Increased Capacitance
- Lateral Scaling
- Keep R constant
- Reduce \( \rho_c \)

\[
R_{ex} = \frac{\rho_c}{A}
\]

\( \rho_c \) has to scale as inverse square of lateral scaling

Device bandwidth scaling roadmap – THz transistor

Emitter Resistance key to THz transistor

Emitter resistance effectively contributes > 50 % in bipolar logic gate delay*

Contact resistance serious barrier to THz technology

\[ 2 \, \text{Ω} \cdot \mu\text{m}^2 \] contact resistivity required for simultaneous THz \( f_t \) and \( f_{\text{max}} \)

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Device bandwidth scaling-FETs

Source contact resistance must scale to the inverse square of device scaling. Source resistance reduces $g_m$ and $I_d$

A 22 nm III-V MOSFET with 5 mA/μm $I_d$

15 $\Omega \cdot \mu m$ source resistance will reduce $I_d$ by 10%

With 50 nm contact width this will require $\rho_c$ of $1 \Omega \cdot \mu m^2$

Low source resistance means better NF in FETs*

$$NF_{\text{min}} \approx 1 + \sqrt{g_{mi} (R_s + R_g + R_i) \Gamma} \cdot \left( \frac{f}{f_{\tau}} \right)$$

*T Takahashi, IPRM 07

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Conventional Contacts

- Conventional contacts
  - complex metallization and annealing schemes
  - Surface oxides, contaminants
  - Fermi level pinning
  - metal-semiconductor reaction improves resistance

$5 \, \Omega \cdot \mu m^2 \, (5 \cdot 10^{-8} \, \Omega \cdot \mu m^2)$ obtained on InGaAs, used on the latest HBT results

Further improvement difficult using this technique

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S.E. Mohney, PSU
M. Urteaga, Teledyne

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**In-situ ErAs-InGaAs Contacts**

- Epitaxial ErAs-InGaAs contact
  - Epitaxially formed, no surface defects, no fermi level pinning
  - *In-situ*, no surface oxides
  - thermodynamically stable
  - ErAs/InAs fermi level should be above conduction band

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3. S. R. Bank, NAMBE, 2006

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Approximate Schottky barrier potential

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S. R. Bank, NAMBE, 2006

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**In-situ and ex-situ Contacts**

- **In-situ Mo Contact**
  - *In-situ* deposition no oxide at metal-semiconductor interface
  - Fermi level pins inside conduction band of InAs

- **Ex-situ contacts**
  - InGaAs surface oxidized by UV Ozone treatment
  - Strong NH4OH treatment before contact metal deposition


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MBE growth and TLM fabrication

• MBE Growth
  – InGaAs:Si grown at 450 C
  – 3.5 E 19 active Si measured by Hall
  – ErAs grown at 450 C, 0.2 ML/s
  – Mo deposited in an electron beam evaporator connected to MBE under UHV
  – Mo cap on ErAs to prevent oxidation
  – Layer thickness chosen so as to satisfy 1-D condition in TLM

• TLM Fabrication
  – Samples processed into TLM structures by photolithography and liftoff
  – Mo and TiW dry etched in SF$_6$/Ar with Ni as etch mask, isolated by wet etch
  – Separate probe pads from contacts to minimize parasitic metal resistance
Contact Resistance

- Resistance measured by 4155 C parameter analyzer
- Pad spacing verified by SEM image
- Smallest gap, contact resistance 60% of total resistance
- 15-18 Ohm sheet resistance for all three contacts

<table>
<thead>
<tr>
<th>Contact</th>
<th>$\rho_c (\Omega \cdot \mu m^2)$</th>
<th>$L_t$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ErAs/InAs</td>
<td>1.5</td>
<td>300</td>
</tr>
<tr>
<td>Mo/InAs</td>
<td>0.5</td>
<td>175</td>
</tr>
<tr>
<td>TiW/InGaAs</td>
<td>0.7</td>
<td>190</td>
</tr>
</tbody>
</table>

\[ 1 \Omega \cdot \mu m^2 = 1 \cdot 10^{-8} \Omega \cdot cm^{-2} \]
Ex-situ Contacts

- Ex-situ contact depends on the concentration of NH$_4$OH$^*$

$\rho_c$ (Ω·µm$^2$)

NH$_4$OH Normality

* A.M. Crook, submitted to APL
Thermal Stability

- Contacts annealed under N₂ flow at different temperatures
- Contacts stays Ohmic after anneal
- In-situ Mo/InAs, ex-situ TiW/InGaAs contact resistivity < 1 Ω-μm² after anneal
- ErAs/InAs contact resistivity increases with anneal
- The increase could be due to lateral oxidation of ErAs
Thermal Stability

- SIMS depth profiling shows that Mo and TiW act as diffusion barrier to Ti and Au

SIMS profile of contacts annealed at 400 C
Error Analysis

• 1-D Approximation
  • Large $L_t/L$,
  • 1-D case overestimates $\rho_c$

• Overlap resistance
  • Wide contact width reduces overlap resistance.

• 1-D case, Overlap resistance overestimates extracted $\rho_c$

• Errors
  • Pad spacing, minimized by SEM inspection
  • Resistance, minimized by using 4155C parameter analyzer
    • $\delta \rho_c/\rho_c$ is 60% at 1 Ω-μm², 75% at 0.5 Ω-μm²

*H. Ueng, IEEE TED, 2001
Integration into Device Processing

• HBT emitter contact*

<table>
<thead>
<tr>
<th>Ti/W or Mo</th>
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<th>Ti/W</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>InGaAs/InP emitter</em></td>
<td><em>InGaAs Base</em></td>
<td><em>InGaAs Base</em></td>
</tr>
<tr>
<td><em>InP Collector</em></td>
<td><em>InP Collector</em></td>
<td><em>Sub-Collector</em></td>
</tr>
<tr>
<td><em>Sub-Collector</em></td>
<td><em>Sub-Collector</em></td>
<td><em>SI substrate</em></td>
</tr>
<tr>
<td><em>SI substrate</em></td>
<td><em>SI substrate</em></td>
<td><em>Dry + Wet etch Emitter</em></td>
</tr>
</tbody>
</table>

Blanket metal deposition

Dry etch Emitter metal

*E. Lind, Late News, DRC 2007

• Source Contact in FETs

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Conclusion

• Ultra Low Ohmic contacts to InGaAs/InP with $\rho_c < 1 \ \Omega \cdot \mu m^2$

• Contacts realized by both in-situ and ex-situ

• In-situ Mo/InAs and ex-situ TiW/InGaAs $\rho_c < 1 \ \Omega \cdot \mu m^2$ even after 500 C anneal

• In-situ ErAs/InAs contacts $\rho_c = 1.5 \ \Omega \cdot \mu m^2$, increases gradually with anneal

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