Planarization and Regrowth of Self-Aligned Ohmic Contacts on InGaAs

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Motivation: Can InGaAs MOSFETs beat Si?
  - Contact resistance is key: \( R_c \sim 1 / f^2 \)

Planarization & Etchback — Self-aligned

Regrown Low Resistance Contacts and MEE

InGaP Etch Stop Layer

Conclusions
In Order to Beat Silicon...

Target... | Strategy...
--- | ---
$R_{sd} = 180 \, \Omega \cdot \mu m$ | $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel
$I_{ds} = 6 \, \text{mA/}\mu \text{m} \ & \text{low gate leakage}$ | High gate barrier: MOSFET
$L_g = 22 \, \text{nm} \, \text{low SD leakage}$ | High back barrier: AlGaAs
$R_c = 1 \, \Omega \cdot \mu m^2 \ (10^{-8} \, \Omega \cdot \text{cm}^2)$ | Regrow S/D epitaxially.*
$R_{access} = 10 \, \Omega \cdot \mu m$ | Backfill channel recess etch.*

*RMajor challenges for MBE.

Source: Rodwell IPRM 2008
Surface Cleaning for Regrowth

- Encapsulate all gate metals
- Surface clean:
  - Recess etch
  - UV ozone 30min
  - 1:10 HCl:H₂O for 1 min, DI rinse
  - UHV bake 200°C
  - H clean or thermally desorb oxide
- No extended defects, low contact resistance: $1.3 \, \Omega \cdot \mu m^2$

![HRTEM](image1)

InGaAs n+ blanket regrowth

Interface

InGaAs n+

5nm

HAADF-STEM

Interface

2 nm

Oxide

Metal

SiO₂

Channel

TLM Measurement

$R_c = 1.3 \, \Omega \cdot \mu m^2$

Resistance ($\Omega$) vs. Gap ($\mu m$)

T=100µm n-3.6e19 cm⁻³
W=25µm

MBE 2008 Conference
Planarization & Etchback

- Goal: self-aligned, selective area contacts
Planarization & Etchback

- Goal: self-aligned, selective area contacts

1. Spin on thick polymer

![Diagram showing polymer spin process with layers of SiO2, Metal, Oxide, and Channel.

2. O2 Ash or Developer

3. Mo & InGaAs Etch

4. Strip resist

• Goal: self-aligned, selective area contacts
Planarization & Etchback

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**Planarization & Etchback**

- **Goal:** self-aligned, selective area contacts

1. Spin on thick polymer

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**Notes:**
- Polymer
- Regrowth
- Channel
- SiO2
- Metal
- Oxide
- Source
- Drain
Choice of Polymers

PMGI / MIF developer

BCB / CF4+O2

SPR510 / O2 plasma

- Easy to process
- Withstands wet & dry etches
- Smooth & uniform...

Spin: 4kRPM 30s. Bake: 90°C 1min, 110°C 1min.
Low Power Plasma Gives Smooth Etchback

- Etchback in **high energy** $\text{O}_2$ plasma:
  - Extreme roughness (micromasking)
  - Scum

- Etchback in **low energy** $\text{O}_2$ plasma (ICP) or UV ozone:
  - Clean, smooth surfaces, no scum
Planarization: Repeatable and Easy

• Thickness by naked eye
  • Purple/Blue – 300nm
  • Yellow – 200nm
  • Light Blue – 100nm
  • Burnt/Black – <70nm

• High yield esp. for <1μm
MBE Regrowth: Bad at any Temperature?

- Conditions: 0.5 µm/hr, V/III=35
- Low growth temperature (<400°C):
  - Smooth in far field
  - Gap near gate (shadowing)
  - No contact to channel!
MBE Regrowth: Bad at any Temperature?

- Conditions: 0.5 μm/hr, V/III=35
- Low growth temperature (<400°C):
  - Smooth in far field
  - Gap near gate (shadowing)
  - No contact to channel!

- High growth temperature (>490°C):
  - Selective/preferential epi on InGaAs
  - No gaps near gate
  - Rough far field
  - High resistance

Regrowth: 50nm InGaAs:Si, 5nm InAs:Si. Si=8E19/cm³, 20nm Mo.
Gap-free Regrowth by MEE

Migration-Enhanced Epitaxy (MEE) conditions:

490-550°C (pyrometer)
As flux constant ~ $1 \times 10^{-6}$ Torr: V/III~3, not interrupted.
0.5nm InGaAs:Si pulses (3.7 sec), 10-15 sec As soak
RHEED: 4x2 ==> 1x2 ==> 4x2 with each pulse.

- No gaps
- Smooth surfaces.

- High Si activation ($4 \times 10^{19} \text{ cm}^{-3}$).
- Quasi-selective: no growth on sidewalls
Rough Regrowth on Thin InP Etch Stop Layer

- Conversion of 2-4nm InP to InAs
- Strain relaxation

![Diagram showing conversion and strain relaxation in InP and InAs layers with InAlAs barrier and InGaAs.]
Rough Regrowth on Thin InP Etch Stop Layer

- Conversion of 2-4nm InP to InAs
- Strain relaxation

**InP regrowth RHEED**

**InP regrowth SEM**

- Acc.V: 5.00 kV, Spot Mag.: 3.0, Det. WD: 80000x, Exp.: 5.0, 1
- SEM: U. Singisetti

**InAlAs barrier**

**InP etch stop (2-4 nm)**

**InGaAs**

**InAs**

**InAs**

**InGaAs**

**InAlAs barrier**
Regrowth on InGaP

- Replace InP with InGaP
- Converts to InGaAs (good!)
- Strain compensation
Summary

• Surface clean before regrowth:
  – UV ozone, 10% HCl, then H clean or thermal desorb
  – Lowest resistance regrown contacts: \( R_c = 1.3 \ \Omega \cdot \mu \text{m}^2 \) 
    \((1.3 \times 10^{-8} \ \Omega \cdot \text{cm}^2)\)

• Planarization by photoresist: simple & repeatable
  – No lithography needed
  – MBE + Planarization = Self-Aligned Regrowth

• Gap-free regrowth \((n=4 \times 10^{19} \ \text{cm}^{-3})\) by MEE above 490°C

• InGaP etch stop prevents relaxation before regrowth
Acknowledgements

- Chris Palmstrøm and Erdem Arkun (now at UCSB)
- IBM Yorktown: Yanning Sun, Edward Kiewra, Devendra Sadana
- SRC
Additional Slides
Transmission Line Method

Length (L)

Metal contact

Conducting layer

Metal contact

\[ R(L) = \left( \frac{R_{SH}}{W} \right) \left( L + 2L_t \right) \]

\[ R(0) = 2R_c = 2L_t \frac{R_{SH}}{W} \]

\[ r_c = R_c A_c \quad \text{or} \quad r_c = R_{SH} L_t^2 \]

Slide courtesy Adam Crook, 2007
Transmission Line Method

Resistance measurements

4-Point Probe

TLM Measurement

Image courtesy Adam Crook, 2007

\[ R_c = 1.3 \times 10^{-8} \, \Omega \cdot \text{cm}^2 \]
Contact Resistance: In-situ Mo Contacts

- InGaAs-InGaAs regrown interface resistance < 1 Ω -μm² on unprocessed surfaces.
- Regrown interfaces comparable with 0.5 Ω-μm² from continuous epitaxy.

Step 1
- In-situ Mo
- n+ Regrowth
- n+ InGaAs
- SI InP

Step 2
- In-situ Mo
- n+ Regrowth
- n+ InGaAs
- SI InP

TLMs by U. Singisetti
MOSFET Process Flow Detail

non-selective area
S/D regrowth

selective area
S/D regrowth
Process Flow: Gate Deposition

High-k first on pristine channel.

Tall gate stack.

Litho.

Selective etches to channel.

<table>
<thead>
<tr>
<th>NID InGaAs Channel</th>
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<tbody>
<tr>
<td>InP etch stop</td>
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<tr>
<td>InAlAs barrier</td>
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<tr>
<td>InP substrate</td>
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</tbody>
</table>
Process Flow: Gate Deposition

- High-k first on pristine channel.
- Tall gate stack.
- Litho.
- Selective etches to channel.

<table>
<thead>
<tr>
<th>Cr</th>
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<tbody>
<tr>
<td>SiO₂</td>
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| Metals |
| εᵣ |
| NID InGaAs Channel |
| InP etch stop |
| InAlAs barrier |
| InP substrate |
Process Flow: Gate Deposition

High-k first on pristine channel.

Tall gate stack.

Litho.

Selective etches to channel.

Critical etch process:
Stop on channel with no damage.
Gate Stack: Multiple Layers & Selective Etches

Key: stop etch before reaching dielectric, then gentle low-power etch to stop on dielectric

- SF$_6$ / Ar etch
- Cr
- SiO$_2$
- Cr or Hf
- W/Mo gate metal
- gate dielectric
- InGaAs well
- InP well
- barrier
- SI substrate

Damage free InGaAs Channel after dry etch

FIB Cross-section
Process Flow: Sidewalls & Recess Etch

**SiN\(_x\) or SiO\(_2\) sidewalls**
- Encapsulate gate metals

**Controlled recess etch**
- Slow facet planes
- Not needed for depletion-mode FETs
Regrowth Interface Resistances: Measured Data

When tested individually in separate experiments:

In-situ Mo Contact $\rho_c = 1 \, \Omega \cdot \mu m^2$

25 nm regrown InGaAs $R_{sh} = 70 \, \Omega/sq$

InGaAs-InGaAs re-growth resistance < 1 $\Omega \cdot \mu m^2$.

InGaAs-InP re-growth resistance = 6 $\Omega \cdot \mu m^2$ (on thick InP).