A 1.1V 150GHz Amplifier with 8dB Gain and +6dBm Saturated Output Power in Standard Digital 65nm CMOS Using Dummy-Prefilled Microstrip Lines

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Outline

• Introduction
• “Dummy-Prefilled” Microstrip Line
  – Structure and Modeling
• Design and Simulation
• Measurement Results
Beyond 100GHz: What Applications?

- Communication
  - Outdoor, indoor
- Imaging (Passive, active)
  - Security
  - All-weather radar
  - Medical
Beyond 100GHz: Why CMOS?

- Low-cost
- Low-power
- Large-scale Integration → Parallelism
  - Large monolithic phased array, imager.
- RF/mm-wave, IF/analog, DSP on a same die.
  - System-on-chip
  - Digital calibration of RF/analog circuit imperfections, process variations.
  - Reconfigurability and adaptability
What Challenges in 150GHz CMOS Amp?

• Low available FET gain, Low Supply Voltage
  – Careful FET layout & sizing
  – Multi-stage Common-Source

• Modeling uncertainties
  – Simple matching topology with microstrip (MS) lines

• Automatic “dummies” alter MS-line characteristics
  – Propose “Dummy-prefilled” MS-line

• Characterization
  – Full 2-port on-wafer TRL calibration
Finger design: Reduce $R_{g,ext}$ and $C_{gd}$ ($W_F=1\mu m$)

Wiring multiple fingers: Parallel versus Series
“Microstrip Line” in Nanoscale CMOS

- “Automatic” dummies/holes to meet metal density rules.
- Line capacitance increases
  - $\Delta C$ depends on E-field orientation $\rightarrow$ Anisotropic
- Direct E/M simulation nearly impossible
Possible Shapes of Dummy Pre-fillers

- “LINE” dummies
  - Parallel to current flow

- “LINE” dummies
  - Perpendicular to current flow

- “SQUARE” dummies
  - No preferred direction of current flow
Reducing Complexity in E/M Sim

E/M simulation feasible by significantly reducing # of dummies

Dummy Pre-fillers

Successive dummy-layer substitution by parallel-plate capacitor simulation

Dummy-free uniform dielectric with adjusted diel. constant
Line Inductance/Capacitance vs Fill Ratio

L per unit length
(317nH/m w/o fillers)

% change

25% Fill
W:S = 1:1

56% Fill
W:S = 3:1

C per unit length
(103pF/m w/o fillers)

% change

Fill Ratio (%)

+17%

+32%
Ground Plane Construction

- Solid GND plane not allowed
- Put holes, and strap M1 & M2

Where current flow is uniform (e.g. under MS-line)

Where current flow is not uniform (e.g. under bends, T-junction, radial stubs)
THRU-REFL-LINE (TRL) Calibration

1. **THRU**
   - Half THRU
   - Reference plane
   - Measurements normalized to the line impedance

2. **REFL**
   - (Open, short, etc)

3. **LINE**
   - (ΔL= 90 deg @center freq)

- **Amplifier Test**

**Notes:**
- REFL & LINE need not be accurately known
- Measurements normalized to the line impedance
3-Stage 150GHz Amplifier: Schematic

- No DC block: Forces \( V_{GS} = V_{DS} \) for M1 & M2, but eliminates loss and modeling uncertainties associated with DC-block cap
- FET size is chosen for low matching loss
- Radial stub for lower loss than quarter-wave TL

\[
\text{All TL's: } Z_0 = 51.2 \quad W=10u \quad (25\% \text{ fill})
\]
FET Sizing

constant-g circle (20mS) S22* (g22 ≈ g11)

constant-Q circle Z0

S11

Conjugate input/output/inter-stage match with shunt tuning stubs only.
Simulated 150-GHz Amplifier Gain

- Radial stub (45deg opening)
- AC short
- Open-stub $\frac{1}{4}\lambda$, $Z_0=34$, $W=20\mu$
- Open-stub $\frac{1}{4}\lambda$, $Z_0=51$, $W=10\mu$

Frequency (GHz):

- $P_{DC} = 25mW$
- $0.65V$ $1.1V$
Die Photograph

- Area
  - = 0.4mm$^2$ (w pads)
  - = 0.16mm$^2$ (w/o pads)

- Stack: 9 Cu + 1 Al
## S-parameter Measurement Setup

<table>
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<tr>
<th>GGB Probes</th>
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<th>OML Inc.</th>
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<tbody>
<tr>
<td>Probe Station</td>
<td>W/G</td>
<td>140-220GHz</td>
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<tr>
<td>WR05</td>
<td>mm-wave heads</td>
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<th>Agilent</th>
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<tbody>
<tr>
<td>W/G</td>
<td>8510C</td>
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<tr>
<td>mm-wave heads</td>
<td>VNA</td>
</tr>
</tbody>
</table>

![Image of measurement setup](image-url)
Can we trust the calibration?

- **Probe coupling** $<-40$ dB
- **Repeatability issues**
  - Probe placement
  - Probe contact resistance
Prefilled MS-Line: Measurement

1mm-long Line

-2.0 dB/mm @ 140 GHz

-2.8 dB/mm @ 200 GHz

E/M Sim.

LINE standard

E/M Sim (8% error)
Measured Amp. S-Parameters

- Peak $|S21| = 8.2$ dB
- $3$ dB BW = $27$ GHz
- $P_{DC} = 25.5$ mW
- $0.65$ V  $1.1$ V
S21 versus Current Density

![Graph showing S21 versus Drain Current Density (uA/um) with DC Power (mW) on the y-axis. The graph includes a diagram of a circuit with a range of 0.5~0.9V and a resistance symbol.]
S21 @Higher Drain Bias (M3)

V1=V2=V3<V4

0.5~0.9V

1.1V

DC power (mW) vs S21 (dB)
• Unconditionally stable over 140-200GHz.
Large-Signal Setup

- **Power correction**: Insertion calibration using W/G THRU & On-wafer THRU

- **Inputs**
  - **20 GHz Signal Source**
  - **x12 Freq. Multiplier**

- **Outputs**
  - **WR05 Variable Attenuator**
  - **WR05-WR10**
  - **Power Meter**

- **On-wafer DUT**

- **Probes**

- **Power Levels**:
  - $P_{IN} = -20 \text{dBm} \sim +15 \text{dBm}$
  - **Frequency**
    - $153 \text{GHz} \sim 175 \text{GHz}$

- **Loss**
  - $0.2 \text{dB}$

**Manufacturers**
- Virginia Diode Inc.
- Erikson Instruments.
Large-Signal Characteristics

$P_{sat} = +6.3\, \text{dBm}$

$\text{oP}_{1\text{dB}} = +1.5\, \text{dBm}$

Peak PAE = 8.4%

freq = 153GHz

$P_{DC} = 25.5\, \text{mW}$

0.65V  1.1V
Comparison of Measured S21

- VNA Measurement: Full 2-port TRL calibration
- Power Measurement: Insertion calibration
## Performance Summary

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<th>Technology</th>
<th>65nm digital CMOS</th>
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<td>Topology</td>
<td>3-stage Common-source</td>
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<tr>
<td>Center freq</td>
<td>150GHz</td>
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<tr>
<td>3dB BW</td>
<td>27GHz</td>
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<tr>
<td>Peak Gain</td>
<td>8.2dB</td>
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<tr>
<td>Input RL</td>
<td>-7.4dB</td>
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<tr>
<td>Output RL</td>
<td>-13.6dB</td>
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<tr>
<td>DC Power</td>
<td>25.5mW</td>
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<tr>
<td>( P_{1dB} )</td>
<td>+1.5dBm</td>
</tr>
<tr>
<td>( P_{sat} )</td>
<td>+6.3dBm</td>
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Conclusion

- Minimalistic Circuit Design Strategy
- “Design-rule Compliant” Transmission Line Structure and Modeling
- Linear/Power measurement up to 200GHz
- Highest frequency CMOS amplifier reported to date
Acknowledgement

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