THz Transistors, sub-mm-wave ICs, mm-wave Systems

Mark Rodwell
University of California, Santa Barbara
The End (of Moore's Law) is Near (?)

It's a great time to be working on electronics!

Things to work on:

- InP transistors: extend to 3-4 THz → GHz & low-THz ICs
- GaN HEMTs: powerful transmitters from 1-300 GHz
- Si MOSFETs: scale them past 16 nm
- III-V MOSFETs: help keep VLSI scaling (maybe)
- VLSI transistors: subvert Boltzmann → solve power crisis
- mm-wave VLSI: massively complex ICs to re-invent radio

Our focus today: THz transistors - how and why
Why

THz Transistors ?
Why Build THz Transistors?

500 GHz digital logic → fiber optics

THz amplifiers → THz radios → imaging, sensing, communications

Transistor Power Gain, dB

Frequency, Hz

precision analog design at microwave frequencies → high-performance receivers

Higher-Resolution Microwave ADCs, DACs, DDSs
What Would You Do With a THz Transistor?

640 Gb/s ETDM optical fiber links

300-1000 GHz imaging systems

mm-wave communication links
At High Frequencies The Atmosphere Is Opaque

Mark Rosker
IEEE IMS 2007
What Else Would You Do With a THz Transistor?

precision, high-performance analog microwave circuits

higher-resolution microwave ADCs, DACs, DDSs
How to Make THz Transistors
Simple Device Physics: Resistance

bulk resistance

contact resistance - perpendicular

contact resistance - parallel

$$R = \frac{\rho_{\text{bulk}} \cdot T}{A}$$

$$R = \frac{\rho_{\text{contact}}}{A}$$

$$R = \frac{\rho_{\text{contact}}}{A} + \rho_{\text{sheet}} \cdot \frac{W'}{3L}$$

Good approximation for contact widths less than 2 transfer lengths.
Simple Device Physics: Depletion Layers

**Capacitance**

\[ C = \varepsilon \cdot \frac{A}{T} \]

**Transit Time**

\[ \tau = \frac{T}{2\nu} \]

**Space-Charge Limited Current**

\[ \frac{I_{\text{max}}}{A} = \frac{2\varepsilon v}{T^2} \left( V_{\text{applied}} + V_{\text{depletion}} + 2\phi \right) \]

\[ I = C \frac{\Delta V}{\Delta T} \]

Where

\[ \frac{C}{I_{\text{max}}} = \frac{\tau}{V_{\text{applied}} + V_{\text{depletion}} + 2\phi} \]
Simple Device Physics: Thermal Resistance

**Exact**
Carslaw & Jaeger 1959

- **Long, Narrow Stripe**
  HBT Emitter, FET Gate
  
  \[
  R_{th} \approx \frac{1}{\pi K_{th}L} \ln\left(\frac{L}{W}\right) + \frac{1}{\pi K_{th}L}
  \]
  
  cylindrical heat flow
  near junction
  spherical heat flow
  far from junction

- **Square (L by L)**
  IC on heat sink
  
  \[
  R_{th} \approx \frac{1}{4 K_{th}L} + \frac{1}{\pi K_{th}L}
  \]
  
  planar heat flow
  near surface
  spherical heat flow
  far from surface
Simple Device Physics: Fringing Capacitance

\[
\frac{C}{L} \approx \varepsilon \cdot \frac{W}{T} + 1.5 \cdot \varepsilon
\]

parallel-plate fringing

\[
\frac{C}{L} \approx \varepsilon \cdot \left[ \text{slowly-varying function of } \frac{W_1}{G} \text{ and } \frac{W_2}{G} \right]
\approx (1 \text{ to } 3) \cdot \varepsilon
\]

wiring capacitance

FET parasitic capacitances

\[
\frac{C}{L} > \varepsilon
\]

VLSI power-delay limits

\[
\frac{C_{\text{parasitic}}}{L} \sim \varepsilon
\]

FET scaling constraints
**Frequency Limits and Scaling Laws of (most) Electron Devices**

\[ \tau \propto \text{thickness} \]
\[ C \propto \frac{\text{area}}{\text{thickness}} \]
\[ R_{\text{top}} \propto \frac{\rho_{\text{contact}}}{\text{area}} \]
\[ R_{\text{bottom}} \propto \frac{\rho_{\text{contact}}}{\text{area}} + \frac{\rho_{\text{sheet}}}{4} \frac{\text{width}}{\text{length}} \]
\[ I_{\text{max, space-charge-limit}} \propto \frac{\text{area}}{(\text{thickness})^2} \]
\[ \Delta T \propto \frac{\text{power}}{\text{length}} \times \log\left(\frac{\text{length}}{\text{width}}\right) \]

*To double bandwidth,*
- reduce thicknesses 2:1
- improve contacts 4:1
- reduce width 4:1, keep constant length
- increase current density 4:1
Bipolar Transistor Scaling Laws

Changes required to double transistor bandwidth:

<table>
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</tr>
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<tbody>
<tr>
<td>collector depletion layer thickness</td>
<td>decrease 2:1</td>
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<tr>
<td>base thickness</td>
<td>decrease 1.414:1</td>
</tr>
<tr>
<td>emitter junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>collector junction width</td>
<td>decrease 4:1</td>
</tr>
<tr>
<td>emitter contact resistance</td>
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<tr>
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Linewidths scale as the inverse square of bandwidth because thermal constraints dominate.
FET Scaling Laws

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<td>current density (mA/µm)</td>
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Linewidths scale as the inverse of bandwidth because fringing capacitance does not scale.
Thermal Resistance Scaling: Transistor, Substrate, Package

\[ \Delta T_{\text{substrate}} \approx \frac{P}{\pi K_{\text{InP}} L_E} \ln \left( \frac{L_e}{W_e} \right) + \frac{P}{\pi K_{\text{InP}}} \left( \frac{1}{L_e} - \frac{1}{D} \right) + \frac{P}{K_{\text{InP}}} \left( \frac{T_{\text{sub}} - D/2}{D^2} \right) \]

- cylindrical heat flow near junction
- spherical flow for \( r > L_e \)
- planar flow for \( r > D_{HBT}/2 \)

increases logarithmically
insignificant variation
increases quadratically if \( T_{\text{sub}} \) is constant

\[ \Delta T_{\text{package}} \approx \left( \frac{1}{4} + \frac{1}{\pi} \right) \frac{P_{\text{chip}}}{K_{\text{Cu}} W_{\text{chip}}} \]

\( T_{\text{sub}} = 40 \mu m \cdot (150 \text{ GHz} / f_{\text{clock}}) \)

Wiring lengths scale as \( 1/\text{bandwidth} \).
Power density, scales as \( (\text{bandwidth})^2 \).
Thermal Resistance Scaling: Transistor, Substrate, Package

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\]

Probable best solution:

Thermal Vias ~500 nm below InP subcollector

...over full active IC area.

\( T_{\text{sub}} = 40 \, \mu\text{m} \cdot (150 \, \text{GHz} / f_{\text{clock}}) \)
Electron Plasma Resonance: Not a Dominant Limit

\[ T_L = \text{area} = A \]

\[ T = L \]

\[ \tau = \text{frequency scattering} \]

\[ \tau = \text{bulk frequency relaxation} \]

\[ \tau = \text{dielectric frequency plasma} \]

\[ \tau = \text{m kinetic} \]

\[ \tau = \text{dielectric bulk} \]

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\[ \tau = \text{dielectric bulk} \]

\[ \text{InGaAs-\cdot} \]

\[ \text{THz 800 THz 7 THz 74} \]

\[ \text{THz 800 THz 7 THz 74} \]

\[ \text{cm/105.3} \]

\[ \text{cm/107} \]

\[ \text{InGaAs-\cdot} \]
Electron Plasma Resonance: Not a Dominant Limit
Electron Plasma Resonance: Not a Dominant Limit

\[ L_{\text{kinetic}} = \frac{T}{A q^2 n m^*} \]

\[ R_{\text{bulk}} = \frac{T}{A q^2 n m^* \tau_m} \]

\[ C_{\text{displacement}} = \frac{\varepsilon A}{T} \]
Electron Plasma Resonance: Not a Dominant Limit

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<tr>
<th>dielectric relaxation frequency ( f_{\text{dielectric}} )</th>
<th>scattering frequency ( f_{\text{scattering}} )</th>
<th>plasma frequency ( f_{\text{plasma}} )</th>
</tr>
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<tr>
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<td>( n - \text{InGaAs} ) ( 3.5 \cdot 10^{19} / \text{cm}^3 )</td>
<td>800 THz</td>
<td>7 THz</td>
</tr>
<tr>
<td>( p - \text{InGaAs} ) ( 7 \cdot 10^{19} / \text{cm}^3 )</td>
<td>80 THz</td>
<td>12 THz</td>
</tr>
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THz & nm Transistors: it's all about the interfaces

Metal-semiconductor interfaces (Ohmic contacts):
very low resistivity

Dielectric-semiconductor interfaces (Gate dielectrics):
very high capacitance density

Transistor & IC thermal resistivity.
THz
Bipolar Transistors
### InP Bipolar Transistor Scaling Roadmap

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<thead>
<tr>
<th></th>
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![Diagram of InP Bipolar Transistor](image)
InP DHBTs: September 2008

popular metrics:
- $f_t$ or $f_{\text{max}}$ alone
- $(f_t + f_{\text{max}})/2$
- $(1/f_t + 1/f_{\text{max}})^{-1}$

much better metrics:
- PAE, associated gain, mW/µm
- low noise amplifiers: $F_{\text{min}}$, associated gain, digital:
  - $f_{\text{clock}}$, hence
  - $(C_{cb} \Delta V / I_c)$,
  - $(R_{\text{ex}} I_c / \Delta V)$,
  - $(R_{bb} I_c / \Delta V)$,
  - $(\tau_b + \tau_c)$
512 nm InP DHBT

Laboratory Technology

500 nm mesa HBT
150 GHz M/S latches
175 GHz amplifiers

Production

( Teledyne )

500 nm sidewall HBT
DDS IC: 4500 HBTs
20-40 GHz op-amps

Z. Griffith
M. Urteaga
P. Rowell
D. Pierson
B. Brar
V. Paidi

\[ f_r = 405 \text{ GHz} \]
\[ f_{\text{max}} = 392 \text{ GHz} \]
\[ V_{\text{br, ceo}} = 4 \text{ V} \]

20 GHz clock

53-56 dBm OIP3 @ 2 GHz with 1 W dissipation
256 nm Generation InP DHBT

150 nm thick collector

$H_{21}$

$f_{\text{max}} = 780 \text{ GHz}$

$f = 424 \text{ GHz}$

70 nm thick collector

$H_{21}$

$f_{\text{max}} = 560 \text{ GHz}$

$f = 560 \text{ GHz}$

60 nm thick collector

$H_{21}$

$f_{\text{max}} = 218 \text{ GHz}$

$f = 660 \text{ GHz}$

Z. Griffith, E. Lind
J. Hacker, M. Jones

324 GHz Amplifier

200 GHz master-slave latch design

Acc.V Spe.Magn Det WD Exp 2.0 3.0 1000x SF 14.2 1 DHBT-35

133 nm, 187 nm, 5.75 \, \mu m

10.9 V 3.9 11000x SF 14.2 1 DHBT-35
324 GHz Medium Power Amplifiers in 256 nm HBT

ICs designed by Jon Hacker / Teledyne

Teledyne 256 nm process flow-
Hacker et al, 2008 IEEE MTT-S

~2 mW saturated output power
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![Diagram](image)
Conventional ex-situ contacts are a mess

THz transistor bandwidths: very low-resistivity contacts are required

**textbook contact**

- Metal
- Semiconductor

**with surface oxide**

- Metal oxides, etc.
- Semiconductor

**with metal penetration**

- Metal
- Semiconductor

*Interface barrier → resistance*

*Further intermixing during high-current operation → degradation*
Ohmic Contacts Good Enough for 3 THz Transistors

64 nm (2.0 THz) HBT needs ~ 2 $\Omega \cdot \mu m^2$ contact resistivities

32 nm (2.8 THz) HBT needs ~ 1 $\Omega \cdot \mu m^2$

**Contacts to N-InGaAs**:  
Mo \hspace{1cm} MBE in-situ \hspace{1cm} 2.2 (+/- 0.5) $\Omega \cdot \mu m^2$  
TiW \hspace{1cm} ex-situ \hspace{1cm} ~2.2 $\Omega \cdot \mu m^2$

**Contacts to P-InGaAs**:  
Mo \hspace{1cm} MBE in-situ \hspace{1cm} below 2.5 $\Omega \cdot \mu m^2$  
Pd/... \hspace{1cm} ex-situ \hspace{1cm} ~1 (+/- ?) $\Omega \cdot \mu m^2$

*measured emitter resistance remains higher than that of contacts.*
Process Must Change Greatly for 128 / 64 / 32 nm Nodes

control undercut → thinner emitter → thinner base metal → excess base metal resistance

Undercutting of emitter ends

{101}A planes: fast

{111}A planes: slow
128 / 64 nm process: where we are going

Developing scalable self-aligned base process

- 0.3 Ω-μm² resistivity emitter contacts - *in-situ, in MBE*

- 2 Ω-μm² resistivity base contacts - *in-situ, in MBE*

Target ~2000 GHz device
THz Field-Effect Transistors (THz HEMTs)
FET Scaling Laws

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*InGaAs HEMTs are best for mm-wave low-noise receivers... but there are difficulties in improving them further.*
Why HEMTs are Hard to Improve

1st challenge with HEMTs: reducing access resistance

- Low electron density under gate recess → limits current
- Gate barrier lies under S/D contacts → resistance

2nd challenge with HEMTs: low gate barrier

- High tunneling currents with thin barrier
- High emission currents with high electron density

III-V MOSFETs do not face these scaling challenges
III-V MOSFETs for VLSI → Also Helps HEMT Development

**What is it?**
MOSFET with an InGaAs channel

**Why do it?**
- Low electron effective mass → Higher electron velocity
- More current, less charge at a given insulator thickness & gate length
- Very low access resistance

**What are the problems?**
- Low electron effective mass → Constraints on scaling!
- Must grow high-K on InGaAs, must grow InGaAs on Si
III-V MOSFETs in Development

Top of gate

Side of gate

Mo S/D metal with N+ InAs underneath

InAs regrowth

Gate

Mo S/D metal with N+ InAs underneath

N+ source regrowth

N+ drain regrowth

Pulse doping

InGaAs well

Barrier
III-V MOSFETs as a Scaling Path for THz HEMTs

**Why?**
- Much lower access resistance in S/D regions
- Higher gate barrier $\rightarrow$ higher feasible electron density in channel
- Higher gate barrier $\rightarrow$ gate dielectric can be made thinner

**Estimated Performance (?)**
- 2 THz cutoff frequencies at 32 nm gate length
Applications of THz III-V Transistors
What Else Would You Do With a THz Transistor?

- Precision, high-performance analog microwave circuits

- Higher-resolution microwave ADCs, DACs, DDSs
mm-wave Op-Amps for Linear Microwave Amplification

Reduce distortion with strong negative feedback

Measured 20-40 GHz bandwidth
Measured 54 dBm OIP3 @ 2 GHz
New designs in fabrication
Simulated 56 dBm OIP3 @ 2 GHz
What Would You Do With a THz Transistor?

640 Gb/s ETDM optical fiber links

300-1000 GHz imaging systems

mm-wave communication links
670 GHz Transceiver Simulations in 128 nm InP HBT

Simulations @ 670 GHz (128 nm HBT)

**LNA:** 9.5 dB $F_{\text{min}}$ at 670 GHz

**PA:** 9.1 dBm $P_{\text{out}}$ at 670 GHz

**VCO:**
-50 dBc (1 Hz)
@ 100 Hz offset
at 620 GHz (phase 1)

**Dynamic divider:**
novel design,
simulates to 950 GHz

**Mixer:**
10.4 dB noise figure
11.9 dB gain

3-layer thin-film THz interconnects
thick-substrate $\rightarrow$ high-Q TMIC
thin $\rightarrow$ high-density digital
What Would You Do With a THz Transistor?

- 640 Gb/s ETDM optical fiber links
- 300-1000 GHz imaging systems
- mm-wave communication links
150 & 250 GHz Bands for 100 Gb/s Radio?

\[ \frac{P_{\text{received}}}{P_{\text{trans}}} = \left( \frac{D_t D_r}{16 \pi^2} \right) \left( \frac{\lambda}{R} \right)^2 \]

\[ P_{\text{received}}(4QPSK) = Q^2 \cdot kT \cdot F \cdot B \; ; \; Q \approx 6 \]

\[ D = \frac{4\pi A_{\text{eff}}}{\lambda^2} \]

125-150 GHz, 200-300 GHz: enough bandwidth for 100 Gb/s QPSK

150 GHz carrier, 100 Gbs/s QPSK radio:
30 cm antennas, 10 dBm power, fair weather → 1 km range

150 GHz band: Expect ~10-20 dB/km attenuation for rain
300 GHz band: expect ~20-30 db/km from 90% humidity
Interconnects within high-speed ICs
CPW has parasitic modes, coupling from poor ground plane integrity

Microstrip has high via inductance, has mode coupling unless substrate is thin.

We prefer (credit to NTT) thin-film microstrip wiring, inverted is best for complex ICs
mm-wave MIMO:

→ Wireless Links at

100's of Gb/s
mm-wave (60-80 GHz) MIMO → wireless at 40+ Gb/s rates?

Rayleigh Criterion:
Spatial angular separation of adjacent transmitters: \( \delta \theta_t = D / R \)
Receive array angular resolution: \( \delta \theta_r = \lambda / (N - 1)D \)
To resolve adjacent channels, \( \delta \theta_r \leq \delta \theta_t \Rightarrow (N - 1)D = \sqrt{\lambda R(N - 1)} \)

70 GHz, 1 km, 16 elements, 2 polarizations, 3.6 x 3.6 meter array, 2.5 GBaud QPSK → 160 Gb/s digital radio?
mm-wave MIMO: 2-channel prototype, 60 GHz, 40 meters

<table>
<thead>
<tr>
<th>Channel Number</th>
<th>Single Active Transmitter</th>
<th>Two Active Transmitters</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$&lt;10^{-5}$</td>
<td>$1.8 \times 10^{-6}$</td>
</tr>
<tr>
<td>2</td>
<td>$&lt;10^{-6}$</td>
<td>$1.8 \times 10^{-5}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Channel Suppression Ratio (dB)</th>
<th>10Mbps per Channel</th>
<th>600Mbps per Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>27.8</td>
<td>21.1</td>
</tr>
<tr>
<td>2</td>
<td>28.8</td>
<td>9.7</td>
</tr>
</tbody>
</table>
mm-wave MIMO: 4-channel prototype, 60 GHz, Indoor

4 x 622 Mb/s
60 GHz carrier
VSLI for mm-wave & sub-mm-wave systems
Billions of 700-GHz Transistors → Imaging & Arrays

65 nm CMOS: ~5 dB gain @ 200 GHz

22 nm will be much faster yet.

What can you do with a few billion 700-GHz transistors?

Build Transmitter / Receiver Arrays

100's or 1000's of transmitters or receivers
...on < 1 cm² IC area
...operating at 100-500 GHz.
3-stage 250GHz Amplifier Design

IBM: Pekarik, Jaganathan
UCSB: M. Seo

Designs in Fabrication
32 nm CMOS

Fcenter = 260GHz
Gain = 9.9dB
P\text{DC} = 15 mW
Millimeter-wave spectrum: new solutions needed

**mm-wave Bands → Lots of bandwidth**

\[
\left( \frac{P_{\text{received}}}{P_{\text{transmit}}} \right) = \left( \frac{1}{16 \pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\]

short wavelength → weak signal → short range

**highly directional antenna → strong signal → long range**

\[
\left( \frac{P_{\text{received}}}{P_{\text{transmit}}} \right) = \left( \frac{D_t D_r}{16 \pi^2} \right) \left( \frac{\lambda^2}{R^2} \right) e^{-\alpha R}
\]

narrow beam → must be aimed → no good for mobile

**monolithic beam steering arrays → strong signal, steerable**

\[
\frac{P_{\text{received}}}{P_{\text{transmit}}} = \frac{N_{\text{receive}} N_{\text{transmit}}}{16} \frac{\lambda^2}{R^2} e^{-\alpha R}
\]

32 x 32 array → 60-90 dB increased SNR → vastly increased range

→ multi-Gigabit mobile communications
Billions of 700-GHz Transistors → Imaging & Arrays

Arrays for point-point radio links:

\[ \text{bit rate} \cdot \text{distance}^2 \propto (\# \text{array elements})^2 \cdot \text{wavelength}^2 \]

Arrays for (sub)-mm-wave imaging:

\# resolvable pixels = \# array elements

Arrays for Spatial-Division-Multiplexing Networks:

\[ \# \text{independent beams} = \# \text{array elements} \leq \frac{4 \cdot \text{array area}}{\text{wavelength}^2} \]
THz Transistors
Why Build THz Transistors?

500 GHz digital logic → fiber optics

THz amplifiers → THz radios → imaging, sensing, communications

- Precision analog design at microwave frequencies → high-performance receivers
- Higher-Resolution Microwave ADCs, DACs, DDSs

Graph showing Transistor Power Gain, dB vs Frequency, Hz.
Device scaling (Moore's Law) is not yet over.

Scaling $\rightarrow$ multi-THz transistors.

Challenges in scaling:
contacts, dielectrics, heat

Multi-THz transistors:
for systems at very high frequencies
for better performance at moderate frequencies

Vast #s of THz transistors
complex systems
new applications.... imaging, radio, and more
end
MIMO Link: a Subsampled Multi-Beam Phased Array

Array places nulls at interfering transmitters

\[ ND^2 = \lambda R \]

Assuming \( N \times N \) square arrays