A 204.8GHz Static Divide-by-8 Frequency Divider in 250nm InP HBT

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Why Static Frequency Dividers?

**MS flip-flops are very widely-used high speed digital circuits:**
- Dividers are master-slave flip-flop with inverting feedback
- Connection as 2:1 frequency divider provides simple test method

**Standard benchmark of logic speed:**
- Performance comparisons across technologies

**Dynamic, super-dynamic, frequency dividers:**
- Higher maximum frequency than true static dividers
- Narrow-band operation → applications are limited

**High speed technology performance for static dividers:**
- 250nm InP HBT: NGAS 200.6GHz (2009), TSC/UCSB 204.8GHz (2010)
- Advanced SiGe HBT: Infinion 110+GHz
Fast divider design – identifying dominant gate delays

Gate Delay Determined by:

Depletion capacitance charging through the logic swing

$$\left( \frac{\Delta V_{LOGIC}}{I_C} \right) \left( C_{cb} + C_{be,depletion} \right)$$

Depletion capacitance charging through the base resistance

$$R_{bb} \left( C_{cb} + C_{be,depletion} \right)$$

Supplying base + collector stored charge through the base resistance

$$R_{bb} \left( \tau_b + \tau_c \right) \left( \frac{I_C}{\Delta V_{LOGIC}} \right)$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 6 \left( \frac{kT}{q} + R_{ex} I_C \right)$$

Delay not well correlated with HBT delay $1/(2\pi f_c)$.

$$\left( \frac{\Delta V_{LOGIC}}{I_C} \right) \left( C_{cb} + C_{be,depletion} \right)$$ is 60% - 80% of total.

Low $\left( C_{cb} / I_c \right)$ is a key HBT design objective.

$$\frac{C_{cb} \Delta V_{LOGIC}}{I_C} = \frac{\Delta V_{LOGIC}}{2V_{CE,min}} \left( \frac{A_{collector}}{A_{emitter}} \right) \left( \frac{T_C}{2v_{effective}} \right)$$

$R_{ex}$ must be very low for low $\Delta V_{logic}$ at high $J_e$

...Need to design for clock speed, not $f_T$ & $f_{max}$
200GHz dividers – collector design for 250nm HBTs

Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J / v_{sat} - qN_d)(T_c^2 / 2\varepsilon)$$

Collector Depletion Layer Collapse

$$V_{cb,\min} + \phi > +(qN_d)(T_c^2 / 2\varepsilon)$$

$$\Rightarrow J_{\max} = 2\varepsilon v_{sat} (V_{ce} + V_{ce,\min}) / T_c^2$$ (1-D collector current flow)

0.5um HBT, 150GHz divider, $J_e = 5mA/um^2$

$$C_{cb,1} \frac{\Delta V_{\text{logic}}}{I_C} = \varepsilon_o \varepsilon_r \frac{1}{2} A_{c,1} \frac{\Delta V_{\text{logic}}}{T_{C,1} J_{e,1} A_{e,1}}$$

0.25um HBT, 200GHz divider – vertical, lateral scaling for $J_e = 10mA/um^2$

$33\%$ reduction

Lateral scaling, current spreading for $J_e = 10mA/um^2$
Key HBT Scaling Limit → Emitter Resistance

ECL delay not well correlated with $f_\tau$ or $f_{\text{max}}$

Largest delay is charging $C_{cb}$

$$C_{cb} \frac{\Delta V_{\text{logic}}}{I_C} = \frac{\varepsilon_o \varepsilon_r A_{\text{collector}} \Delta V_{\text{logic}}}{J_e A_{\text{emitter}}} \quad \text{where } J_{e,max} \propto 1/T_c^2.$$  

→ $J_e \approx 10 \text{ mA/}\mu\text{m}^2$ needed for 200 GHz clock rate

Voltage drop of emitter resistance becomes excessive

$$R_{\text{ex}} I_c = \rho_{\text{ex}} J_e = (15 \Omega \cdot \mu\text{m}^2) \cdot (10 \text{ mA/}\mu\text{m}^2) = 150 \text{ mV}$$  

→ considerable fraction of $\Delta V_{\text{logic}} \approx 300 \text{ mV}$

Degrades logic noise margin

→ $\rho_{\text{ex}} \leq 7 \Omega \cdot \mu\text{m}^2$ needed for 200 GHz clock rate

This slide presented at BCTM 2004 for phase-I 150GHz divider.

HBT metrics here invoked to demonstrate the phase-III 200GHz divider.
$C_{cb}/I_c$ Charging Rate: ECL delays lower than CML

Chart 6

$V_{cb} = -0.3$ V

$0.0$ V

$0.2$ V

$V_{cb} = 0.6$ V

$\Delta V_{logic} = 300$ mV
Design approach for 200GHz logic

**Approach:** (new design elements presented in **bold**)

- Emitter coupled logic (ECL) topology
- Faster HBTs with lower $C_{cb}$ and lower $R_{ex} \ (\Omega-\text{um}^2)$
  - **Scaled device from 0.5um to 0.25um**
  - 150nm collector, 30nm base (400GHz $f_t$, 650GHz $f_{max}$)
- Reduce signal bus and loading delays
  - **Decreased device-to-device spacing**
- Thin-film microstrip with low loss $\varepsilon_r = 2.7$
- Resistive pulldown voltage biasing
- Small peaking inductance $L_{\text{peak}}$
- Emitter-follower HBTs having reduced $C_{cb}$ (Q1, Q2)
  - Collector-base DC voltage $V_{cb}$ increased

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![Schematic of a flip-flop configured as a static divider](image)

![Block diagram of Divide-by-8](image)
IC micrographs of the TSC 200GHz Static Frequency Dividers

Final fabrication, top-metal ground plane omitted

Divide-by-2 circuit, 36 HBTs (0.42×0.41-mm$^2$)

Divide-by-8 circuit, 108 HBTs (0.68×0.45-mm$^2$)
TSC/UCSB/GSC 150GHz divider (September 2004)

Summary of divider physical size:
- 5μm device-to-device spacing
- Two-sided collector HBT
- Latch width = 112μm
- Latch-to-buffer signal distance = 190μm

Close-up view of flip-flop interconnect, configured for divide-by-2
TSC/UCSB 200GHz divider – scaling summary

Summary of divider physical size:
- 2um device-to-device spacing
- One-sided narrower collector HBT
- Latch width = 50um (55% reduction)
- Latch-to-buffer signal distance = 64um
  - 66% reduction

Simulated CLK rate, 213GHz

DC power ~ 592mW

Close-up view of flip-flop interconnect, configured for divide-by-2

TSC mixed-signal technology cross-section
Probe-station for 200GHz divider testing

Mechanical attenuator

200GHz source

Output

Close-up showing wafer probes

WR-05 output power sweep

Output at 204.8GHz operation

200GHz 8x VDI source from UCSB

200GHz source

Probe station for 200GHz testing
Divide-by-8 static divider operating to 204.8GHz

- Peak divider toggle rate is 204.8GHz
  - Expected output at 25.60GHz, no spectral content at lower frequencies
- Input divider operational down to 4.0GHz to confirm static operation at all frequencies
  - 3rd-stage divider is operating at 1.0GHz clock (differential 350mV_{p-p}), 500MHz final output
- $P_{DC}$ of divide-by-8 circuit = 1.82W
  - Input divider operating at 204.8GHz, $P_{DC} = 592$mW
Sensitivity plot of the 204.8GHz static divider

- Sensitivity plot of the divider: 0.1-50GHz, 61.5-113.25GHz, 182.4-204.8GHz
- Expected trends of input power sensitivity versus frequency observed
- Source-free self oscillation (no input signal) reference to the input is 143GHz
Summary

- A record static divide-by-8 frequency divider has been demonstrated
  - 108 HBTs, all having 250nm features
  - TSC 4-metal layer, mixed-signal interconnect
  - Operational from 4.0GHz to 204.8GHz
  - Total $P_{DC} = 1.82W$, input divider only (no buffers) = 592mW

### Summary of the Fastest Reported Static Frequency Dividers

<table>
<thead>
<tr>
<th>Max. Clock Freq. (GHz)</th>
<th>Division Rate</th>
<th>Technology</th>
<th>Scale (nm)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>4</td>
<td>SiGe HBT</td>
<td>140</td>
<td>Infinion [3]</td>
</tr>
<tr>
<td>151.6</td>
<td>4</td>
<td>InP HBT</td>
<td>400</td>
<td>HRL [4]</td>
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<tr>
<td>152.0</td>
<td>2</td>
<td>InP HBT</td>
<td>500</td>
<td>Teledyne [1]</td>
</tr>
<tr>
<td>152</td>
<td>4</td>
<td>InP HBT</td>
<td>500</td>
<td>Lucent [5]</td>
</tr>
<tr>
<td>200.6</td>
<td>2</td>
<td>InP HBT</td>
<td>250</td>
<td>NGAS [6]</td>
</tr>
<tr>
<td>204.8</td>
<td>8</td>
<td>InP HBT</td>
<td>250</td>
<td>Teledyne, this work</td>
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</tbody>
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- Continued increases to static divider toggle rate require balanced reductions to HBT base $R_{bb}$ and emitter resistance $R_{ex}$, and junction capacitances $C_{je}$, $C_{cb}$.
  - Presentation (Tues-F1) by M. Urteaga discusses recent HBT developments
Acknowledgement

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Thank you!!